DATASHEET v1.0

nPM2100 Power Management IC

The nPM2100 Power Management IC (PMIC) is designed for primary (non-rechargeable) batteries in an extremely compact form factor. It features an ultra-efficient boost regulator and a wide range of energy-saving features, all of which extend the operating time for non-rechargeable battery applications. nPM2100 provides power regulation for low power microcontroller units (MCU) and System-on-Chip (SoC) devices, like the nRF52, nRF53, and nRF54L Series advanced wireless multiprotocol SoCs from Nordic Semiconductor.

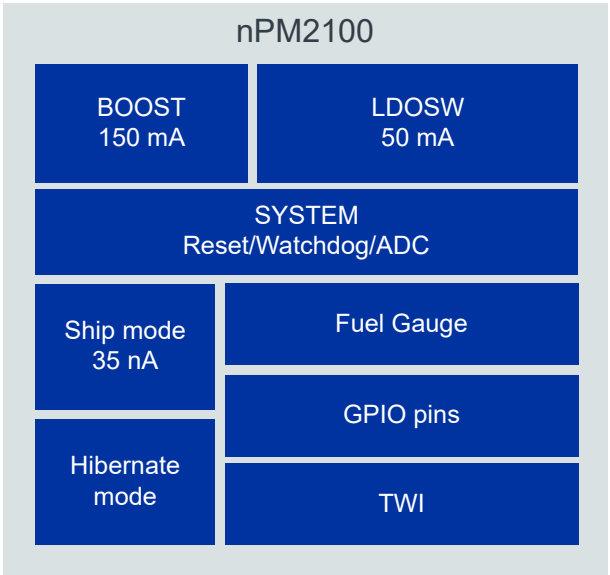
It features one boost regulator that supplies 1.8 V to 3.3 V output, from input voltages of 0.7 V to 3.4 V. Supported batteries include any battery that operates within the input voltage range of nPM2100.

The 150 nA IQ internal boost regulator is among the most efficient boost regulators on the market. A 35 nA Ship mode allows the device to be shipped with batteries inserted without draining the battery. Timed wakeup is available in Hibernate mode for applications that spend most of their time in deep sleep, lowering sleep current to 175 nA and extending battery lifetime by almost triple.

Designed to provide highly efficient power regulation for any primary-cell application, the nPM2100 comes with exceptional software support found in the nRF Connect SDK. The nPM2100 is also suitable for use with other host devices.

The nPM2100 supports precise algorithm-based fuel gauging. Standard voltage-based estimations are often inaccurate, leading to replacing batteries that are still charged, or unexpected shutdown. Instead, nPM2100 uses a voltage and temperature-based fuel gauge running on the host microprocessor for more accurate readings, ensuring full battery utilization with minimal additional load.

Bluetooth matter THREAD zigbee 2.4 GHz



Key features

- Ultra-efficient boost regulator
  - Up to 95%
  - 1.8 V to 3.3 V output
  - 150 mA max
- LDO/Load switch supplied by the boost regulator
  - 0.8 V to 3.0 V in LDO mode
  - 50 mA max
- 35 nA Ship Mode
- 175 nA Hibernate mode with wakeup timer
- Fuel gauge for primary cell batteries
- 0.7 V to 3.4 V supply voltage
- Multiple package options
  - 1.9x1.9 mm WLCSP
  - 4.0x4.0 mm QFN16

Applications

- Computer peripherals/HID
- Remote controls
- Smart home sensors
- Bluetooth® asset tracking
- Fitness accessories
- Personal medical devices

nPM FAMILY

Key features

Features:

- Ultra-high efficiency boost regulator
  - 0.7 V to 3.4 V input voltage range
  - 1.8 V to 3.3 V output voltage range
  - Up to 150 mA output current
  - Up to 95% efficiency
- Linear voltage regulator/load switch (LDOSW)
  - Input connected to boost output
  - 0.8 V to 3 V output voltage range
  - Up to 50 mA output current
- Ultra-low power Ship mode
  - Down to 35 nA current consumption
  - Wakeup or enter from a button press
  - Wakeup from breaking a connection (break-to-wake)
  - Enables the product to be shipped with batteries
  - Eliminates pull-tabs and enhances out-of-the-box experience
- Low power fuel gauge and System Monitor
  - Battery state-of-charge information when paired with Nordic fuel gauge algorithm running on host MCU
- Multifunction single-button support
  - Long-press hard reset
  - Ship mode enter/exit
  - Power ON/OFF
  - User interface
- Two general purpose input/output (GPIO) pins
  - Boost and LDO/load switch control
  - Interrupt output
- System management features
  - Down to 175 nA Hibernate mode with wakeup timer
  - Watchdog timer
  - Boot monitor
  - Power good output
  - GPIO pins
- I^2C compatible two-wire interface (TWI) for control and monitoring
- Low cost BOM and small solution size
  - Small form factor inductor and 5 capacitors
  - PCB area from 3.9x3.6 mm
- Package options
  - WLCSP 1.9x1.9 mm
  - QFN 4.0x4.0 mm

Applications:

- Computer peripherals/HID
- Remote controls
- Smart home sensors
- *Bluetooth*® Low Energy asset tracking
- Fitness accessories
- Personal medical devices

1 Revision history

Date	Version	Description
June 2025	1.0	First release

2 About this document

This document is organized into chapters that are based on the modules available in the IC.

2.1 Document status

The document status reflects the level of maturity of the document.

Document name	Description
Preliminary Datasheet	Applies to document versions up to 1.0. This document contains target specifications for product development.
Datasheet	Applies to document versions 1.0 and higher. This document contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Table 1: Defined document names

2.2 Core component chapters

Every core component has a unique capitalized name or an abbreviation of its name, such as BOOST, used for identification and reference. This name is used in chapter headings and references, and it will appear in the C-code header file to identify the component.

The core component instance name, which is different from the core component name, is constructed using the core component name followed by a numbered postfix, starting with 0. For example, BOOST0. A postfix is normally only used if a core component can be instantiated more than once. The core component instance name is also used in the C-code header file to identify the core component instance.

The chapters describing core components may include the following information:

- A detailed functional description of the core component
- Register configuration for the core component
- Electrical specification tables, containing performance data which apply for the operating conditions described in Recommended operating conditions on page 13

3 Product overview

nPM2100 is an integrated Power Management IC (PMIC) designed for primary (non-rechargeable) batteries in an extremely compact form factor. It features an ultra-efficient boost regulator and a wide range of energy-saving features, extending the operating time for non-rechargeable battery applications.

nPM2100 provides power regulation for low-power microcontroller units (MCU) and System-on-Chip (SoC) devices, like the nRF52, nRF53, and nRF54 Series advanced wireless multiprotocol SoCs from Nordic Semiconductor. The device is optimized for maximum efficiency and uses an I^2C compatible two-wire interface (TWI) for configuration. This interface enables easy access to a range of advanced functions, including Ship mode.

The boost regulator provides output voltages in the range of 1.8 V to 3.3 V and supports automatic Pass-through mode when the battery voltage exceeds the target output voltage. nPM2100 also includes a load switch/LDO that supports up to 50 mA output current and output voltages in the range of 0.8 V to 3.0 V.

nPM2100 supports battery voltages up to 3.4 V and can run from batteries such as one or two alkaline AA/AAA in series or one CR2032. It is able to start-up from 0.8 V battery voltage and run down to 0.7 V.

nPM2100 measures temperature and battery voltage, supporting algorithm-based fuel gauging. This is a unique feature in primary batteries for monitoring the state-of-charge in a non-rechargeable battery more accurately and eliminates unnecessary battery replacements.

Products can be shipped with the battery installed when using Ship mode. Ship mode supports sleep current down to 35 nA with multiple wakeup options, including a break-to-wake function that wakes a product from Ship mode when an electrical connection is broken. Hibernation mode uses an ultra-low power wakeup timer that enables timed wakeups. It provides lower power consumption than an SoC or MCU power-down.

The PMIC also features two GPIO pins that can control time-critical functions as an alternative to serial communication.

Application examples for nPM2100 include computer peripherals/HID, remote controls, smart home sensors, Bluetooth Low Energy asset tracking, fitness accessories and personal medical devices.

3.1 Block diagram

The block diagram illustrates the overall system.

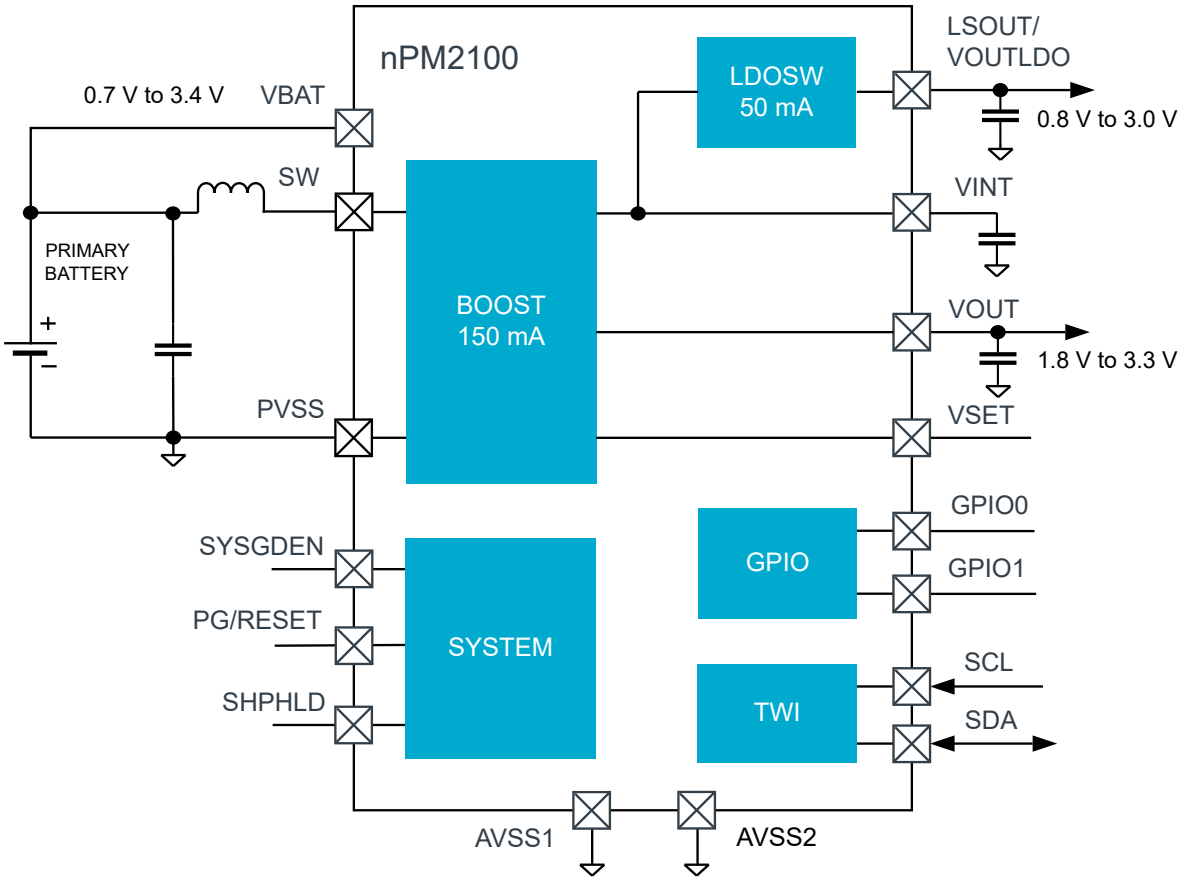


Figure 1: Block diagram

3.1.1 In-circuit configurations

The device is configurable for different applications and battery characteristics through input pins. The following pins must be configured before a power-on reset.

Pin	Function	Reference
VSET	BOOST output voltage selection VOUT=3.0 V when the pin is not connected VOUT=1.8 V when the pin is grounded	BOOST
SYSGDEN	Boot monitor (timer) control Boot monitor enabled when the pin is not connected Boot monitor disabled when the pin is grounded	Boot monitor

Table 2: In-circuit configurations

3.2 System description

The device has the following core components that are described in detail in their respective chapters.

- BOOST — Boost regulator on page 14

- LDOSW – Linear voltage regulator/load switch on page 39
- GPIO – General purpose input/output on page 51
- System Monitor on page 57
- TIMER — Timer/monitor on page 64
- TWI — I^2C compatible two-wire interface on page 80

3.3 Power-on reset and brownout reset

VBAT and VINT are the two power domains on the device.

When the following condition is met, a power-on reset (POR) occurs:

- VBAT domain – $VBAT > VBAT_{POR\_RISING}$
- VINT domain – $VINT > VINT_{POR}$

When the following condition is met, a brownout reset (BOR) occurs in the VINT domain and the device enters the COLD START state:

- $VINT < VINT_{BOR}$

When the following condition is met, a reset occurs in the VBAT domain and the device enters the NO SUPPLY state:

- $VBAT < VBAT_{POR\_FALLING}$

3.4 Device protection

The device includes the following protection:

- Thermal protection
- Overcurrent protection for BOOST
- Short circuit protection for LDOSW

Note: External load on the **VINT** pin is not allowed.

3.4.1 Thermal protection

If the die temperature exceeds the operating temperature range (TSD_{SD}), the device enters the COLD START state. When the device cools down, it returns to Active mode.

The die temperature is monitored when the BOOST is in High Power mode.

There is a warning threshold, TSD_{WARN}, that can be set to give an interrupt to the host.

3.4.1.1 Thermal specification

Symbol	Description	Min.	Typ.	Max.	Units
TSD_{WARN_RISING}	Thermal warning limit, rising threshold	85		105	°C
TSD_{SD_RISING}	Thermal shutdown limit, rising threshold	110		125	°C
TSD_{WARN_HYS}	Thermal warning limit, hysteresis		10		°C

Table 3: Thermal protection electrical specification

3.5 Operational modes and states

The device behavior when in specific operation modes and states is shown in the following diagram.

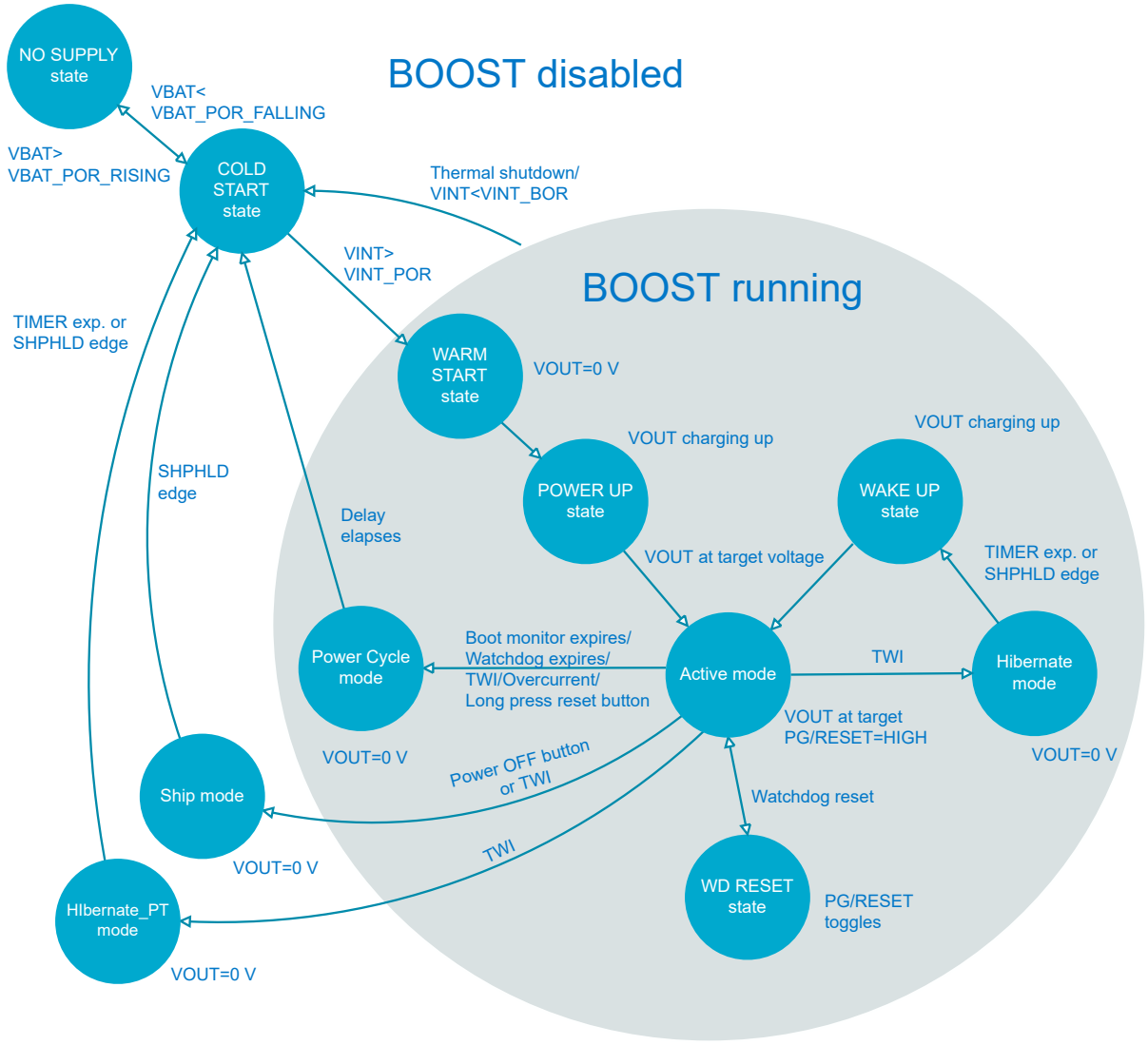


Figure 2: Operational modes and states diagram

Active mode

PG/RESET is set `HIGH` unless the Reset button is pulling it `LOW`.

Ship, Hibernate, and Hibernate_PT modes can be entered through TWI and register bits.

The chip enters the Ship mode when pressing and holding the **Ship** button for 2 seconds.

A reset is initiated by pressing and holding the **Reset** button for $t_{RST\_DEB\_L}$ seconds (default 10 s). This forces the device to enter the Power cycle mode. A watchdog reset takes the chip to WD RESET state.

A BOOST overcurrent event sets the chip to the Power cycle mode.

Die temperature rising over TSD_{SD} sets the chip to the COLD START state.

Hibernate mode

VOUT is discharged to ground. **VINT** remains supplied as BOOST is running in Ultra-Low Power mode. LDOSW can be configured to be ON in Ultra-Low Power mode. If enabled, the wakeup timer is running. **PG/RESET** is set LOW.

The **SHPHLD** pin and TIMER can set the chip to the WAKE UP state.

Please refer to Hibernate mode for more details.

Hibernate_PT mode

VOUT is discharged to ground. BOOST is in Pass-through mode so that **VINT** remains at **VBAT** level. LDOSW is OFF. If enabled, the wakeup timer is running. **PG/RESET** is set LOW.

A wakeup from the **SHPHLD** pin or TIMER causes the chip to enter the COLD START state and resets the registers.

Please refer to Hibernate mode for more details.

Ship mode

Everything is disabled and only the **SHPHLD** pin can wake up the chip.

Please refer to Ship mode for more details.

Power Cycle mode

BOOST and LDOSW are disabled in Power cycle mode. **VOUT** and **LSOUT/VOUTLDO** are discharged to ground and **PG/RESET** is set LOW. The registers will be reset.

When a delay of t_{PWRDN} occurs, the chip returns to Active mode.

3.5.1 Electrical specification

T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
IQ_{SHIP}	Current consumption from battery in Ship mode		35		nA
$IQ_{BREAKTOWAKE}$	Current consumption from battery in Break-to-wake mode		65		nA
IQ_{HIB}	Current consumption from battery in Hibernate mode with TIMER running (VINT=1.8 V, LDOSW disabled)		320		nA
IQ_{HIB_PT}	Current consumption from battery in Hibernate Pass-through mode with TIMER running (VBAT=3 V, T_J=25°C, LDOSW disabled)		175		nA
IQ_{ULP}	Current consumption from battery when BOOST is running in Ultra-Low Power mode, no load (VOUT=3 V, LDOSW disabled)		300		nA
IQ_{LP}	Current consumption from battery when BOOST is running in forced Low Power mode, no load (VOUT=3 V, LDOSW disabled)		2.7		µA
IQ_{HP}	Current consumption from battery when BOOST is running in forced High Power mode, no load (VOUT=3 V, LDOSW disabled)		7.2		mA
IQ_{PT}	Quiescent current, Pass-through mode (no load, OCP disabled)		170		nA
$VBAT_{COLD\_START}$	Battery voltage range, cold start (loaded voltage). The battery needs to be able to provide at least 10 mA (typ.) current during startup.	0.8		3.4	V
$VBAT_{OVR}$	Battery voltage range, operating (loaded voltage)	0.7		3.4	V
$VBAT_{POR\_RISING}$	Power-on reset rising threshold		0.6		V
$VBAT_{POR\_FALLING}$	Power-down reset falling threshold, VBAT domain		0.5		V
$VINT_{POR}$	Power-on reset rising, VINT domain		2.2		V
$VINT_{BOR}$	Brown-out reset, VINT domain		1.6		V

Table 4: System electrical specification

3.5.2 Electrical characteristics

The following graph shows typical Ship mode current consumption.

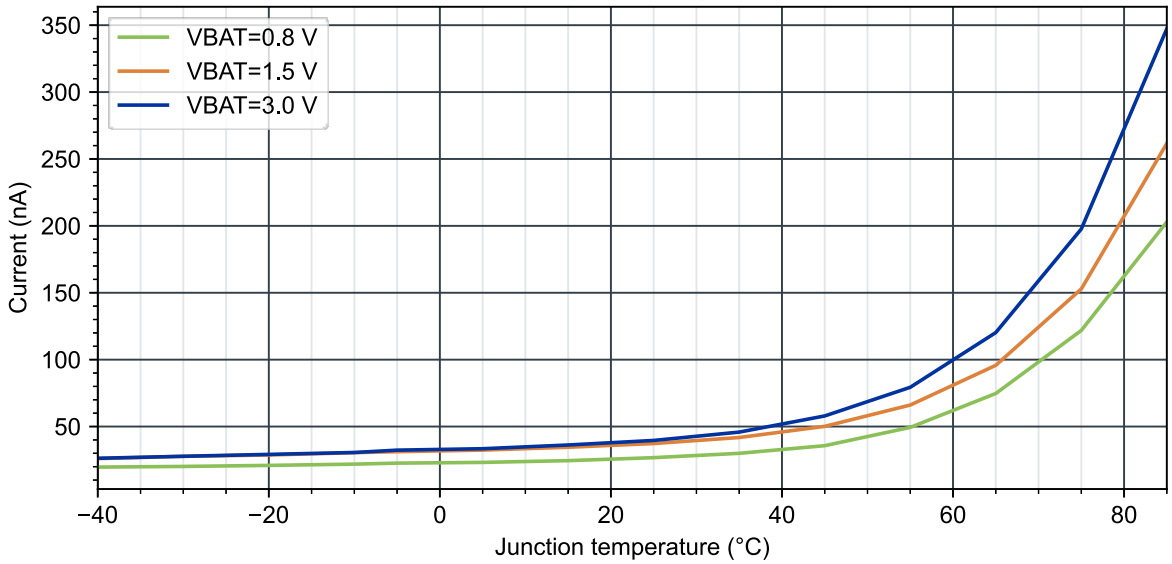


Figure 3: Ship mode current from the battery vs. junction temperature T_J

4 Absolute maximum ratings

Maximum ratings are the extreme limits to which the device can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

Pin	Notes	Min.	Max.	Units
VBAT, **SW**, **VOUT**, **LSOUT/VOUTLDO**, **VINT**	Power (wrt **AVSS1**)	-0.3	5.5	V
SDA, **SCL**, **VSET**, **PG/RESET**, **GPIO0**, **GPIO1**, **SYSGDEN**	Digital pins (wrt **AVSS1**)	-0.3	5.5	V
SHPHLD	Analog pins (wrt **AVSS1**)	-0.3	1.9	V

Table 5: Absolute maximum ratings

	Notes	Min.	Max.	Units
Storage temperature		-40	+125	°C
MSL WLCSP	Moisture sensitivity level		1	
MSL QFN	Moisture sensitivity level		2	
ESD HBM	Human body model class 2		2	kV
ESD CDM	Charged device model		500	V

Table 6: Environmental

5 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Parameter	Min.	Max.	Units
Supply voltage VBAT	0.7	3.4	V
Junction temperature T_J	-40	105	°C
Ambient temperature T_A	-40	85	°C

Table 7: Recommended operating conditions

5.1 Dissipation ratings

Thermal resistances and thermal characterization parameters as defined by JESD51-7 are shown in the following tables.

Symbol	Parameter	Value	Units
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	58	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	11	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	26	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	26.6	°C/W

Table 8: Thermal resistances and characterization parameters, WLCSP

Symbol	Parameter	Value	Units
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	22	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	20	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.75	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.9	°C/W

Table 9: Thermal resistances and characterization parameters, QFN

5.2 WLCSP light sensitivity

WLCSP package is sensitive to visible and near infrared light, which means that a final product design must shield the chip properly.

6 Core components

6.1 BOOST — Boost regulator

BOOST consists of a step-up boost regulator with the following features.

- Low voltage startup, even from a battery with high internal resistance
- Flexible and power efficient operating modes
  - High Power (HP)
  - Low Power (LP)
  - Ultra-Low Power (ULP)
  - Pass-through (PT)
- Pin selectable initial output voltage 1.8 V and 3.0 V
- Configurable output voltage in 50 mV steps from 1.8 V to 3.3 V
- Overcurrent protection (OCP) for pass-through operation

6.1.1 Output voltage selection

The output voltage range for BOOST is programmable with TWI. The default output voltage selection is defined by the **VSET** pin and is effective only at startup. A pin that is not connected configures VOUT to 3 V, and a grounded pin configures VOUT to 1.8 V.

Output voltage can be set in 50 mV steps in register BOOST.VOUT. Once the voltage is selected, register BOOST.VOUTSEL must be written to for the values to take effect.

6.1.2 Mode selection

BOOST efficiency and quiescent current consumption depend on the operating mode.

In Auto mode, BOOST switches automatically between High Power, Low Power, Ultra-Low Power, and Pass-through modes. In Low Power and Ultra-Low Power modes, the average output voltage of BOOST is 50 mV above the target level.

BOOST can be blocked from entering High Power mode (NOHP). In this case, it will automatically choose between Low Power, Ultra-Low Power, or Pass-through mode.

BOOST enters Pass-through mode when battery voltage is at least 100 mV above the target VOUT.

Exit criteria from Pass-through mode depends on the following settings:

- Auto or High Power – BOOST exits to High Power mode when VOUT drops 50 mV below the target VOUT
- Auto, No High Power or Low Power – BOOST exits to Low Power mode when VOUT falls below target VOUT +25 mV for longer than 30 µs

BOOST can be forced to High Power, Low Power, or Pass-through modes through registers BOOST.GPIO, BOOST.PIN, or BOOST.OPER. When forced to High Power or Low Power mode, it can still enter Pass-through mode. When in forced Low Power mode, Ultra-Low Power mode is not available.

> **Note:** A GPIO pulled `HIGH` should request for a lower power mode. For example, GPIO `HIGH`=Low Power (host sleeping) and GPIO `LOW`=High Power (host active). This ensures that the host is supplied when a host reset occurs.

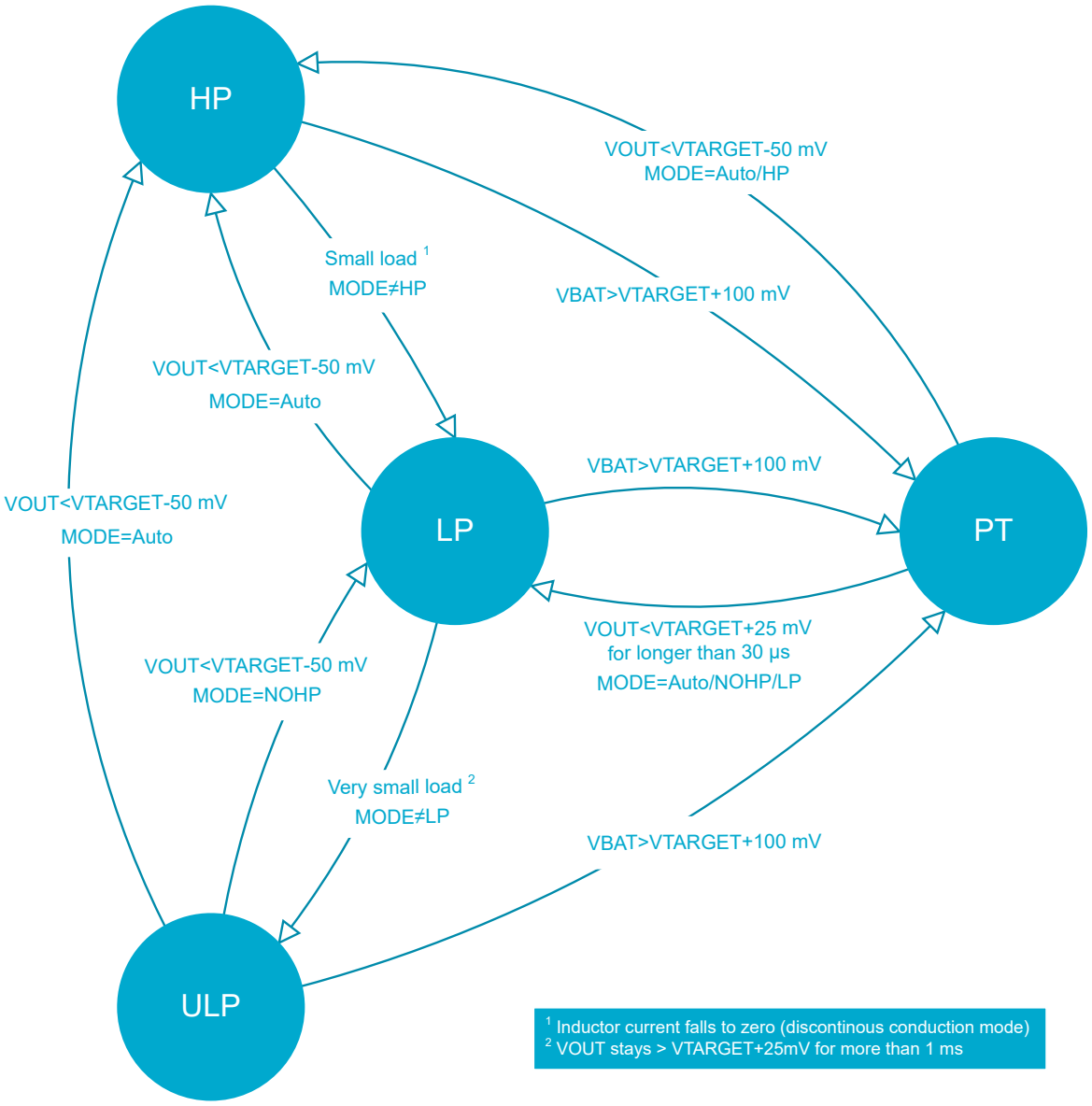


Figure 4: BOOST operating modes

High Power mode

High Power mode has the highest output current capability I_{VOUT_MAX} and highest quiescent current IQ_{HP}.

Low Power mode

Low Power mode provides less output current but also consumes much less quiescent current IQ_{LP} compared to High Power mode. See Figure Load current triggering mode change vs. VOUT on page 20 for details.

Ultra-Low Power mode

Ultra-Low Power mode has very low quiescent current consumption IQ_{ULP}.

Pass-through mode

Pass-through mode has very low quiescent current consumption IQ_{PT} and can provide output current up to $I_{VOUT\_MAX\_PT}$.

In case Pass-through is a valid operating mode for the application (e.g. a fresh battery has higher voltage than target VOUT), it is strongly recommended to set BOOST in Auto mode. The only additional configuration needed is the setting of the output voltage either by using pin VSET or register BOOST.VOUT. Once battery has been discharged and its voltage falls, BOOST automatically exits the Pass-through mode to regulate the output voltage.

In order to use forced Pass-through mode, BOOST output voltage VOUT has to be first configured to the minimum setting (1.8 V) and only then forced Pass-through mode is to be set in register BOOST.OPER. Forced Pass-through operation continues until the mode is changed by the host, even if battery voltage falls below 1.8 V.

6.1.3 Active output capacitor discharge

The **VOUT** pin is discharged to **AVSS1** when the chip enters Ship, Hibernate, Hibernate_PT, or Power Cycle mode.

6.1.4 Electrical specification

Electrical parameters have been measured using a 2.2 µH Taiyo Yuden inductor (LSCNB1608HKT2R2MD), C_{VBAT}=10 µF, C_{VINT}=22 µF, C_{VOUT}=2.2 µF. T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
$VBAT_{START}$	Regulator power stage input voltage range, cold start	0.8		3.4	V
$VBAT_{OPER}$	Regulator core part input voltage range, operating	0.7		3.4	V
$VBAT_{PT}$	Regulator core part input voltage range, Pass-through mode	1.8		3.4	V
$VOUT_{PROG}$	Programmable output voltage range (except Pass-through mode)		1.8 to 3.3		V
$VOUT_{STEP}$	Output voltage step		50		mV
$VOUT_{LP}$	Average VOUT level in Low Power and Ultra-Low Power modes		VOUT.LVL + 0.05		V
$VOUT_{LP\_RIPPLE}$	VOUT ripple in Low Power and Ultra-Low Power modes		70		mVp-p
$I_{VOUT\_MAX\_PT}$	Maximum output current, Pass-through mode			150	mA
$POUT_{MAX}$	Maximum output power, High Power mode (3.0<VOUT≤3.3 V, loaded VBAT≥1.25 V)			450	mW
I_{VOUT_MAX}	Maximum output current, High Power mode (VOUT≤3.0 V, loaded VBAT≥1.25 V)			150	mA
C_{VBAT}	Effective input capacitance on VBAT pin	3.5			µF
C_{VINT}	Effective capacitance on VINT pin	3.5			µF
C_{VOUT}	Effective capacitance on VOUT pin	0.7		15	µF
$VOUT_{ACCURWC}$	Output voltage accuracy, High Power mode, includes line and load regulation (loaded VBAT≥1.25 V)	-5		5	%
$VOUT_{ACCUR}$	Output voltage accuracy, High Power mode, excluding load and line regulation (loaded VBAT=1.25 V, T_J=25°C)	-2		2	%
F_{BOOST}	Switching frequency in High Power mode		2		MHz
EFF_{ULP1V5}	Efficiency (VBAT=1.5 V, VOUT=1.8 V, I_{VOUT}=0.1 mA, Ultra-Low Power mode)		87		%
EFF_{ULP2V9}	Efficiency (VBAT=2.9 V, VOUT=3 V, I_{VOUT}=0.1 mA, Ultra-Low Power mode)		91		%
EFF_{LP1V5}	Efficiency (VBAT=1.5 V, VOUT=1.8 V, I_{VOUT}=10 mA, Low Power mode)		88		%
EFF_{LP2V9}	Efficiency (VBAT=2.9 V, VOUT=3 V, I_{VOUT}=10 mA, Low Power mode)		92		%
EFF_{HP1V5}	Efficiency (VBAT=1.5 V, VOUT=1.8 V, I_{VOUT}=110 mA, High Power mode)		88		%

Symbol	Description	Min.	Typ.	Max.	Units
EFF_{HP2V9}	Efficiency (VBAT=2.9 V, VOUT=3 V, I_{VOUT}=110 mA, High Power mode)		93		%
$ILIM_{BOOST}$	Input (valley) current limiter ILIM range, High Power mode		100 to 800		mA
$ILIM_{STEP}$	ILIM step (register setting)		100		mA
$VBAT_{MON}$	Input voltage monitoring: VBATMINL and VBATMINH range		0.65 to 3.15		V
$VBATMIN_{STEP}$	Step for VBATMINL and VBATMINH		50		mV
$VOUT_{MON}$	Threshold range for output voltage monitoring, VOUTMIN and VOUTWRN		1.7 to 3.25		V
$VOUT_{STEPSIZE}$	Step size for VOUTMIN and VOUTWRN		50		mV
OCP_{BOOST_PT}	Overcurrent protection limit for the PMOS transistor in Pass-through mode		325		mA

Table 10: BOOST electrical specification

6.1.5 Electrical characteristics

The graphs show typical electrical characteristics for BOOST when supplied by an alkaline AA battery. They have been measured using a 2.2 µH Taiyo Yuden inductor (LSCNB1608HKT2R2MD), C_{VBAT}=10 µF, C_{VINT}=22 µF, and C_{VOUT}=2.2 µF, unless mentioned otherwise.

The following three figures show efficiency in Auto mode for various output voltages.

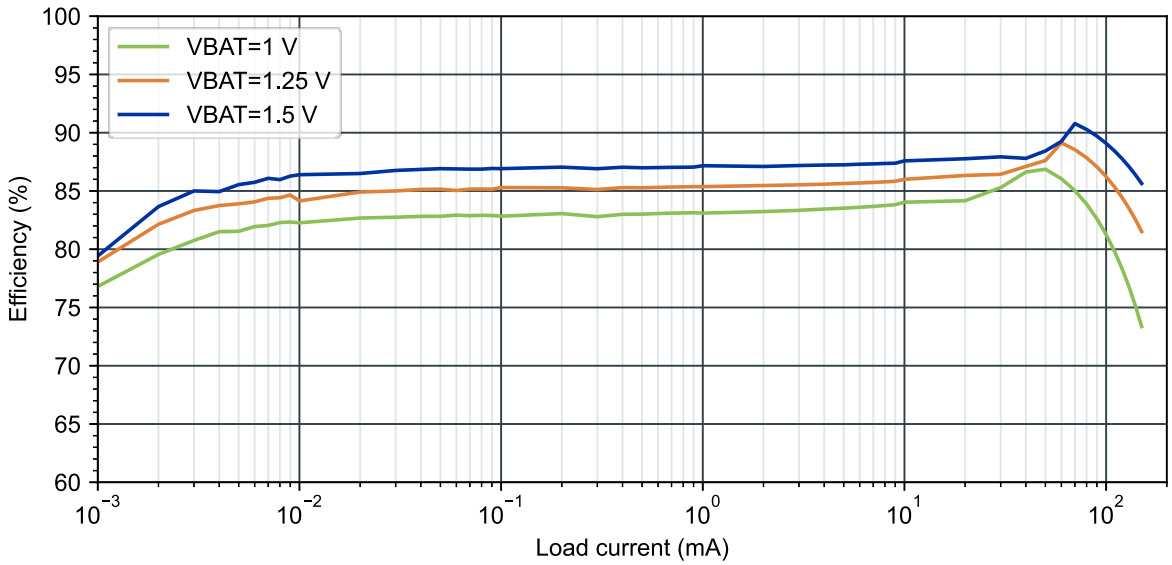


Figure 5: Efficiency, VOUT=1.8 V

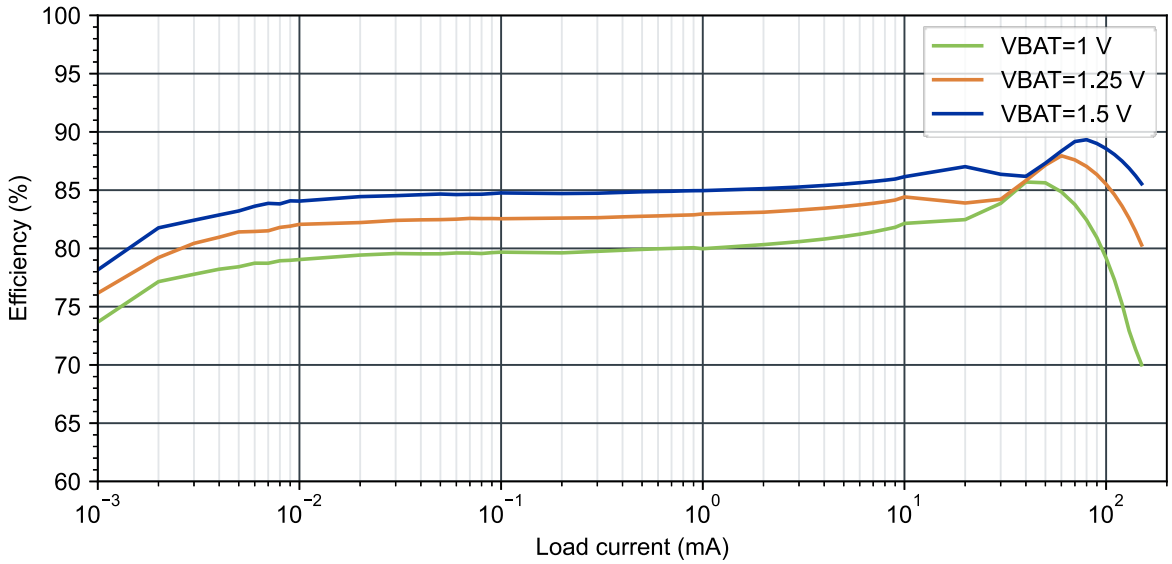


Figure 6: Efficiency, VOUT=3.3 V

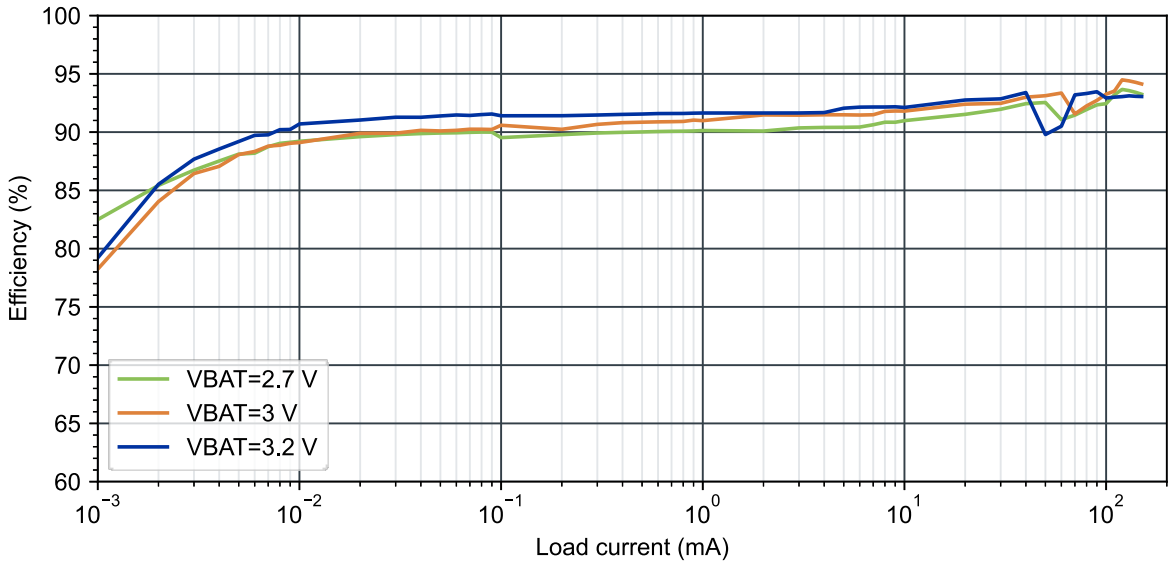


Figure 7: Efficiency, VOUT=3.3 V

The following figure shows the typical load current threshold in Auto mode where BOOST changes from Low Power to High Power mode.

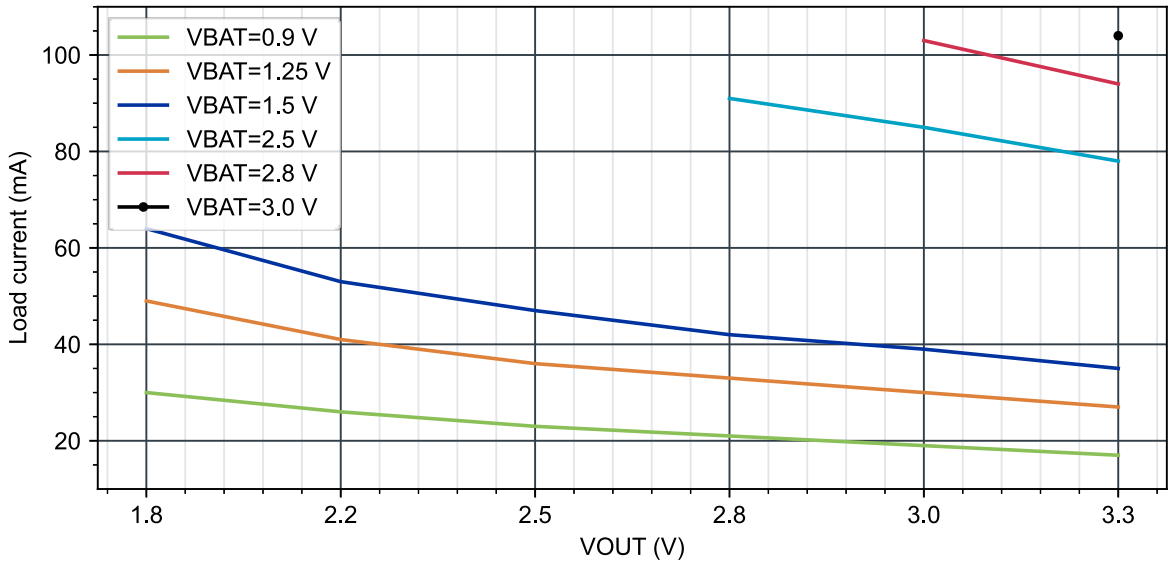


Figure 8: Load current triggering mode change vs. VOUT

The following two figures show device startup at various **VSET** configurations when an alkaline AA battery is inserted.

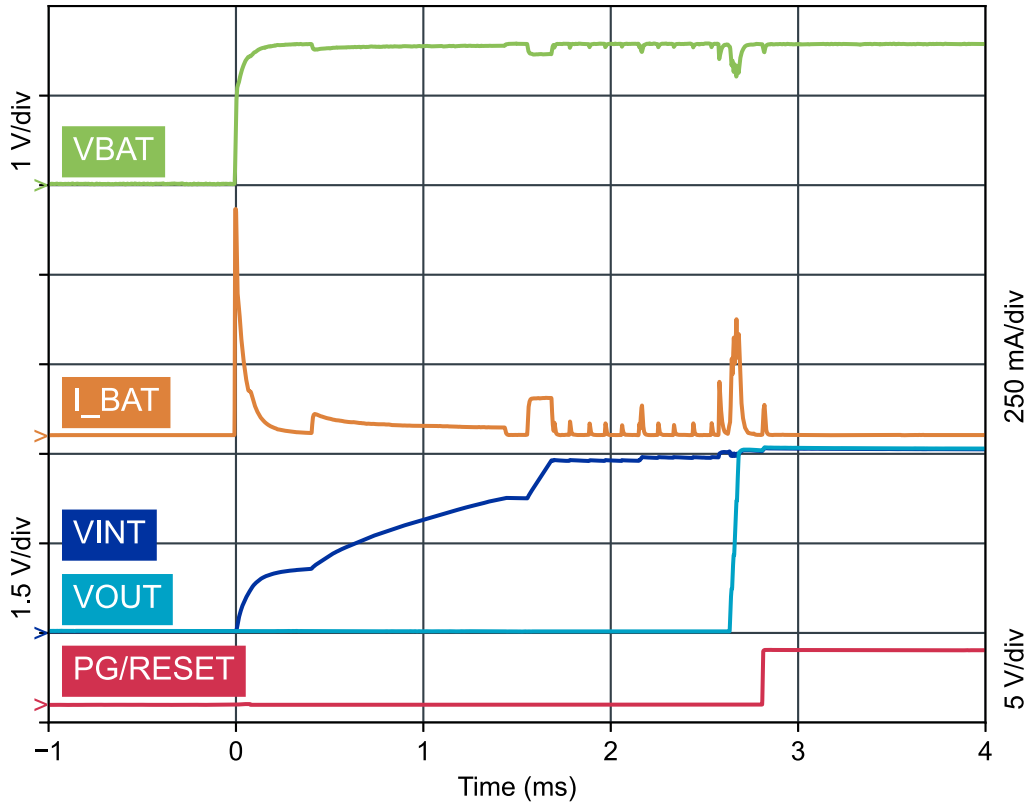


*Figure 9: Battery insertion, **VSET** not connected*

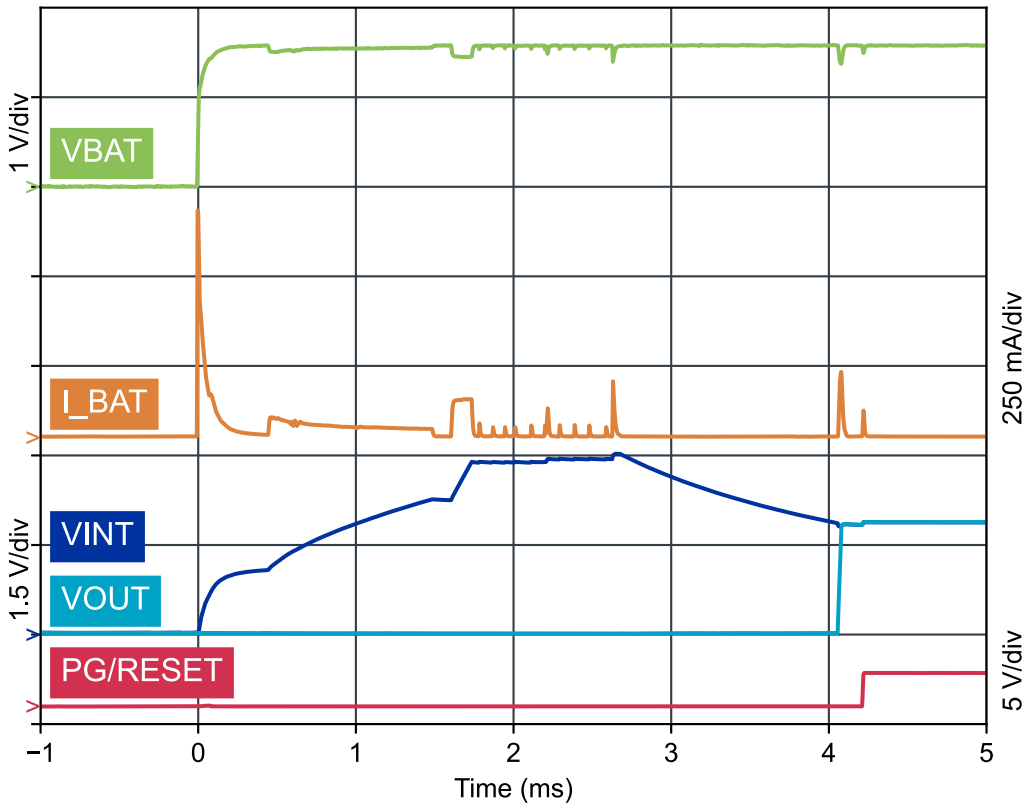


*Figure 10: Battery insertion, **VSET** connected to ground*

The following two figures show load regulation in High Power mode for various output voltages.

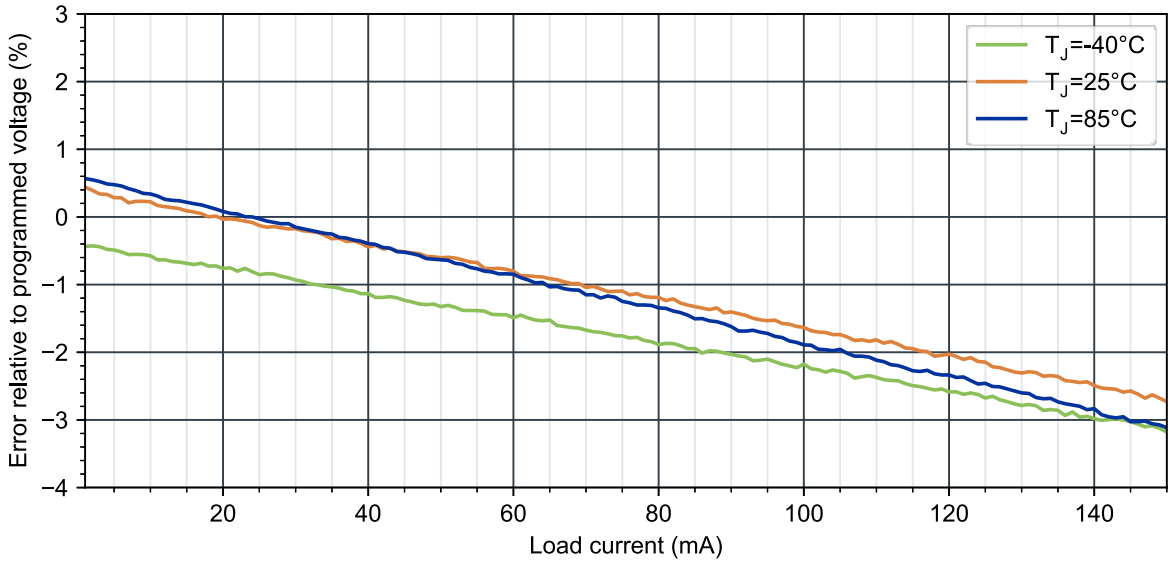


Figure 11: Load regulation, VOUT=1.8 V (VBAT=1.5 V)

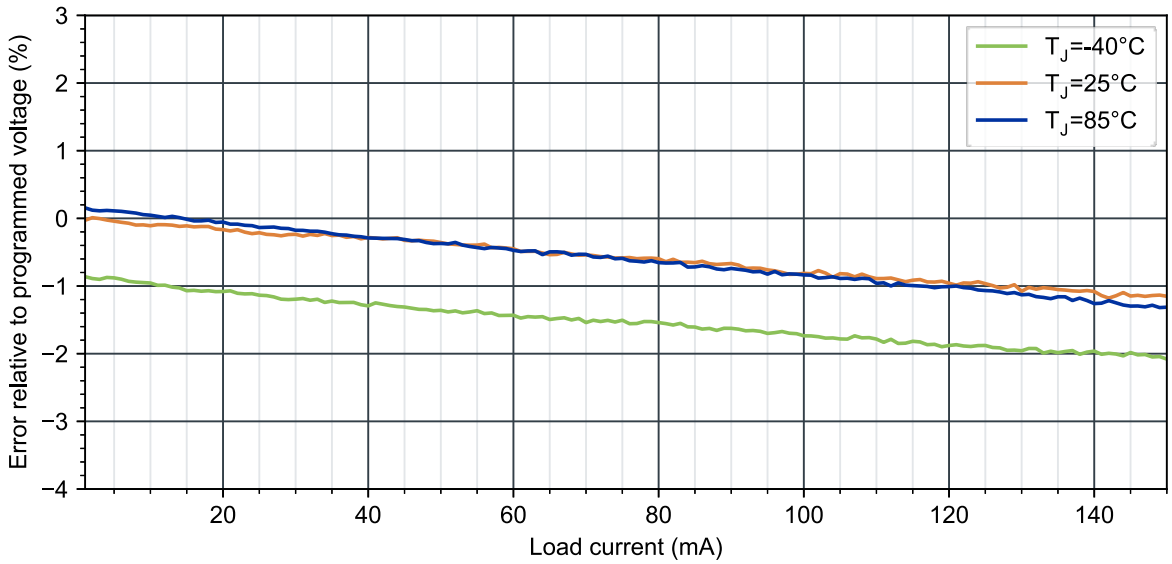


Figure 12: Load regulation, VOUT=3.0 V (VBAT=2.5 V)

The following two figures show load regulation in Auto mode for various output voltages.

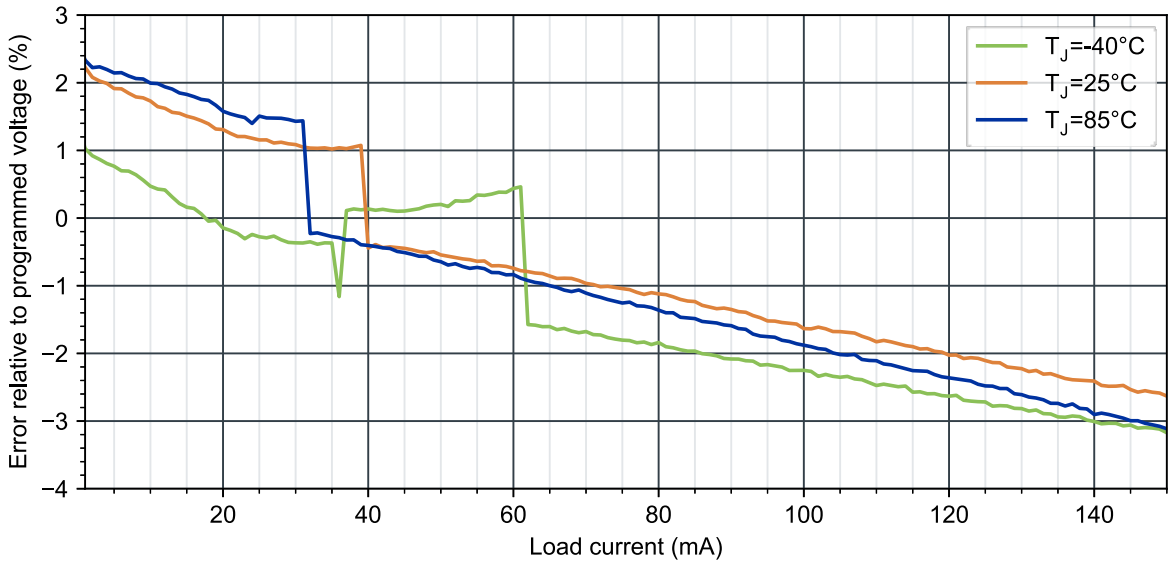


Figure 13: Load regulation, VOUT=1.8 V (VBAT=1.5 V)

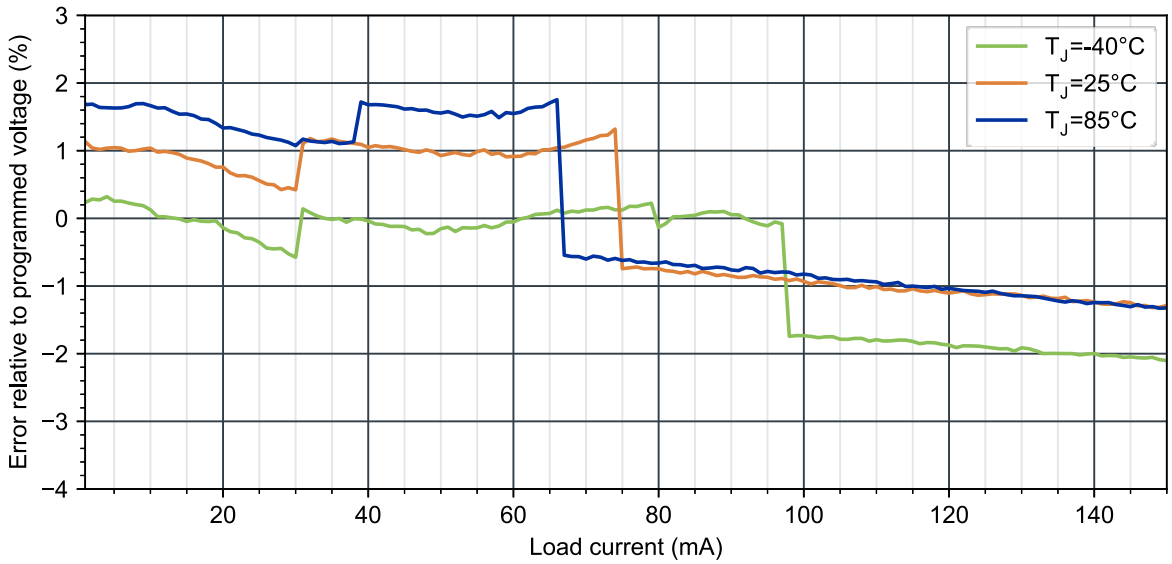


Figure 14: Load regulation, VOUT=3.0 V (VBAT=2.5 V)

The following two figures show load transient in Auto mode (automatic mode change from Low Power mode to High Power mode, and back) when supplied by an alkaline AA battery. Load changes from 1 mA to 100 mA in 10 µs.

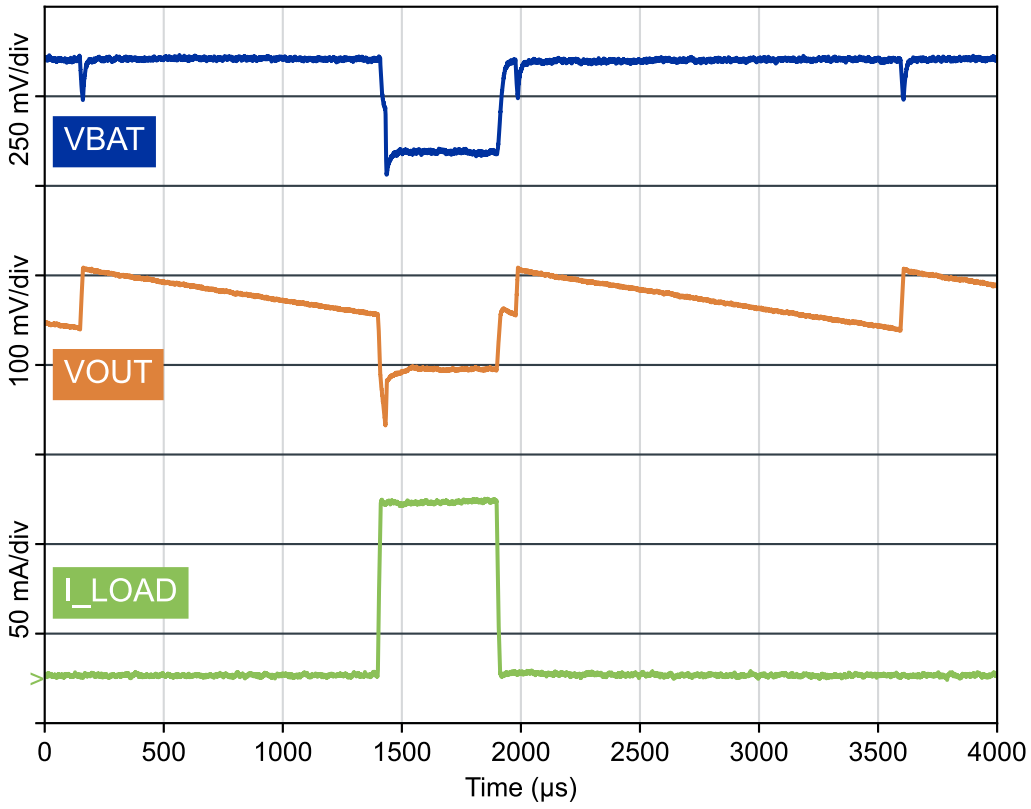


Figure 15: Load transient, VOUT=1.8 V

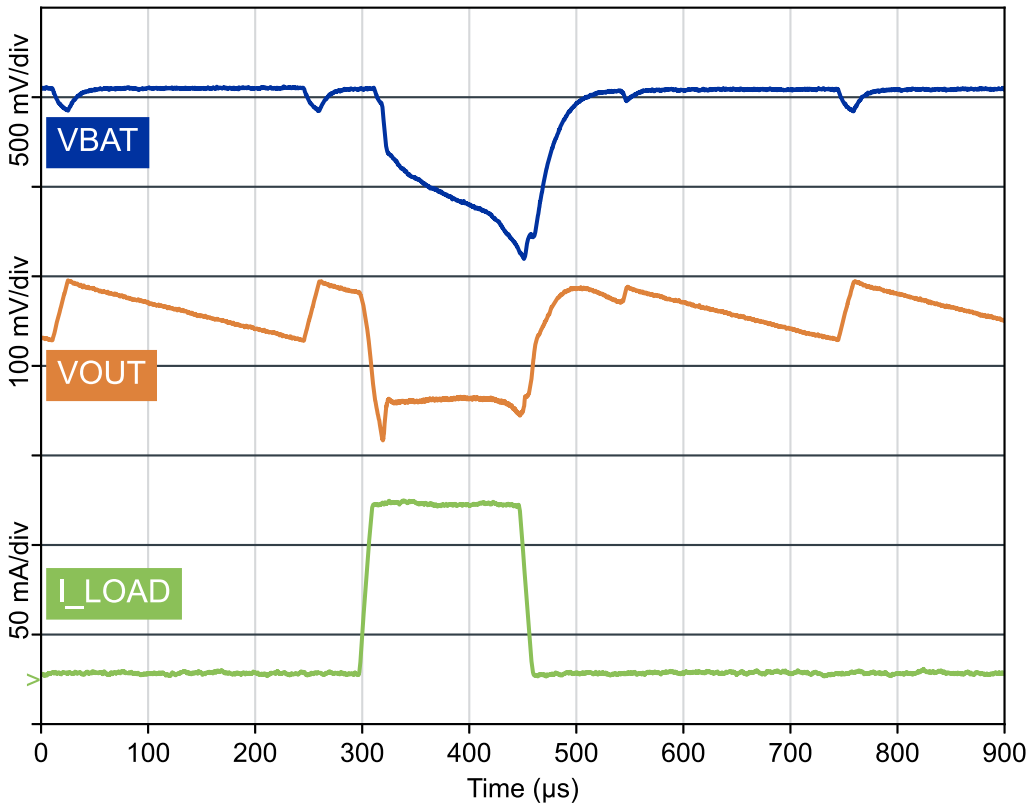


Figure 16: Load transient, VOUT=3.0 V

The following two figures show load transient in Low Power mode when supplied by an alkaline AA battery. Load changes from 1 mA to 100 mA in 10 µs.

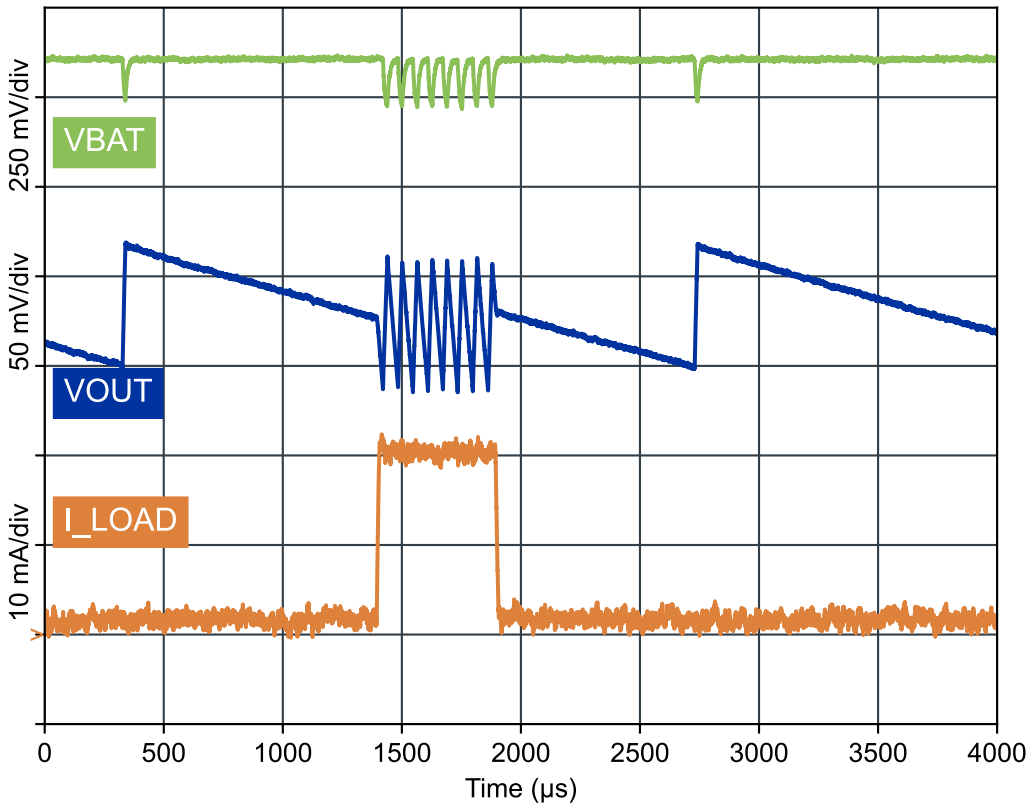


Figure 17: Load transient, VOUT=1.8 V

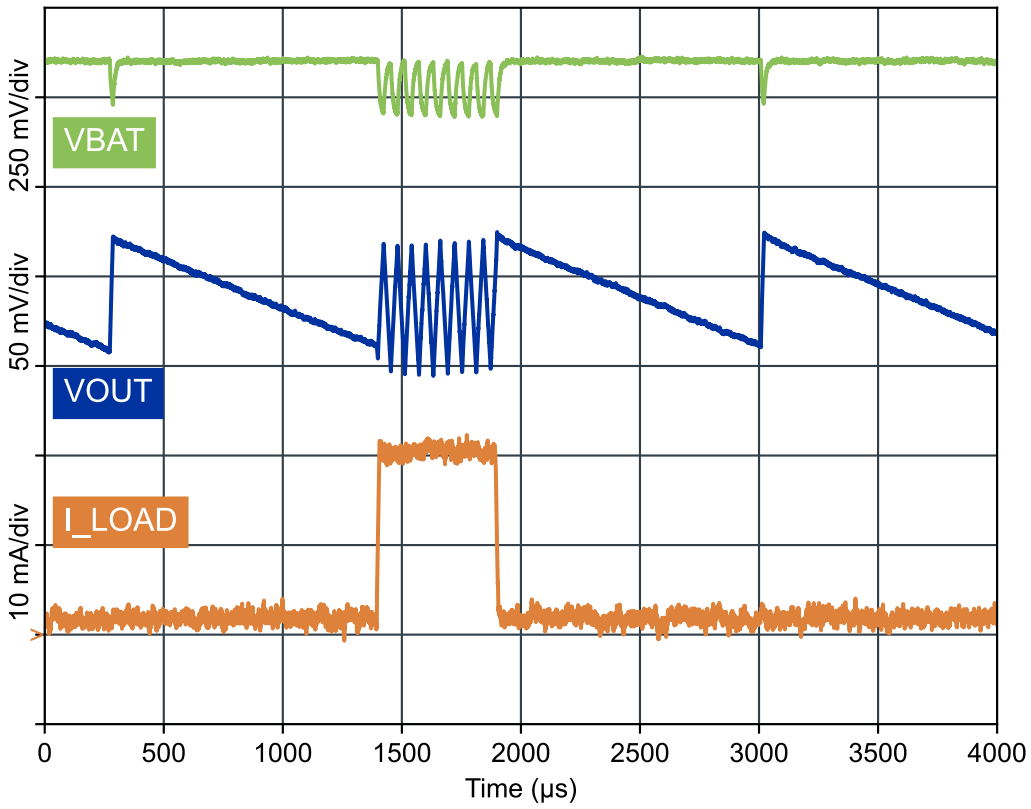


Figure 18: Load transient, VOUT=3.0 V

The following figure shows mode change from Low Power to High Power mode using GPIO control when supplied by an alkaline AA battery. Load is 10 mA.

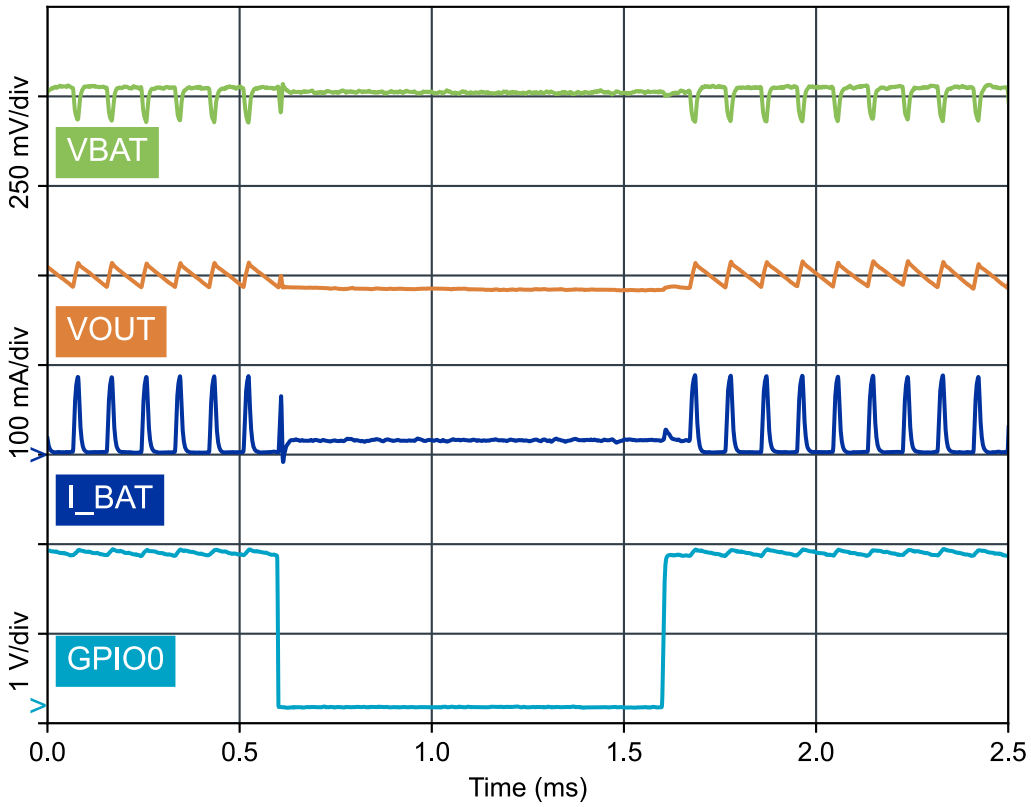


Figure 19: Mode change, VOUT=1.8 V

The following two figures show output voltage programming via TWI from 1.8 V to 2.5 V in various modes without load when supplied by an alkaline AA battery (LDOSW is in High Power mode, no load).

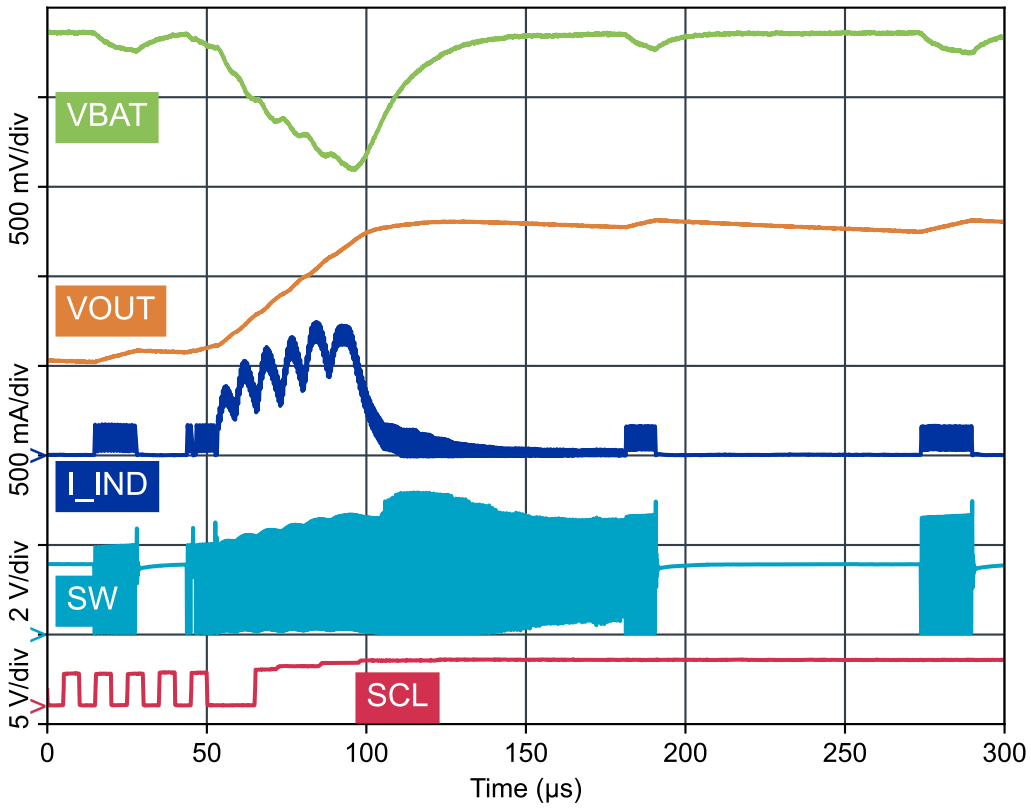


Figure 20: Output voltage programming, Auto mode

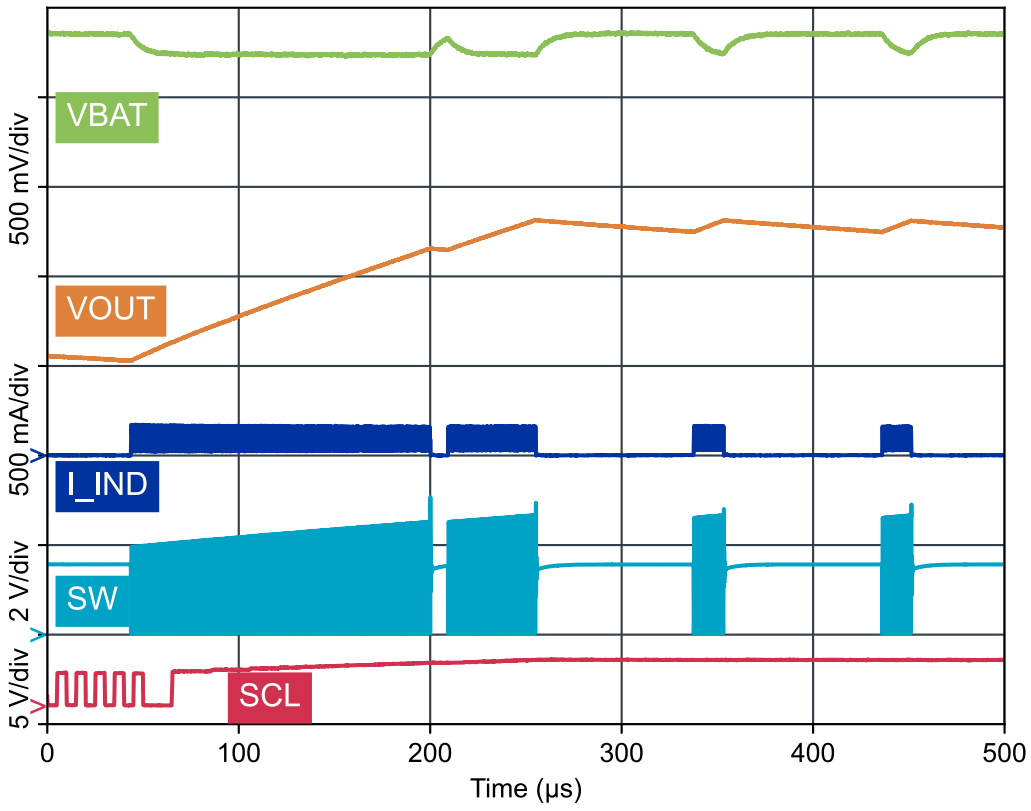


Figure 21: Output voltage programming, Low Power mode

The following figure shows output voltage programming via TWI from 2.5 V to 1.8 V in Low Power mode without load when supplied by an alkaline AA battery (LDOSW is in High Power mode, no load).

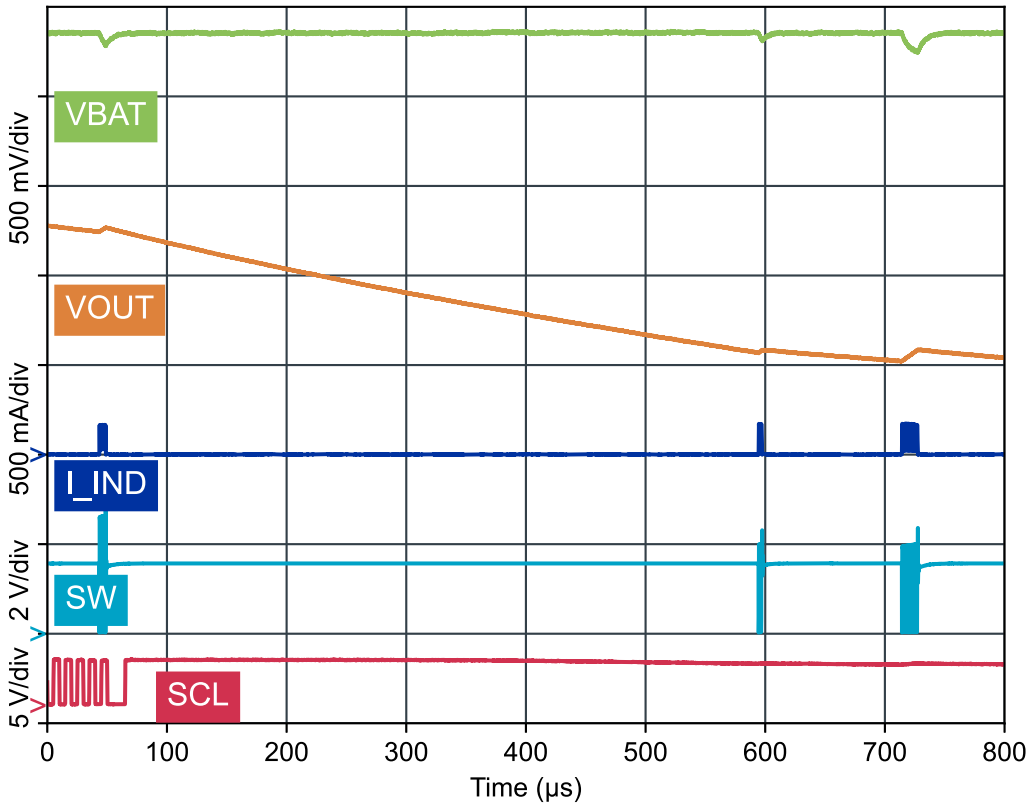


Figure 22: Output voltage programming downwards

The following two figures show switching waveforms in various modes when VOUT=3.0 V when supplied by an alkaline AA battery.

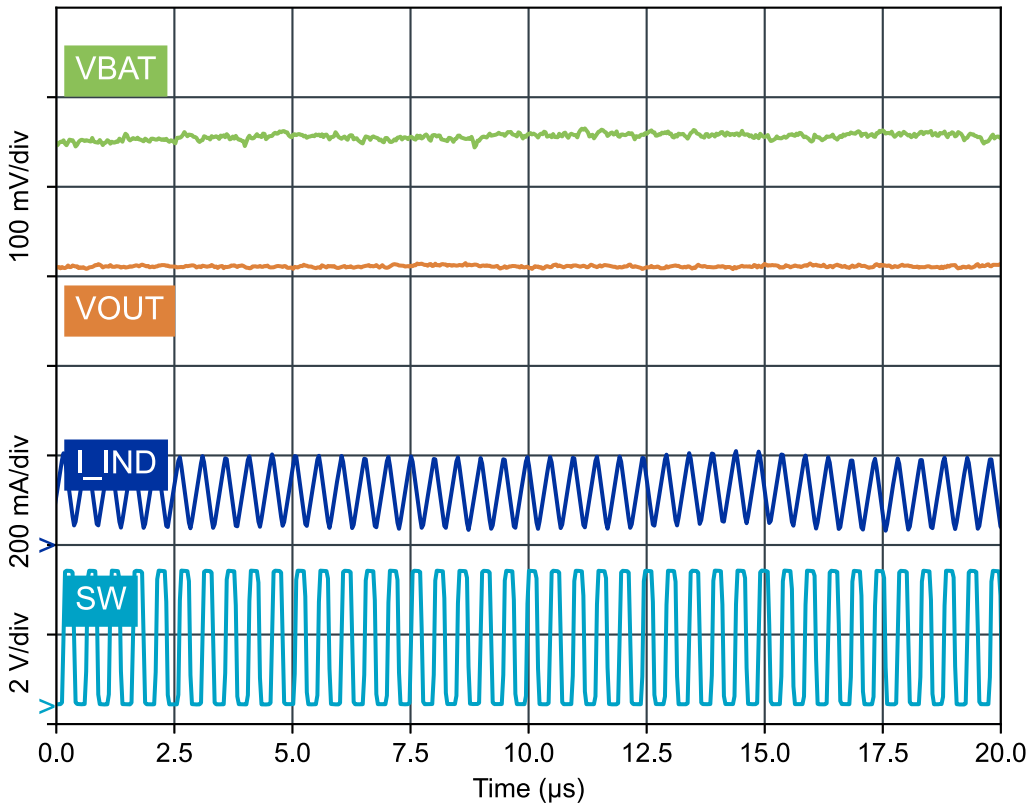


Figure 23: Switching waveforms in High Power mode, load=50 mA

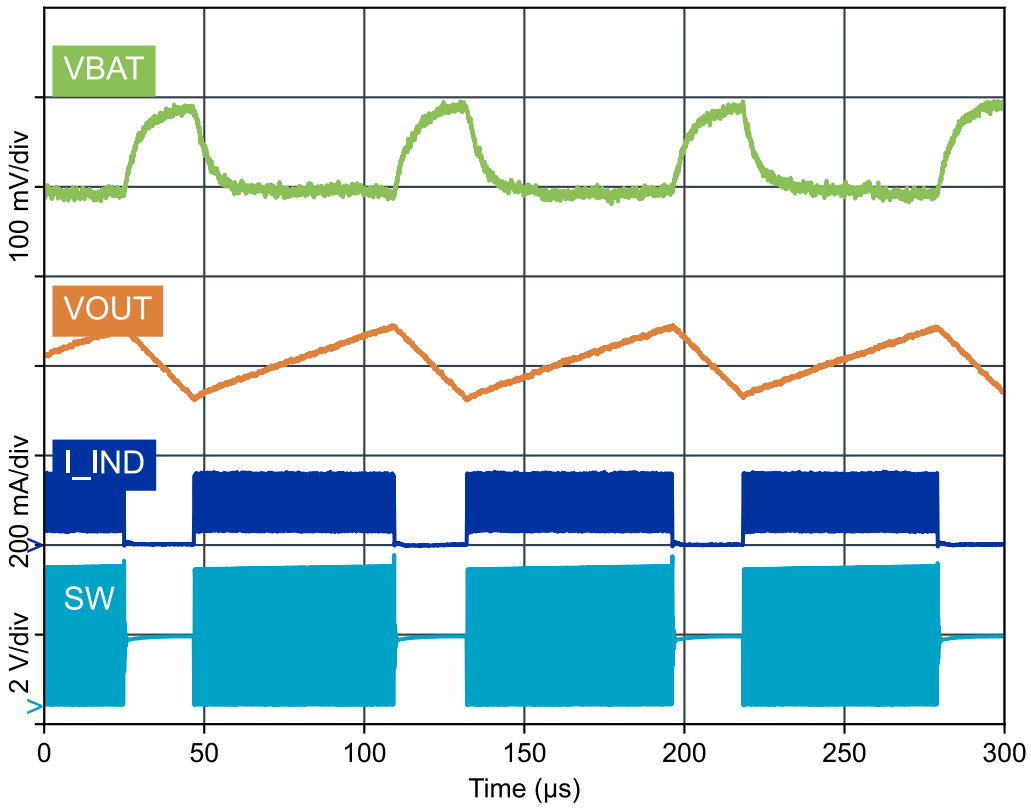


Figure 24: Switching waveforms in Low Power mode (load=30 mA)

The following figure shows switching waveforms when VOUT=1.8 V and load=10 mA when supplied by an alkaline AA battery.

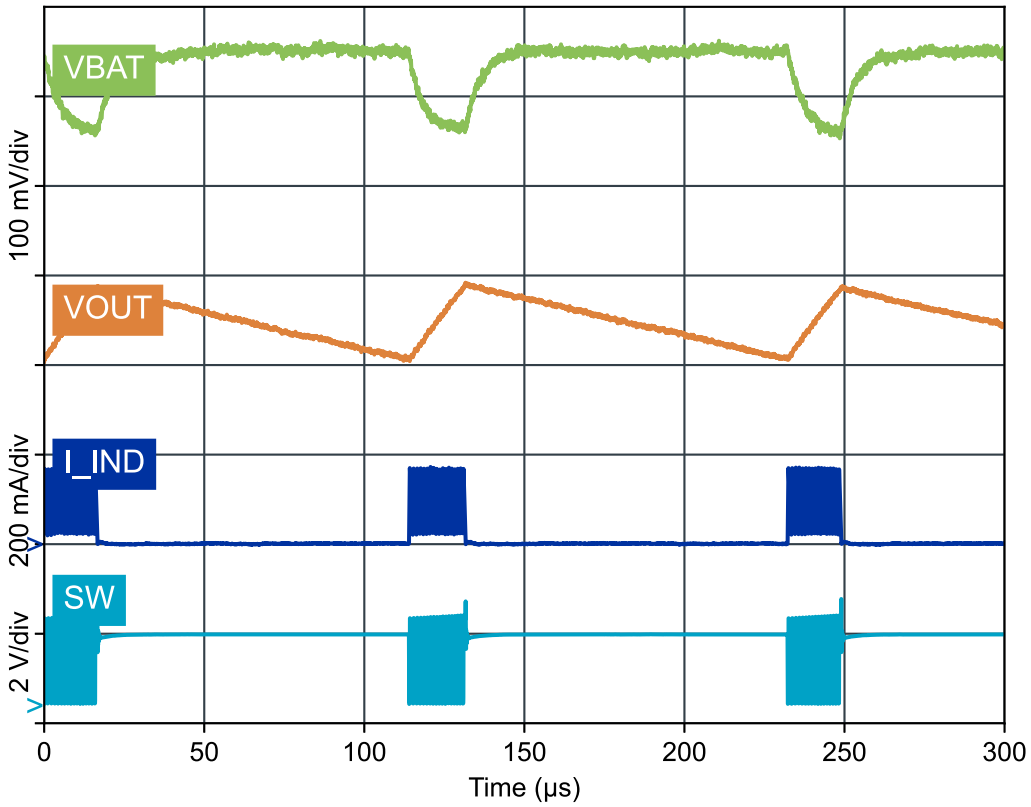


Figure 25: Switching waveforms in Ultra-Low Power mode

The following figure shows VOUT ripple frequency vs. load in Low Power mode.

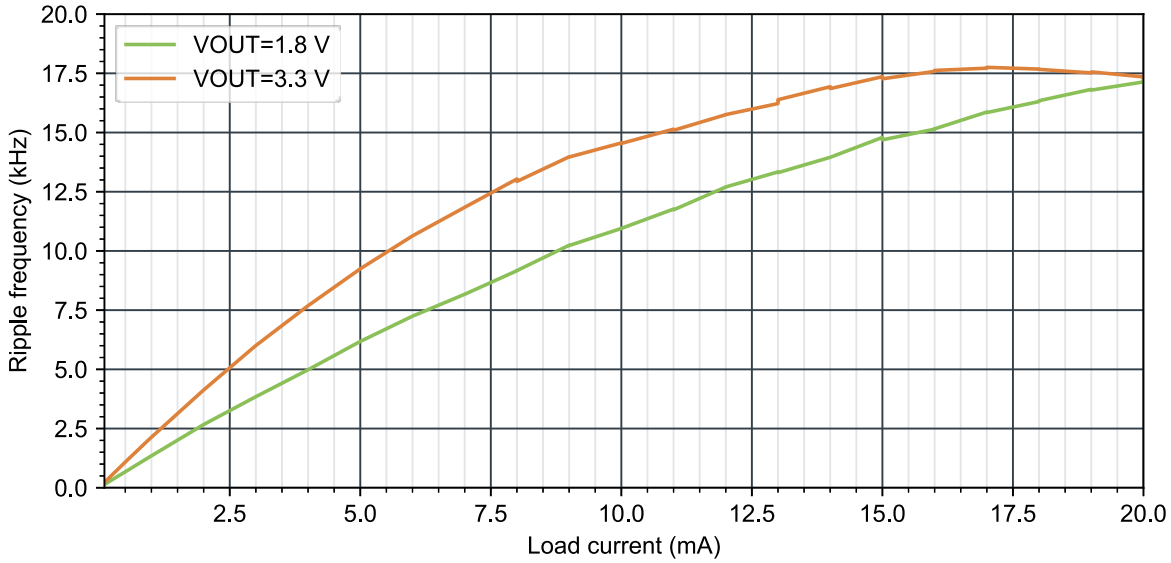


Figure 26: Ripple frequency vs. load current (VBAT=1.5 V)

The following two figures show alkaline AA battery removal for various output voltages (LDOSW in High Power mode, no load).

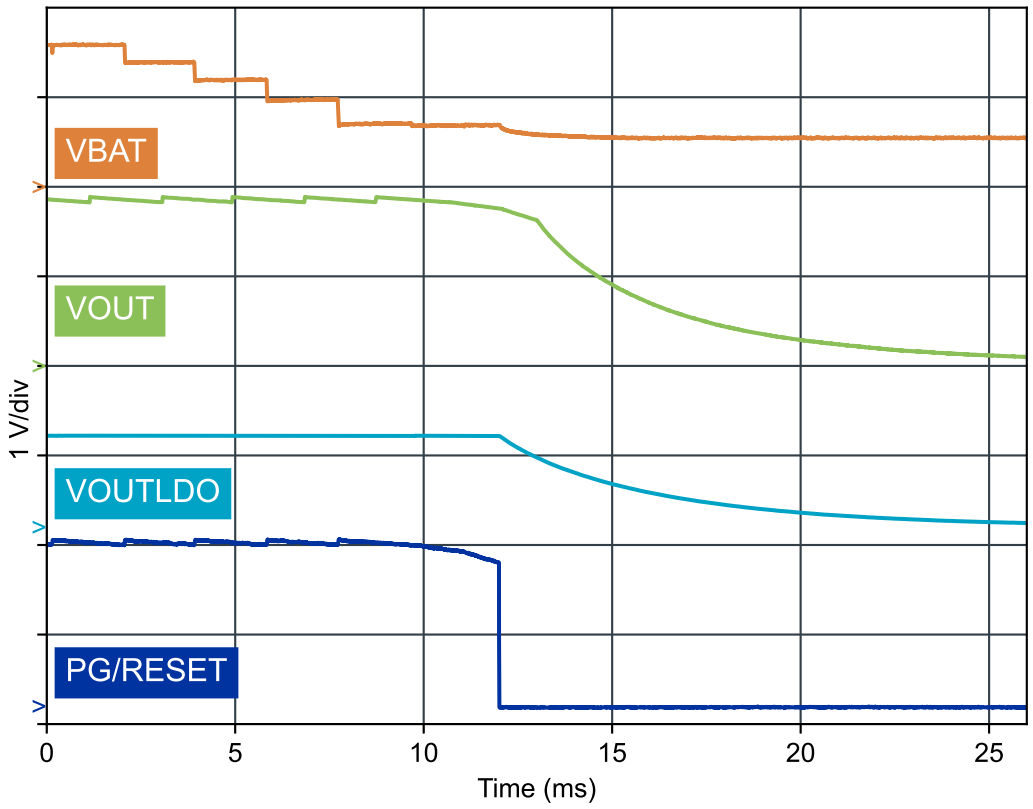


Figure 27: Battery removal, VOUT=1.8 V

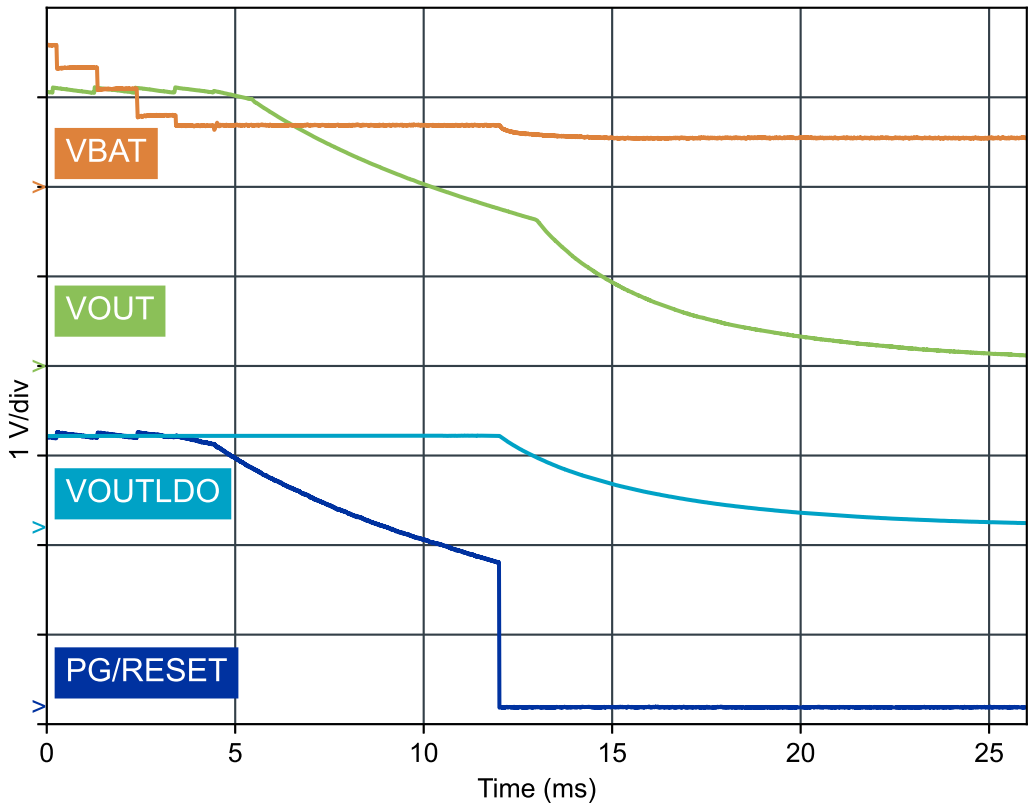


Figure 28: Battery removal, VOUT=3.0 V

6.1.6 Registers

Instances

Instance	Base address	Description
BOOST	0x00000000	BOOST Registers

Register overview

Register	Offset	Description
TASKS_START	0x20	Start tasks
VOUT	0x22	Output voltage setting
VOUTSEL	0x23	Output voltage set by pin or register
OPER	0x24	Operating mode selection
COUNT	0x25	Coil current pulse counter result in DPS mode
LIMIT	0x26	Coil current pulse limiter setting in DPS mode
DPS	0x27	Duration of DPS mode
GPIO	0x28	GPIO and polarity selection for BOOST control
PIN	0x29	GPIO usage for BOOST control
CTRLSET	0x2A	Enable VOUTMIN, VOUTWRN, VOUTDPS, OCP and VBATMINSEL
CTRLCLR	0x2B	Disable VOUTMIN, VOUTWRN, VOUTDPS, OCP and VBATMINSEL
IBATLIM	0x2D	Battery current limit setting
VBATMINLHSEL	0x2E	Enable register control for VBATMINL and VBATMINH comparator thresholds
VBATMINL	0x2F	Battery voltage threshold setting for VBATMINL
VBATMINH	0x30	Battery voltage threshold setting for VBATMINH
VOUTMIN	0x31	Output voltage threshold setting for VOUTMIN
VOUTWRN	0x32	Output voltage threshold setting for VOUTWRN
VOUTDPS	0x33	Output voltage threshold setting for VOUTDPS
STATUS0	0x34	Read operating mode
STATUS1	0x35	Status of output voltage

6.1.6.1 TASKS_START

Address offset: 0x20

Start tasks

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	PULSECNT			Start coil current pulse counter for DPS mode								
			NoEffect	0	No effect								
			Trigger	1	Start counter								
B	W	DPSDUR			Start DPS mode duration measurement								
			NoEffect	0	No effect								
			Trigger	1	Start measurement								

6.1.6.2 VOUT

Address offset: 0x22

Output voltage setting

Bit number					7	6	5	4	3	2	1	0
ID								A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LVL			Output voltage setting (VOUT=1.8V+LVL*0.05V, legal range: 0-30)							
			1V8	0	1.8 V (default)							
			3V3	30	3.3 V							

6.1.6.3 VOUTSEL

Address offset: 0x23

Output voltage set by pin or register

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	PINREG			Output voltage set by pin VSET or register BOOST.VOUT							
			Pin	0	VOUT level is set by VSET pin							
			Register	1	VOUT is set by register BOOST.VOUT							

6.1.6.4 OPER

Address offset: 0x24

Operating mode selection

Bit number					7	6	5	4	3	2	1	0
ID						C	C	B	B	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	MODE			Set BOOST operating mode							
			Auto	0	Auto (HP/LP/ULP/PT) mode							
			HP	1	Forced High Power (HP) mode							
			LP	2	Forced Low Power (LP) mode							
			PT	3	Forced Pass-through (PT) mode							
			NOHP	4	Forced Prevent High Power mode							
B	RW	DPS			DPS mode control							
			Disable	0	DPS operation not allowed							
			ALLOW	1	Allow DPS mode (MODE must be set to '4' or '2')							
			ALLOWLP	2	Allow DPS mode only in LP mode (MODE must be set to '4' or '2')							
C	RW	DPSTIMER			Periodic timer setting for DPS mode							
			100us	0	100 us (default)							
			200us	1	200 us							
			400us	2	400 us							
			800us	3	800 us							

6.1.6.5 COUNT

Address offset: 0x25

Coil current pulse counter result in DPS mode

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	PULSES			Number of counted coil current pulses per re-fresh period in DPS mode (pcs)							

6.1.6.6 LIMIT

Address offset: 0x26

Coil current pulse limiter setting in DPS mode

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	PULSES			Limit setting for coil current pulses per re-fresh period in DPS mode.							
			NoLimit	0	Coil current pulse count not limited							
			Sel3	3	3 pulses (min. value)							
			Sel4	4	4 pulses							
			Sel255	255	255 pulses							

6.1.6.7 DPS

Address offset: 0x27

Duration of DPS mode

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	DURATION			Duration of DPS mode (ms)							

6.1.6.8 GPIO

Address offset: 0x28

GPIO and polarity selection for BOOST control

Bit number					7	6	5	4	3	2	1	0
ID										A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	POL			One GPIO can be selected to control BOOST. Polarity can be active low or high.							
			None	0	No GPIO controls BOOST							
			GPIO0LO	1	GPIO0 in use, active low							
			GPIO0HI	2	GPIO0 in use, active high							
			GPIO1LO	3	GPIO1 in use, active low							
			GPIO1HI	4	GPIO1 in use, active high							
			GPIO2LO	5	Reserved (GPIO2 in use, active low)							
			GPIO2HI	6	Reserved (GPIO2 in use, active high)							

6.1.6.9 PIN

Address offset: 0x29

GPIO usage for BOOST control

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	FORCE			Operating mode setting when GPIO is used to control BOOST. Active GPIO selects the mode from this register. When GPIO is inactive, operating mode is defined by register BOOST.OPER.								
			HP	0	Active GPIO forces High Power (HP) mode								
			LP	1	Active GPIO forces Low Power (LP) mode								
			PT	2	Active GPIO forces Pass-through (PT) mode								
			NOHP	3	Active GPIO forces Prevent HP mode								

6.1.6.10 CTRLSET

Address offset: 0x2A

Enable VOUTMIN, VOUTWRN, VOUTDPS, OCP and VBATMINSEL

Bit number						7	6	5	4	3	2	1	0
ID									E	D	C	B	A
Reset 0x08						**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1S	VOUTMIN			Enable output voltage comparator VOUTMIN								
			NoEffect	0	No effect								
			Enable	1	Enable								
B	RW W1S	VOUTWRN			Enable output voltage comparator VOUTWRN								
			NoEffect	0	No effect								
			Enable	1	Enable								
C	RW W1S	VOUTDPS			Enable output voltage comparator VOUTDPS								
			NoEffect	0	No effect								
			Enable	1	Enable								
D	RW W1S	OCP			Enable overcurrent protection (OCP) for Pass-through mode								
			NoEffect	0	No effect								
			Enable	1	Enable								
E	RW W1S	VBATMINSEL			Allow VOUTMIN comparator to control VBATMIN L/H selection								
			NoEffect	0	No effect								
			Enable	1	Enable								

6.1.6.11 CTRLCLR

Address offset: 0x2B

Disable VOUTMIN, VOUTWRN, VOUTDPS, OCP and VBATMINSEL

Bit number						7	6	5	4	3	2	1	0
ID									E	D	C	B	A
Reset 0x08						**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1C	VOUTMIN			Disable output voltage comparator VOUTMIN								
			NoEffect	0	No effect								
			Disable	1	Disable								
B	RW W1C	VOUTWRN			Disable output voltage comparator VOUTWRN								
			NoEffect	0	No effect								
			Disable	1	Disable								
C	RW W1C	VOUTDPS			Disable output voltage comparator VOUTDPS								
			NoEffect	0	No effect								
			Disable	1	Disable								
D	RW W1C	OCP			Disable overcurrent protection (OCP) for Pass-through mode								
			NoEffect	0	No effect								
			Disable	1	Disable								
E	RW W1C	VBATMINSEL			Do not allow VOUTMIN comparator to control VBATMIN L/H selection								
			NoEffect	0	No effect								
			Disable	1	Disable								

6.1.6.12 IBATLIM

Address offset: 0x2D

Battery current limit setting

Bit number						7	6	5	4	3	2	1	0
ID											A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LVL			Battery (valley) current limit setting								
			600MA	0	600 mA (default)								
			100MA	1	100 mA								
			200MA	2	200 mA								
			300MA	3	300 mA								
			400MA	4	400 mA								
			500MA	5	500 mA								
			700MA	6	700 mA								
			800MA	7	800 mA								

6.1.6.13 VBATMINLHSEL

Address offset: 0x2E

Enable register control for VBATMINL and VBATMINH comparator thresholds

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VBATMINLSEL			Enable register control for VBATMINL threshold setting							
			Disable	0	Default value is used							
			Enable	1	Value is set by register VBATMINL							
B	RW	VBATMINHSEL			Enable register control for VBATMINH threshold setting							
			Disable	0	Default value is used							
			Enable	1	Value is set by register VBATMINH							

6.1.6.14 VBATMINL

Address offset: 0x2F

Battery voltage threshold setting for VBATMINL

Bit number					7	6	5	4	3	2	1	0
ID							A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LVL			VBATMINL comparator threshold setting (VBATMINL=0.65V+LVL*0.05V, legal range: 0-50)							
			0V65	0	0.65 V (default)							
			3V15	50	3.15 V							

6.1.6.15 VBATMINH

Address offset: 0x30

Battery voltage threshold setting for VBATMINH

Bit number					7	6	5	4	3	2	1	0
ID							A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LVL			VBATMINH comparator threshold setting (VBATMINH=0.65V+LVL*0.05V, legal range: 0-50)							
			0V65	0	0.65 V (default)							
			3V15	50	3.15 V							

6.1.6.16 VOUTMIN

Address offset: 0x31

Output voltage threshold setting for VOUTMIN

Bit number					7	6	5	4	3	2	1	0
ID								A	A	A	A	A
Reset 0x0A					**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LVL			VOUTMIN comparator threshold setting (VOUTMIN=1.7V+LVL*0.05V, legal range: 0-31)							
			1V70	0	1.70 V							
			2V20	10	2.20 V (default)							
			3V25	31	3.25 V							

6.1.6.17 VOUTWRN

Address offset: 0x32

Output voltage threshold setting for VOUTWRN

Bit number					7	6	5	4	3	2	1	0
ID								A	A	A	A	A
Reset 0x0C					**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LVL			VOUTWRN comparator threshold setting (VOUTWRN=1.7V+LVL*0.05V, legal range: 0-31)							
			1V70	0	1.70 V							
			2V30	12	2.30 V (default)							
			3V25	31	3.25 V							

6.1.6.18 VOUTDPS

Address offset: 0x33

Output voltage threshold setting for VOUTDPS

Bit number					7	6	5	4	3	2	1	0
ID								A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LVL			VOUTDPS comparator threshold setting (VOUTDPS=1.9V+LVL*0.05V, legal range: 0-31)							
			1V9	0	1.9 V (default)							
			3V45	31	3.45 V							

6.1.6.19 STATUS0

Address offset: 0x34

Read operating mode

Bit number						7	6	5	4	3	2	1	0
ID											A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	MODE			Read BOOST operating mode								
			HP	0	High Power (HP) mode								
			LP	1	Low Power (LP) mode								
			ULP	2	Ultra-Low Power (ULP) mode								
			PT	3	Pass-through (PT) mode								
			DPS	4	Dynamic Power Smoothing (DPS) mode								

6.1.6.20 STATUS1

Address offset: 0x35

Status of output voltage

Bit number						7	6	5	4	3	2	1	0
ID							G	F	E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	VOUTMIN			Output voltage vs. VOUTMIN								
			NotActive	0	VOUT above VOUTMIN threshold								
			Active	1	VOUT below VOUTMIN threshold								
B	R	VOUTWRN			Output voltage vs. VOUTWRN								
			NotActive	0	VOUT above VOUTWRN threshold								
			Active	1	VOUT below VOUTWRN threshold								
C	R	VOUTDPS			Output voltage vs. VOUTDPS								
			NotActive	0	VOUT above VOUTDPS threshold								
			Active	1	VOUT below VOUTDPS threshold								
D	R	VOUTLVL			Output voltage vs. target								
			UnderVolt	0	VOUT is below target level								
			AtTarget	1	VOUT at target level								
E	R	CNTRDY			Coil current pulse count valid (for DPS mode)								
			NotReady	0	Coil current pulse count not available								
			Ready	1	Coil current pulse counter result ready								
F	R	DURRDY			DPS mode duration result valid								
			NotReady	0	DPS mode duration result not available								
			Ready	1	DPS mode duration result ready								
G	R	VSETCAPTURED			Captured value of VSET pin								
			GND	0	Grounded (low)								
			NC	1	Not connected (high)								

6.2 LDOSW – Linear voltage regulator/load switch

The linear voltage regulator/load switch (LDOSW) can be used as a switch or LDO regulator both in Active and Hibernate modes.

LDOSW is supplied from BOOST output (VINT). LDO or load switch must be selected prior to enabling LDOSW in register LDOSW.SEL. The mode can also be controlled through a GPIO by selecting **`PINCTRL`** in register LDOSW.SEL and configuring register LDOSW.GPIO.

The power modes for LDOSW are configured in register LDOSW.SEL and consist of the following:

- Auto – This is the default mode where the device operating mode determines the LDOSW mode. When the device is in Active mode, LDOSW is in High Power mode. When the device is in Hibernate mode, LDOSW is in Ultra-Low Power mode.
- High Power – Output current up to 50 mA.
- Ultra-Low Power – Output current up to 2 mA.

Overcurrent protection is enabled by default. It can be disabled in register CONF. The current limits for soft start and overcurrent protection can be configured in register PRGOCP. The **LSOUT/VOUTLDO** pin is actively discharged when LDOSW is disabled.

Note: GPIO controls must be disabled before entering Hibernate or Hibernate_PT mode.

LDO mode

The LDO is OFF by default. LDO mode is set by selecting **LDO** in register LDOSW.SEL. The output voltage is configurable in 50 mV steps in register LDOSW.VOUT and enabled in register LDOSW.LDOSW.

Load switch

The load switch is OFF by default. Load switch mode is set by selecting **LoadSW** in register LDOSW.SEL and enabled in register LDOSW.LDOSW.

6.2.1 LDO electrical specification

Electrical parameters have been measured using a 2.2 µF output capacitor. T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
$VLDOSW_{PROG}$	Output voltage range		0.8 to 3		V
$VLDOSW_{STEP}$	Output voltage step (register setting)		50		mV
$VLDOSW_{ACC}$	Output voltage accuracy, High Power mode excluding transients	-3		3	%
$VLDOSW_{DROPHP}$	Drop-out voltage, High Power mode (VLDOSW=1.8 V)		300		mV
$VLDOSW_{DROPLP}$	Drop-out voltage, Ultra-Low Power mode (VLDOSW=1.8 V)		400		mV
$IVLDOSW_{LDO}$	Output current, High Power mode			50	mA
$IVLDOSW_{LDO\_ULP}$	Output current, Ultra-Low Power mode (drop-out voltage=600 mV)			2	mA
$IQ_{LDOSW\_LDO\_HPLP}$	Quiescent current, High Power mode (no load, BOOST in Low Power/Ultra-Low Power mode, VBAT=1.5 V) - additional to chip's consumption		1900		µA
$IQ_{LDOSW\_LDO\_HP}$	Quiescent current, High Power mode (no load, BOOST in High Power mode, VBAT=1.5 V) - additional to chip's consumption		60		µA
$IQ_{LDOSW\_LDO\_ULP}$	Quiescent current, Ultra-Low Power mode (no load, BOOST in Ultra-Low Power mode, VBAT=1.5 V) - additional to chip's consumption		0.6		µA
$VLDOSW_{LDTR}$	Load transient (1 mA to 40 mA in 10 µs), High Power mode		50		mV
$VLDOSW_{LNTR}$	Line transient (300 mV in 10 µs), both modes		25		mV
$VLDOSW_{PSRR}$	Power supply rejection ratio, High Power mode (1 Hz to 10 kHz)		30		dB
C_{LDOSW_LDO}	Effective capacitance on LSOUT/ VOUTLDO pin	0.7		12	µF
$VLDOSW_{PD}$	Pull-down resistor		2		kΩ

Table 11: LDO electrical specification

6.2.2 Load switch electrical specification

T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
RON_{LDOSW_SW}	RON, High Power mode (1.8 V, OCP disabled)		500		mΩ
$RON_{LDOSW\_SW\_ULP}$	RON, Ultra-Low Power mode		40		Ω
$ILDOSW_{SW}$	Output current, High Power mode			50	mA
$ILDOSW_{SW\_ULP}$	Output current, Ultra-Low Power mode			2	mA
$IQ_{LDOSW\_SW\_HPLP}$	Quiescent current, High Power mode (no load, BOOST in Low Power/Ultra-Low Power mode, VBAT=1.5 V) - additional to chip's consumption		1800		µA
$IQ_{LDOSW\_SW\_HP}$	Quiescent current, High Power mode (no load, BOOST in High Power mode, VBAT=1.5 V) - additional to chip's consumption		50		µA
$IQ_{LDOSW\_SW\_ULP}$	Quiescent current, Ultra-Low Power mode (no load, BOOST in Ultra-Low Power mode, VBAT=1.5 V) - additional to chip's consumption		20		nA
$VLDOSW_{PD}$	Pull-down resistor		2		kΩ

Table 12: Load switch electrical specification

6.2.3 Electrical characteristics

The following graphs show typical electrical characteristics for LDO and Load switch. They have been measured using a 2.2 µF output capacitor, unless mentioned otherwise.

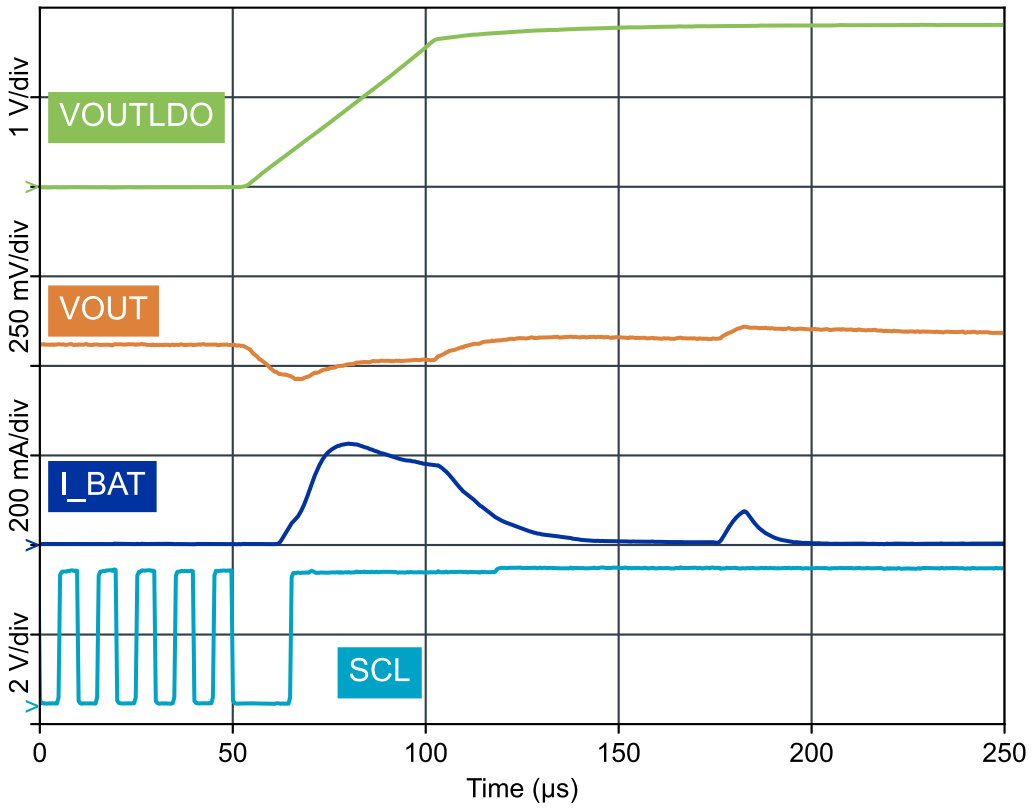


Figure 29: LDO start-up, VOUTLDO=1.8 V

The following two figures show load regulation in various modes for VOUTLDO=1.8 V.

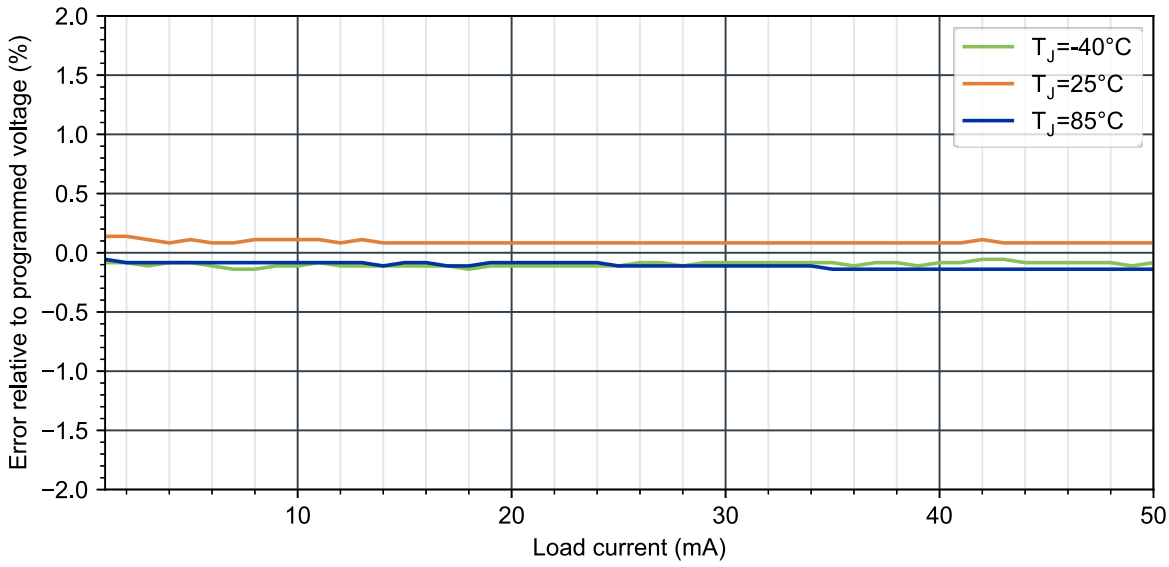


Figure 30: LDO load regulation in High Power mode

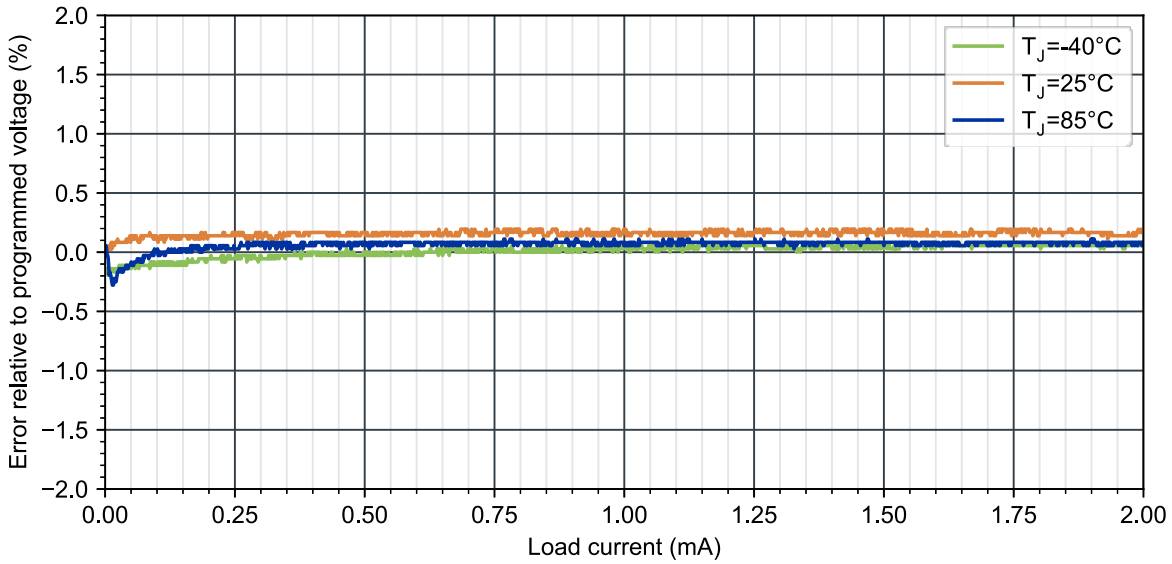


Figure 31: LDO load regulation in Ultra-Low Power mode

The following two figures show accuracy over temperature in various modes.

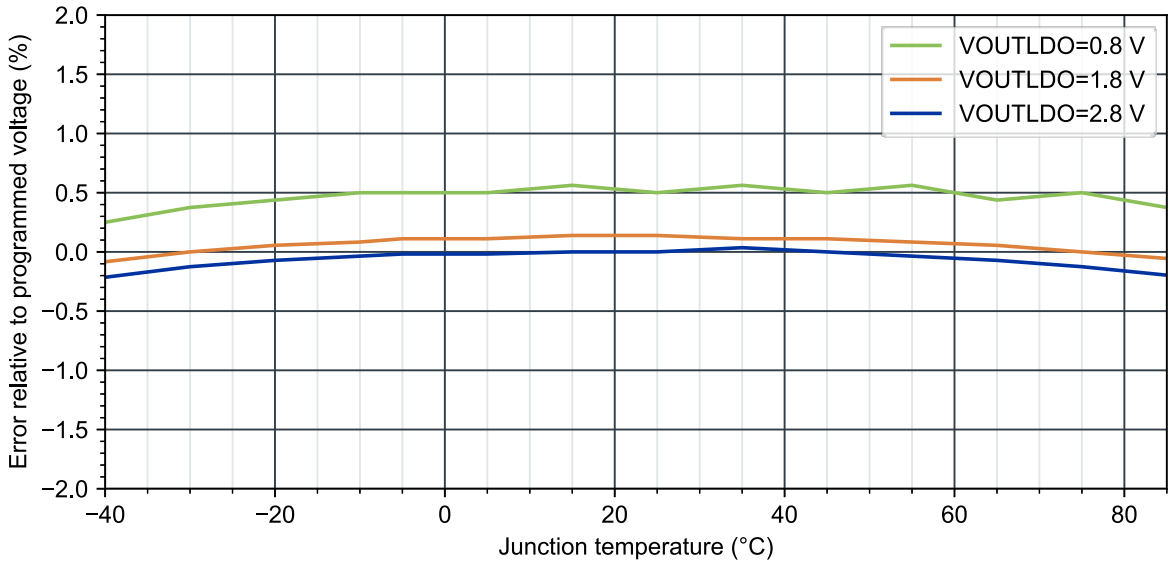


Figure 32: LDO accuracy, High Power mode (load=1 mA)

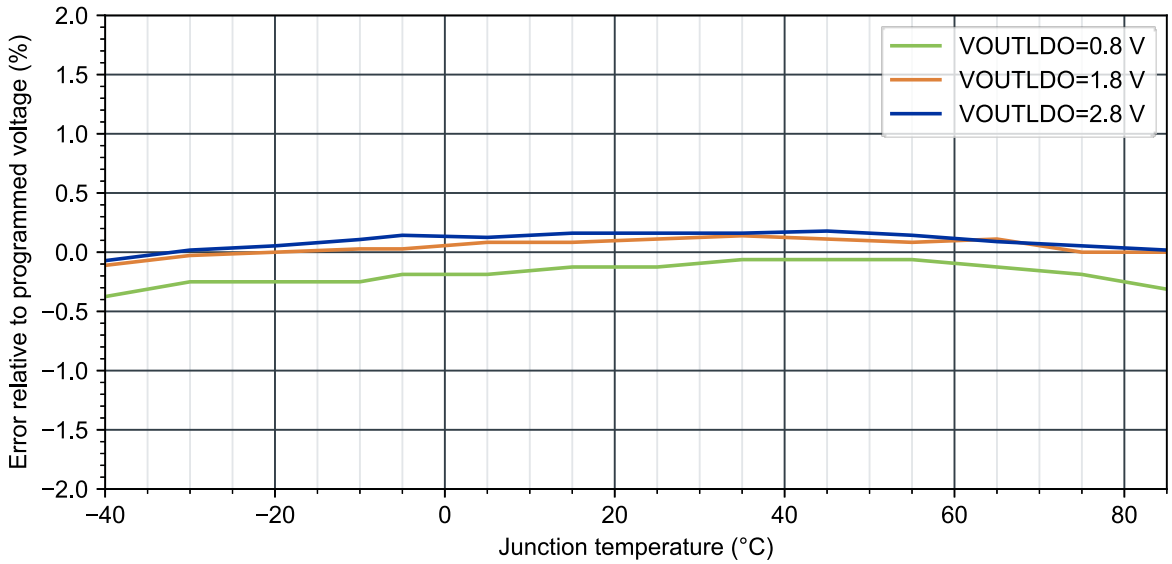


Figure 33: LDO accuracy, Ultra-Low Power mode (load=0.1 mA)

The following two figures show load transient in High Power mode for various output voltages. Load changes from 1 mA to 40 mA in 10 µs.

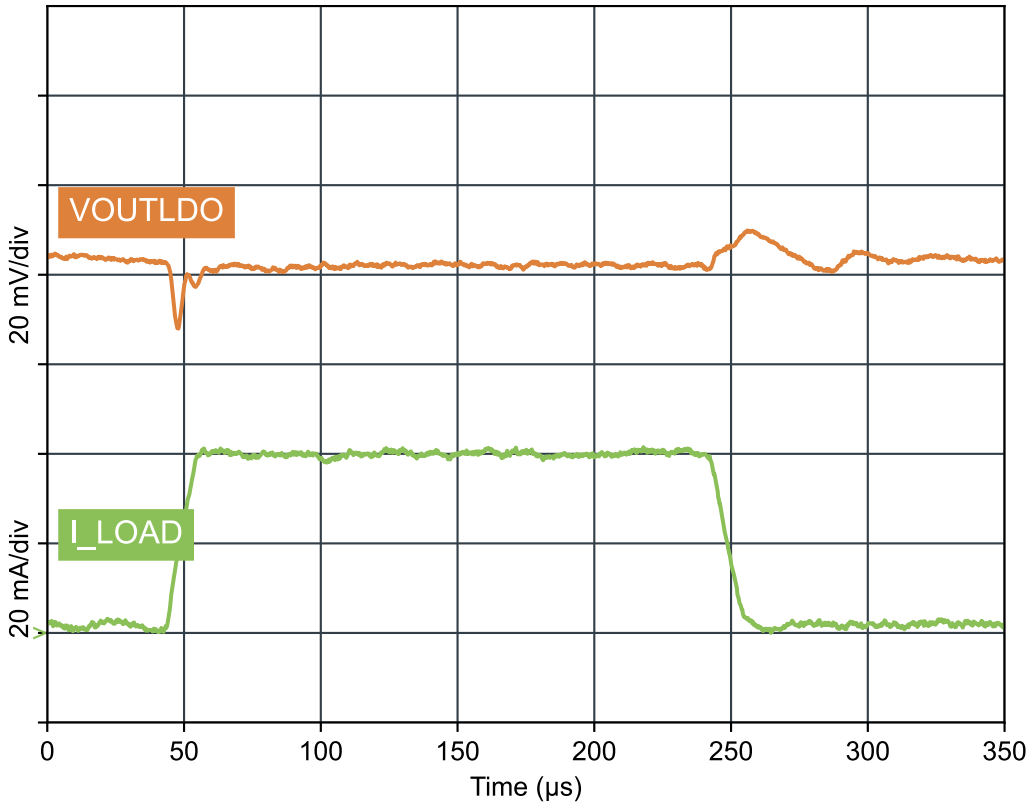


Figure 34: LDO load transient, VOUTLDO=1.0 V (VINT=1.8 V)

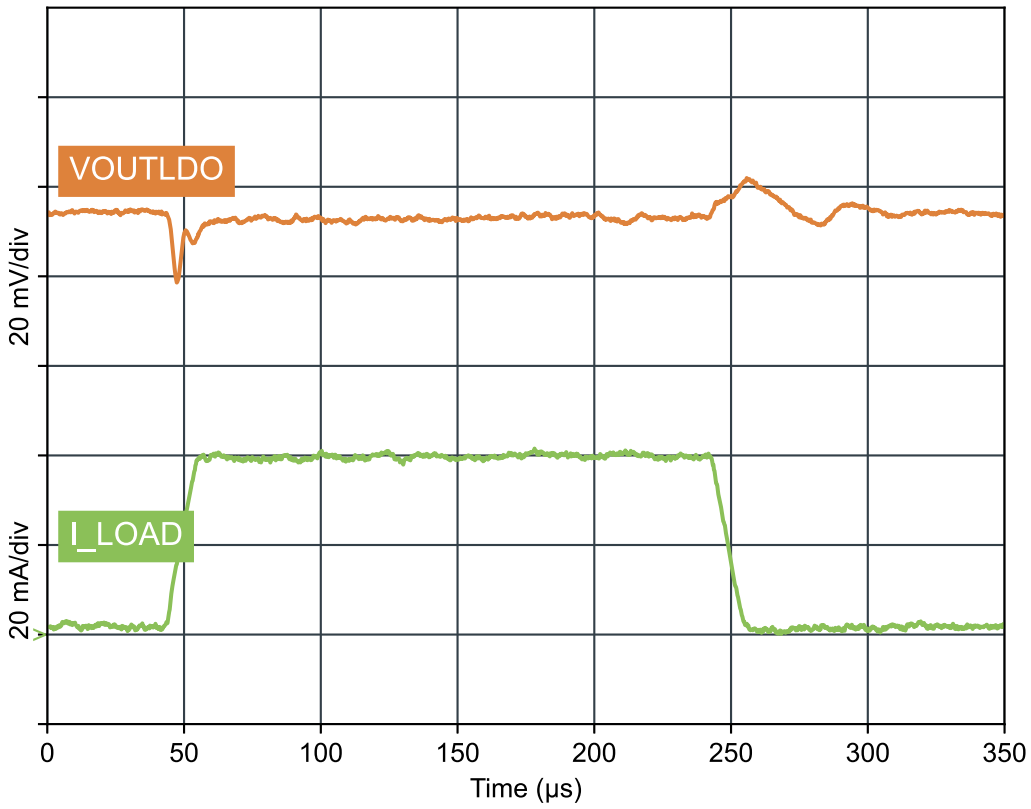


Figure 35: LDO load transient, VOUTLDO=1.8 V (VINT=3.0 V)

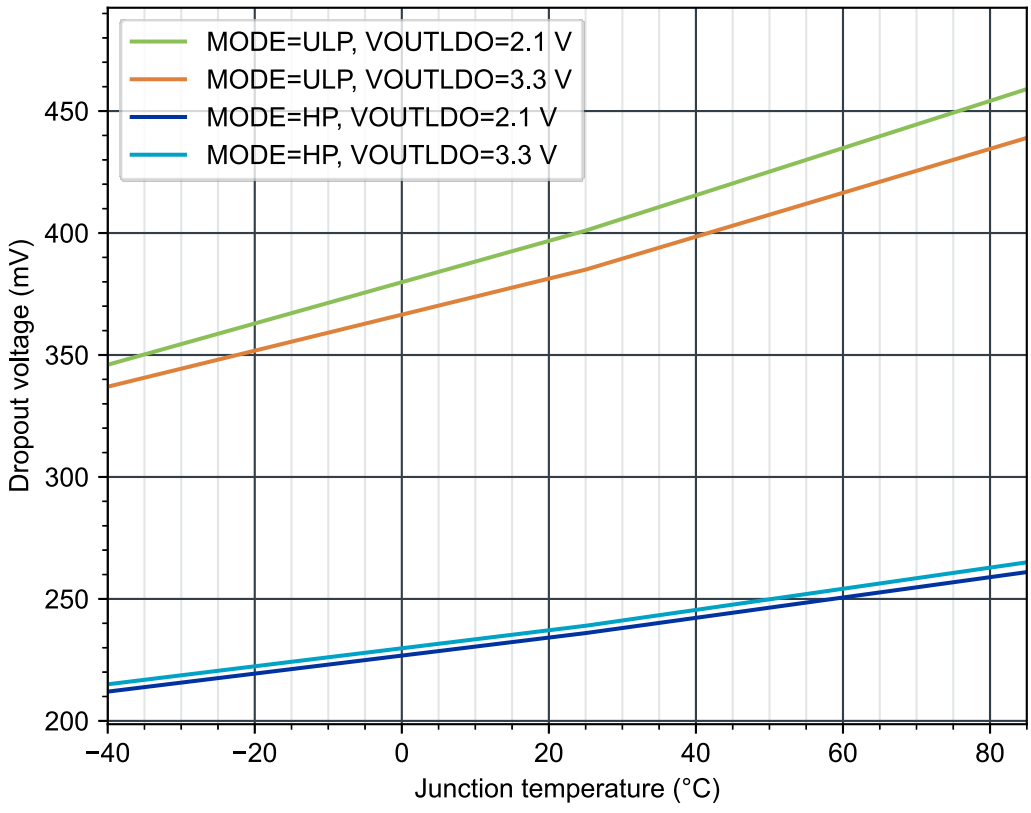


Figure 36: LDO drop-out voltage vs. temperature

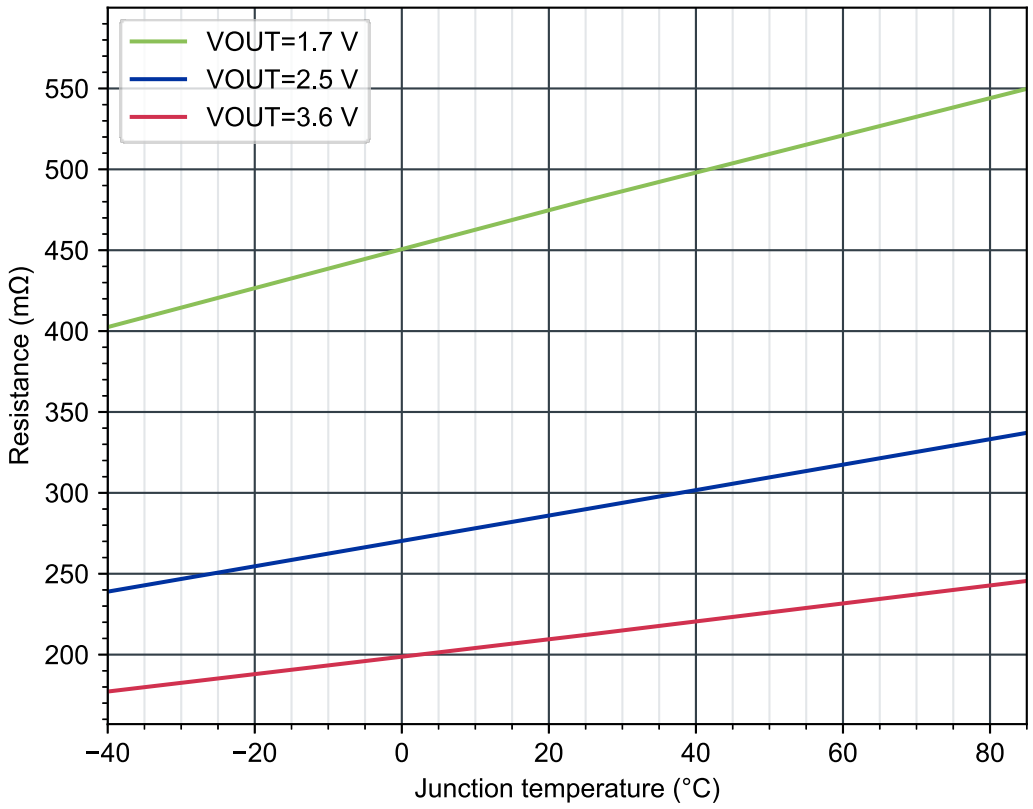


Figure 37: Load switch resistance vs. temperature (OCP disabled)

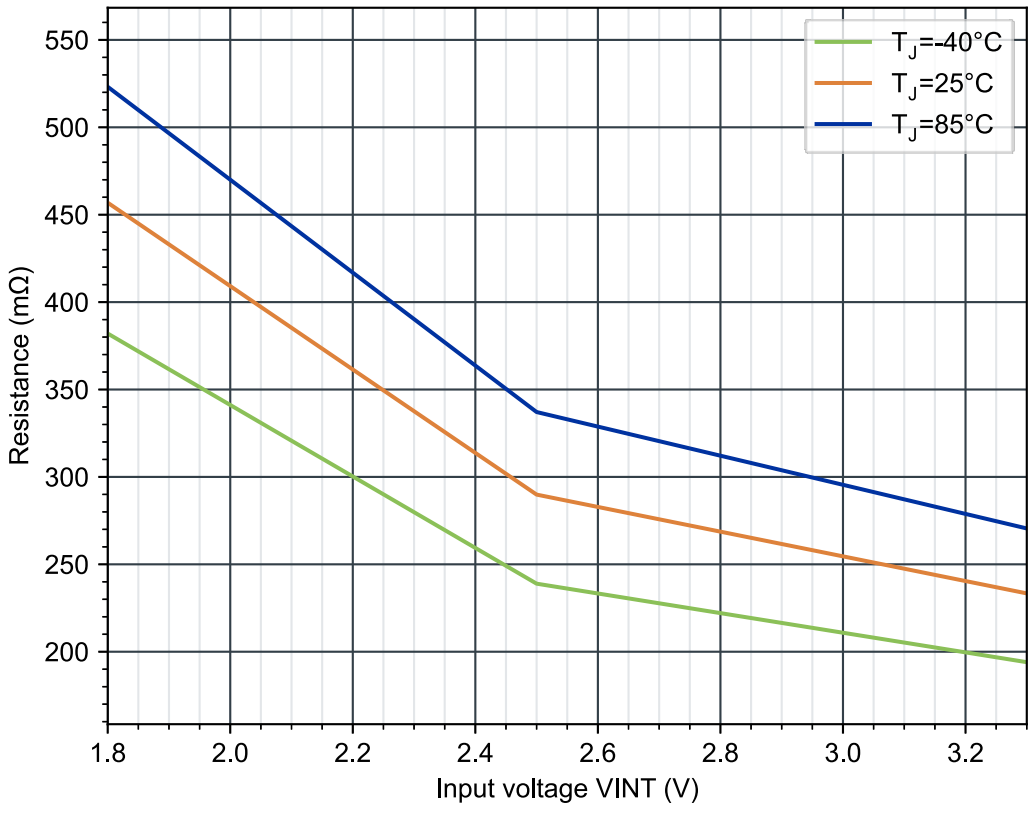


Figure 38: Load switch resistance vs. input voltage (OCP disabled)

6.2.4 Registers

Instances

Instance	Base address	Description
LDOSW	0x00000000	LDOSW Registers

Register overview

Register	Offset	Description
VOUT	0x68	Output voltage setting for LDO mode
LDOSW	0x69	Enable
SEL	0x6A	LDO or Load switch mode and operating mode selection
GPIO	0x6B	GPIO polarity and pin select and configuration when GPIO control in use
CONF	0x6C	Overcurrent protection (OCP)
RAMP	0x6D	Output voltage ramping configuration (LDO mode)
STATUS	0x6E	Read operating mode
PRGOCP	0x6F	Select OCP and soft start current limits

6.2.4.1 VOUT

Address offset: 0x68

Output voltage setting for LDO mode

Bit number						7	6	5	4	3	2	1	0
ID								A	A	A	A	A	A
Reset 0x08						**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LVL			Output voltage setting for LDO mode (VOUTLDO=0.4+LVL*0.05, legal range: 8-52)								
			0V8	8	0.8 V (default)								
			3V0	52	3.0 V								

6.2.4.2 LDOSW

Address offset: 0x69

Enable

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	ENABLE			Enable (both for LDO and Load switch modes)								
			OFF	0	LDOSW disabled								
			ON	1	LDOSW enabled								

6.2.4.3 SEL

Address offset: 0x6A

LDO or Load switch mode and operating mode selection

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	MODE			Select LDO or Load switch mode. (Needs to be selected before enabling the LDO or Load switch)								
			LDO	0	LDO mode								
			LoadSW	1	Load switch mode								
B	RW	OPER			Select operating mode (for both LDO and Load switch modes)								
			Auto	0	Auto (HP in Active mode/ULP in Hibernate mode) mode								
			ULP	1	Forced Ultra-Low Power mode								
			HP	2	Forced High Power mode								
			PINCTRL	3	GPIO controlled								

6.2.4.4 GPIO

Address offset: 0x6B

GPIO polarity and pin select and configuration when GPIO control in use

Bit number						7	6	5	4	3	2	1	0
ID									D	C	B	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	POL			Select polarity for the GPIO								
			ActiveLo	0	Active low								
			ActiveHi	1	Active high								
B	RW	PIN			Select which GPIO controls LDO or Load switch								
			GPIO0	0	GPIO0 in use								
			GPIO1	1	GPIO1 in use								
			GPIO2	2	Reserved (GPIO2 in use)								
			GPIO22	3	Reserved (GPIO2 in use)								
C	RW	PINACT			Mode selected, when GPIO active								
			ONHP	0	ON, HP mode								
			ONULP	1	ON, ULP mode								
D	RW	PININACT			Mode selected, when GPIO inactive								
			OFF	0	OFF								
			ONULP	1	ON, ULP mode								

6.2.4.5 CONF

Address offset: 0x6C

Overcurrent protection (OCP)

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	OCP			Enable OCP (before enabling LDO or Load switch)								
			Disable	0	OCP disable								
			Enable	1	OCP enable								

6.2.4.6 RAMP

Address offset: 0x6D

Output voltage ramping configuration (LDO mode)

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	USE			Use output voltage ramping (stepping)							
			NOTUSE	0	No ramping							
			USE	1	VOUTLDO ramps up step-by-step							
B	RW	HALT			Halt output voltage ramping in case VINT droops							
			NOTHALT	0	Ignore VINT droop and continue VOUTLDO ramping							
			HALT	1	Halt VOUTLDO ramping in case of VINT droop							

6.2.4.7 STATUS

Address offset: 0x6E

Read operating mode

Bit number					7	6	5	4	3	2	1	0
ID								E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	LDO			LDO mode							
			NTH	0	Non-LDO mode (load switch mode, disabled or powering up)							
			LDO	1	LDO mode							
B	R	SW			Load switch mode							
			NTH	0	Non-Load switch mode (LDO mode, disabled or powering up)							
			LOADSW	1	Load switch mode							
C	R	HP			HP operating mode							
			NTH	0	Non-HP mode							
			HP	1	HP mode							
D	R	ULP			ULP operating mode							
			NTH	0	Non-ULP mode							
			ULP	1	ULP mode							
E	R	OCP			Overcurrent							
			NONE	0	No overcurrent detected							
			ACTIVE	1	Overcurrent detected							

6.2.4.8 PRGOCP

Address offset: 0x6F

Select OCP and soft start current limits

Bit number					7	6	5	4	3	2	1	0
ID					B	B	B	B	A	A	A	A
Reset 0x84					**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	LDO			Select OCP and soft start current limits for LDO operating mode (valid in HP mode)							

Bit number						7	6	5	4	3	2	1	0
ID						B	B	B	B	A	A	A	A
Reset 0x84						**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			DNU	0	Do not use								
			150mA	1	150 mA								
			75mA	4	75 mA (default)								
			50mA	6	50 mA								
			38mA	7	38 mA								
			25mA	13	25 mA								
B	RW	LOADSW			Select OCP and soft start current limits for Load switch operating mode (valid in HP mode)								
			DNU	0	Do not use								
			40mA	1	40 mA								
			70mA	7	70 mA								
			75mA	8	75 mA (default)								
			80mA	9	80 mA								
			110mA	15	110 mA								

6.3 GPIO – General purpose input/output

The general purpose input/output pins, **GPIO0** and **GPIO1**, are set as input with weak pull-down by default.

GPIO has the following configurable features:

- General purpose input
- Control input for BOOST and LDOSW
- Output
- Interrupt

Debouncing, pull-up and pull-down resistors, and variable drive strength are available through register configuration.

6.3.1 Pin configuration

The GPIO peripheral implements two pins, **GPIO0** and **GPIO1**. Both pins can be individually configured in the CONFIG[n], USAGE[n], and OUTPUT[n] registers.

Note: GPIO pins cannot be used while in Hibernate, Hibernate_PT, or Ship mode.

General purpose input

GPIO can be used as a general purpose input to monitor the input logic level. For a pin to function as a GPIO, select **GPIO** in register USAGE[n]. Input buffer enable, debounce, pull-down, and pull-up are set in the CONFIG[n] register. Pin state can be read in the READ register.

GPIO can also be used as an input to trigger an event using INTEN_GPIO_SET to enable events. Set bit GPIO[n]RISE to generate an event on the rising edge. To generate an event on a falling edge, set bit GPIO[n]FALL. The events are visible in register EVENTS_GPIO_SET.

Control input

For a pin to function as a control input, first select **GPIO** in USAGE[n], then configure the pin in CONFIG[n].

The following components can be controlled through GPIO once enabled in the corresponding register.

- LDOSW – Registers LDOSW.GPIO and LDOSW.SEL (select **PINCTRL**)
- BOOST – Registers BOOST.PIN and BOOST.GPIO

Output

For a pin to function as an output, select **GPIO** in the USAGE[n] register. Use the CONFIG[n] register to enable the output buffer and configure the settings. OUTPUT[n] drives the pin to the desired state.

Note: In case of a power cycle, the GPIOs are reset and return to their default state (input, pull-down) once delay t_{PWRDN} has completely elapsed. The GPIOs are internally supplied by VINT. In case a GPIO pin is configured as a push-pull (a.k.a. CMOS) output and connected to the host MCU, backfeeding of power to host's supply rail (VOUT) might take place during the mentioned delay. As a consequence VOUT might not drop down enough to reset the host. The issue can be avoided by using open-drain instead of push-pull operation for such signals.

Interrupt output

A pin is set as an interrupt output by selecting **INTHI** or **INTLO** (active high or low, respectively) in the USAGE[n] register. The CONFIG[n] register is used to enable the output buffer and configure the settings.

GPIO can be used as an interrupt by setting one or more from the following registers:

- INTEN_SYSTEM_SET
- INTEN_ADC_SET
- INTEN_GPIO_SET
- INTEN_BOOST_SET
- INTEN_LDOSW_SET

6.3.2 Electrical specification

T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	0.7 x VOUT		VOUT	V
V_{IL}	Input low voltage	VSS		0.3 x VOUT	V
V_{OH}	Output high voltage	0.75 x VOUT		VOUT	V
V_{OL}	Output low voltage	VSS		0.25 x VOUT	V
PU_{GPIO}	Pull-up resistor		50		kΩ
PD_{GPIO}	Pull-down resistor		500		kΩ
I_{DRIVE_LO}	Drive strength, weak		2		mA
I_{DRIVE_HI}	Drive strength, strong		4		mA
t_{DEB_GPIO}	Input debounce		10		ms

Table 13: GPIO electrical specification

6.3.3 Registers

Instances

Instance	Base address	Description
GPIO	0x00000000	GPIO Registers

Register overview

Register	Offset	Description
CONFIG0	0x80	GPIO0 configuration
CONFIG1	0x81	GPIO1 configuration
USAGE0	0x83	GPIO0 usage
USAGE1	0x84	GPIO1 usage
OUTPUT0	0x86	GPIO0 output value set
OUTPUT1	0x87	GPIO1 output value set
READ	0x89	GPIO pin states

6.3.3.1 CONFIG0

Address offset: 0x80

GPIO0 configuration

Bit number								7	6	5	4	3	2	1	0
ID									G	F	E	D	C	B	A
Reset 0x09								**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**
ID	R/W	Field		Value ID		Value		Description							
A	RW	INPUT						Enable input buffer							
				DISABLE		0		Disable input buffer							

Bit number					7	6	5	4	3	2	1	0
ID						G	F	E	D	C	B	A
Reset 0x09					**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description							
			ENABLE	1	Enable input buffer							
B	RW	OUTPUT			Enable output buffer							
			DISABLE	0	Disable output buffer							
			ENABLE	1	Enable output buffer							
C	RW	OPENDRAIN			Open-drain enable							
			OFF	0	Open-drain disabled							
			ON	1	Open-drain enabled							
D	RW	PULLDOWN			Pull-down enable							
			OFF	0	Pull-down disabled							
			ON	1	Pull-down enabled							
E	RW	PULLUP			Pull-up enable							
			OFF	0	Pull-up disabled							
			ON	1	Pull-up enabled							
F	RW	DRIVE			Drive strength select							
			NORMAL	0	Normal drive strength							
			HIGH	1	High drive strength							
G	RW	DEBOUNCE			Debounce enable							
			OFF	0	Debounce filter disabled							
			ON	1	Debounce filter enabled							

6.3.3.2 CONFIG1

Address offset: 0x81

GPIO1 configuration

Bit number					7	6	5	4	3	2	1	0
ID						G	F	E	D	C	B	A
Reset 0x09					**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description							
A	RW	INPUT			Enable input buffer							
			DISABLE	0	Disable input buffer							
			ENABLE	1	Enable input buffer							
B	RW	OUTPUT			Enable output buffer							
			DISABLE	0	Disable output buffer							
			ENABLE	1	Enable output buffer							
C	RW	OPENDRAIN			Open-drain enable							
			OFF	0	Open-drain disabled							
			ON	1	Open-drain enabled							
D	RW	PULLDOWN			Pull-down enable							
			OFF	0	Pull-down disabled							
			ON	1	Pull-down enabled							
E	RW	PULLUP			Pull-up enable							
			OFF	0	Pull-up disabled							
			ON	1	Pull-up enabled							
F	RW	DRIVE			Drive strength select							
			NORMAL	0	Normal drive strength							
			HIGH	1	High drive strength							
G	RW	DEBOUNCE			Debounce enable							
			OFF	0	Debounce filter disabled							

Bit number					7	6	5	4	3	2	1	0
ID						G	F	E	D	C	B	A
Reset 0x09					**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description							
			ON	1	Debounce filter enabled							

6.3.3.3 USAGE0

Address offset: 0x83

GPIO0 usage

Bit number					7	6	5	4	3	2	1	0
ID											A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	SEL			Select usage							
			GPIO	0	GPIO							
			INTLO	1	Interrupt output, active low							
			INTHI	2	Interrupt output, active high							

6.3.3.4 USAGE1

Address offset: 0x84

GPIO1 usage

Bit number					7	6	5	4	3	2	1	0
ID											A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	SEL			Select usage							
			GPIO	0	GPIO							
			INTLO	1	Interrupt output, active low							
			INTHI	2	Interrupt output, active high							

6.3.3.5 OUTPUT0

Address offset: 0x86

GPIO0 output value set

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	VALUE			GPIO0 output value							
			LOW	0	Pin is driven low							
			HIGH	1	Pin is driven high							

6.3.3.6 OUTPUT1

Address offset: 0x87

GPIO1 output value set

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	VALUE			GPIO1 output value								
			LOW	0	Pin is driven low								
			HIGH	1	Pin is driven high								

6.3.3.7 READ

Address offset: 0x89

GPIO pin states

Bit number						7	6	5	4	3	2	1	0
ID											C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	GPIO0			GPIO0 pin state								
			LOW	0	Pin is low								
			HIGH	1	Pin is high								
B	R	GPIO1			GPIO1 pin state								
			LOW	0	Pin is low								
			HIGH	1	Pin is high								
C	R	GPIO2_RESERVED			GPIO2 pin state (reserved)								
			LOW	0	Pin is low								
			HIGH	1	Pin is high								

7 System features

7.1 System Monitor

The chip has an 8-bit ADC with offset calibration that is used for measuring internal parameters. It can be used in the following measurement modes:

- Single-shot
- Timed
- Averaged

Measurements

- VBAT voltage measurement
- VOUT voltage measurement
- Die temperature measurement (can be used to estimate battery temperature)
- Offset measurement

An interrupt can be configured to trigger once a measurement is complete. ADC status is available in a register ADC.STATUS. One measurement at a time can be done. New conversion can only be started once status indicates that ADC is ready. Separate result registers are available for each mode and for the averaged result.

By default, ADC uses factory offset calibration stored in register ADC.OFFSETFACTORY. ADC offset can be re-calibrated on demand by selecting mode Offset in register ADC.CONFIG followed by a common conversion task in ADC.TASKS_ADC. The new offset value is stored in ADC.OFFSETMEASURED and can be taken into use instead of the factory calibration using register ADC.OFFSETCFG.

Single-shot measurements

Single-shot measurements are triggered by selecting the mode in register ADC.CONFIG followed by a common conversion task in ADC.TASKS_ADC.

Timed measurements

Timed measurements for battery voltage (VBAT) are enabled in registers ADC.CONFIG and ADC.DELAY, and triggered by ADC.TASKS_ADC.

Software can abort a timed VBAT measurement in register ADC.TASKS_ADC to free up ADC for another measurement. Interrupt and conversion results are available for the aborted measurement.

Averaged measurements

Averaged measurements are enabled in registers ADC.CONFIG and triggered by ADC.TASKS_ADC and the results are available in ADC.AVERAGE. Averaging is available for all modes except offset measurement.

Events and interrupts

An event register and interrupt are available for each measurement and are issued once the measurement has been completed. See registers MAIN.EVENTS_ADC_SET, MAIN.EVENTS_ADC_CLR, MAIN.INTEN_ADC_SET and MAIN.INTEN_ADC_CLR.

Measurement results

Results from the ADC are stored in registers according to the following table.

Value	Register
Battery voltage	ADC.READVBAT
VOUT voltage	ADC.READVOUT
Die temperature	ADC.READTEMP
Averaged battery voltage, VOUT, or die temperature	ADC.AVERAGE

Table 14: ADC measurements

VBAT

The equation for (instant and delayed) VBAT is given by the following:

$$V_{\mathrm{BAT}} = \mathrm{ADC.READVBAT} \cdot \frac{3.2}{255}$$

In case averaged measurement mode has been used, ADC.READVBAT needs to be replaced with ADC.AVERAGE in the above equation.

VOUT

The equation for VOUT is given by the following:

$$V_{\mathrm{OUT}} = 1.8 + \mathrm{ADC.READVOUT} \cdot \frac{1.5}{255}$$

In case averaged measurement mode has been used, ADC.READVOUT needs to be replaced with ADC.AVERAGE in the above equation.

Die temperature

The die temperature, T (in °C), is given by the following equation:

$$T = 389.5 - 2.12 \cdot \mathrm{ADC.READTEMP}$$

In case averaged measurement mode has been used, ADC.READTEMP needs to be replaced with ADC.AVERAGE in the above equation.

Die temperature can be used to estimate battery temperature. The self-heating of nPM2100 is negligible in typical Bluetooth Low Energy applications, making die temperature a good approximation of battery temperature.

7.1.1 Electrical specification

T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
t_{CONV}	Conversion time		100		µs
$VBAT_{RANGE}$	VBAT measurement range	0		3.2	V
$VBAT_{ACC}$	VBAT measurement accuracy, 0.7 V<VBAT<3.2 V	-2		2	%
$VBAT_{ACC\_25C}$	VBAT measurement accuracy, 0.7 V<VBAT<3.2 V, T_J=25°C		± 1		%
$VBAT_{DELAY}$	Timed VBAT measurement delay range (4 ms steps)		5 to 1025		ms
$VOUT_{RANGE}$	Measurement range for VOUT	1.8		3.3	V
$DIET_{RANGE}$	Die temperature measurement range	-20		105	°C
$DIET_{ACC}$	Die temperature measurement accuracy, -10°C<T_J<60°C	-8		8	°C
DNL	Differential non-linearity		<0.5		LSB

Table 15: System monitor electrical specification

7.1.2 Registers

Instances

Instance	Base address	Description
ADC	0x00000000	ADC Registers

Register overview

Register	Offset	Description
TASKS_ADC	0x90	Start ADC sampling and conversion process, abort ADC delays
CONFIG	0x91	Select mode, averaging and GPIO control
DELAY	0x92	Delay setting for VBAT measurement
OFFSETCFG	0x93	ADC offset configurations
CTRLSET	0x94	VOUT droop detector and recovery counter
CTRLCLR	0x95	VOUT droop detector and recovery counter
READVBAT	0x96	VBAT conversion result
READTEMP	0x97	Die temperature conversion result
READDROOP	0x98	Droop detection conversion result
READVOUT	0x99	VOUT conversion result
VOUTRECOV	0x9A	VOUT recovery time
AVERAGE	0x9B	Averaged measurement result
BOOST	0x9C	Boost operating mode snapshot (for battery voltage measurement)
STATUS	0x9D	ADC and VOUT droop detector and recovery counter status
OFFSETFACTORY	0x9E	Factory delivered value for offset correction.
OFFSETMEASURED	0x9F	ADC offset calibration result. Can be updated by on-chip offset measurement.

7.1.2.1 TASKS_ADC

Address offset: 0x90

Start ADC sampling and conversion process, abort ADC delays

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	CONV			Start ADC sampling and conversion process								
			NoEffect	0	No effect								
			Trigger	1	Start process								
B	W	ABORTDELAY			Abort the delay for an ongoing delayed VBAT measurement								
			NoEffect	0	No effect								
			Trigger	1	Abort delay and start conversation process								

7.1.2.2 CONFIG

Address offset: 0x91

Select mode, averaging and GPIO control

Bit number						7	6	5	4	3	2	1	0
ID						C	C	B	B	B	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	MODE			Select mode								
			InsVBAT	0	Instant VBAT measurement (READVBAT)								
			DelVBAT	1	Delayed VBAT measurement (READVBAT)								
			DieTemp	2	Die temperature measurement (READTEMP)								
			VOUTDroop	3	VOUT droop measurement (READDROOP)								
			VOUT	4	VOUT measurement (READVOUT)								
			Offset	5	ADC offset measurement (OFFSETMEASURED)								
B	RW	AVG			Averaging configuration								
			Disabled	0	Averaging disabled								
			Avg2	1	Averaging by 2								
			Avg4	2	Averaging by 4								
			Avg8	3	Averaging by 8								
			Avg16	4	Averaging by 16								
C	RW	GPIO			Select GPIO for VOUT droop detection "window" control								
			None	0	No GPIO controls VOUT droop detector								
			GPIO0	1	GPIO0 in use (active high)								
			GPIO1	2	GPIO1 in use (active high)								
			GPIO2	3	Reserved (GPIO2 in use, active high)								

7.1.2.3 DELAY

Address offset: 0x92

Delay setting for VBAT measurement

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	TIME			Delay (ms)=5+TIME*4. Legal range is 0-255 or 5-1025 ms.								

7.1.2.4 OFFSETCFG

Address offset: 0x93

ADC offset configurations

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x01						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	OFFSETEN			Offset correction enable								
			Disabled	0	Offset correction disabled								
			Enabled	1	Offset correction enabled								
B	RW	SELOFFSET			Offset register select								
			OFFSETFACTORY	0	Factory offset register								
			OFFSETMEASURED	1	Measured offset register								

7.1.2.5 CTRLSET

Address offset: 0x94

VOUT droop detector and recovery counter

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1S	DROOPSTART			VOUT droop detector measurement								
			NoEffect	0	No effect								
			Trigger	1	Start VOUT droop detection "window"								
B	RW W1S	RECOVSTART			VOUT droop revovery time counter								
			NoEffect	0	No Effect								
			Trigger	1	Start VOUT droop recovery time counter								

7.1.2.6 CTRLCLR

Address offset: 0x95

VOUT droop detector and recovery counter

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1C	DROOPSTOP			VOUT droop detector measurement								
			NoEffect	0	No effect								
			Trigger	1	End VOUT droop detection "window" (and trigger A/D conversion)								
B	RW W1C	RECOVSTOP			VOUT droop revovery time counter								
			NoEffect	0	No Effect								
			Trigger	1	Stop VOUT droop recovery time counter								

7.1.2.7 READVBAT

Address offset: 0x96

VBAT conversion result

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	RESULT			VBAT conversion result								

7.1.2.8 READTEMP

Address offset: 0x97

Die temperature conversion result

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	RESULT			Die temperature conversion result								

7.1.2.9 READDROOP

Address offset: 0x98

Droop detection conversion result

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	RESULT			VOUT droop minimum level result								

7.1.2.10 READVOUT

Address offset: 0x99

VOUT conversion result

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	RESULT			VOUT level result								

7.1.2.11 VOUTRECOV

Address offset: 0x9A

VOUT recovery time

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	TIME			VOUT recovery time (ms)							

7.1.2.12 AVERAGE

Address offset: 0x9B

Averaged measurement result

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	RESULT			Averaged result. Updated after averaging is complete							

7.1.2.13 BOOST

Address offset: 0x9C

Boost operating mode snapshot (for battery voltage measurement)

Bit number					7	6	5	4	3	2	1	0
ID										A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	MODE			BOOST operating mode snapshot							
			HP	0	High Power mode							
			LP	1	Low Power mode							
			ULP	2	Ultra-Low Power mode							
			PT	3	Pass-through mode							
			DPS	4	Dynamic Power Smoothing mode							

7.1.2.14 STATUS

Address offset: 0x9D

ADC and VOUT droop detector and recovery counter status

Bit number					7	6	5	4	3	2	1	0
ID										C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	ADC			ADC status							
			Ready	0	Ready							
			Delay	1	Busy, waiting delay							
			Single	2	Busy, instant measurement							
			Droop	3	Busy, VOUT droop measurement active							
B	R	DROOP			Droop detector status							
			Off	0	Powered OFF							
			On	1	Powered ON							
C	R	RECOV			VOUT droop recovery time counter status							
			Stopped	0	Counter stopped							

Bit number						7	6	5	4	3	2	1	0
ID											C	B	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
			Running	1	Counter running								

7.1.2.15 OFFSETFACTORY

Address offset: 0x9E

Factory delivered value for offset correction.

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	OFFSET			Coded in signed 8-bit two's complement. The value is compensated in all future ADC conversions.								

7.1.2.16 OFFSETMEASURED

Address offset: 0x9F

ADC offset calibration result. Can be updated by on-chip offset measurement.

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	OFFSET			Coded in signed 8-bit two's complement. The value is compensated in all future ADC conversions.								

7.2 TIMER — Timer/monitor

TIMER can be used in the following ways, depending on configuration in CONFIG.

- Boot monitor
- Watchdog timer
- Wakeup timer
- General purpose timer

TIMER only runs one configuration at a time because it is shared for all functions. TIMER target is a 24-bit number split into three registers TARGET. The least significant bit (LSB) is equal to 15.625 ms. The value can be calculated using the given equation:

$$Value = \mathrm{ROUND}[\frac{\mathrm{Time(ms)}}{15.625}] - 1$$

Note: Timer target registers contain non-zero default values after power-up and reset.

TIMER is started and stopped using TASKS_START and TASKS_STOP, respectively

The wakeup timer wakes the system from Hibernate or Hibernate_PT mode. Do not use the watchdog timer or general purpose timer when the system is in Ship or Hibernate modes.

A pre-warning interrupt 32 ms before timer expiration is available in all timer modes, but is most relevant for Watchdog and General purpose timer modes. See register INTEN_SYSTEM_SET.

Timer Free event and interrupt in INTEN_SYSTEM_SET can be used to determine when TIMER becomes free. The interrupt is available when software stops a timer (or boot monitor) and whenever the general purpose timer expires.

7.2.1 Boot monitor

Boot monitor power cycles the host System on Chip when the software fails to boot within t_{BOOT_TIMER}.

Boot monitor starts when the chip enters Active mode unless the **SYSGDEN** pin has been pulled low externally. The pin state is checked during chip power-up.

Software can stop the boot monitor by activating the timer stop task in TASKS_STOP to avoid the power cycle. Boot monitor cannot be re-enabled through TWI after it has been stopped.

7.2.2 Watchdog timer

Watchdog timer expiration can be configured by host software to generate a host reset on the **PG/RESET** pin or a power cycle. When configured to issue a reset, nPM2100 is not reset internally.

A power cycle turns VOUT OFF for t_{PWRDN} and issues a reset through the **PG/RESET** pin. LDOSW is disabled and nPM2100 is reset internally.

7.2.3 Wakeup timer

The wakeup timer wakes the system from Hibernate or Hibernate_PT modes. Host software configures the timer before the device enters the Hibernate mode. The time programmed to the wakeup timer must be longer than t_{PWRDN}.

If the chip exits from Hibernate mode due to the wakeup timer expiring, TIMER mode is automatically changed to boot monitor.

7.2.4 General purpose timer

The general purpose timer interrupts the host after a timeout.

7.2.5 Electrical specification

T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
F_{TIMER}	Frequency of timer clock		64		Hz
t_{MIN_PERIOD}	Minimum time period		16		ms
t_{MAX_PERIOD}	Maximum time period		3		days
t_{BOOT_TIMER}	Boot monitor period		10		s
t_{PREWRN}	Time between prewarning interrupt and timer expiration		32		ms
$TIMER_{ACC\_25C}$	Accuracy of timer clock (T_J=25°C)		±3		%
$TIMER_{ACC}$	Accuracy of timer clock	-20		20	%
$TIMER_{ACC\_10\text{-}60C}$	Accuracy of timer clock, limited die temperature range -10°C<T_J<60°C	-10		10	%

Table 16: TIMER electrical specification

7.2.6 Registers

Instances

Instance	Base address	Description
TIMER	0x00000000	TIMER Registers

Register overview

Register	Offset	Description
TASKS_START	0xB0	Start task
TASKS_STOP	0xB1	Stop task
TASKS_KICK	0xB2	Watchdog kick task
CONFIG	0xB3	Timer mode select
TARGETHI	0xB4	Most significant byte
TARGETMID	0xB5	Middle byte
TARGETLO	0xB6	Least significant byte
STATUS	0xB7	Timer status

7.2.6.1 TASKS_START

Address offset: 0xB0

Start task

Bit number								7	6	5	4	3	2	1	0
ID															A
Reset 0x00								**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field		Value ID		Value	Description								
A	W	TIMER					Start task								
				NoEffect		0	No effect								
				Trigger		1	Start timer								

7.2.6.2 TASKS_STOP

Address offset: 0xB1

Stop task

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	TIMER			Stop task								
			NoEffect	0	No effect								
			Trigger	1	Stop timer (also boot monitor)								

7.2.6.3 TASKS_KICK

Address offset: 0xB2

Watchdog kick task

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	WD			Watchdog kick								
			NoEffect	0	No effect								
			Trigger	1	Kick watchdog								

7.2.6.4 CONFIG

Address offset: 0xB3

Timer mode select

Bit number						7	6	5	4	3	2	1	0
ID												A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	MODE			Mode select (only to be modified once timer has been stopped)								
			GenPurp	0	General purpose timer								
			WDRST	1	Watchdog timer with reset								
			WDPWRC	2	Watchdog timer with power cycle								
			WKUP	3	Wakeup timer (for Hibernate and Hibernate_PT modes)								

7.2.6.5 TARGETHI

Address offset: 0xB4

Most significant byte

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BYTE			The most significant byte of the 24-bit timer value								

7.2.6.6 TARGETMID

Address offset: 0xB5

Middle byte

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x02						**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BYTE			The middle byte of the 24-bit timer value								

7.2.6.7 TARGETLO

Address offset: 0xB6

Least significant byte

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x7F						**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	BYTE			The least significant byte of the 24-bit timer value (lsb equals to 1/64 seconds or 15.625 ms)								

7.2.6.8 STATUS

Address offset: 0xB7

Timer status

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	STATUS			Timer status								
			IDLE	0	Timer is idle								
			BUSY	1	Timer is busy								

7.3 Ship and Break-to-wake modes

Ship mode and Break-to-wake mode are the lowest power consumption modes. Ship mode provides the lowest current consumption IQ_{SHIP}.

Ship mode

There are two ways to enter and wake up from Ship mode.

The button connected to the **SHPHLD** pin is one way to access Ship mode, as described by the following.

- Press the button for a duration of t_{PWROFF}. The chip enters Ship mode when the button is released (**SHPHLD** returns high).
- To wake up the device, press the button again. The debounce time is $t_{SHPHLD\_DEB\_SHP}$.

The second way to enter and wake up from Ship mode is through a task register. In addition, either **SHPHLD** edge can be used for wakeup by doing the following:

- TWI configures the desired edge for wakeup in WAKEUP and checks that the **SHPHLD** pin is in an inactive state (`HIGH` when the falling edge is selected, and `LOW` when it is a rising edge). Pin state is visible in register MAIN.STATUS. TWI then activates the task in register TASKS_SHIP to enter Ship mode.
- Wakeup happens when a suitable edge appears on the **SHPHLD** pin. The debounce time is $t_{SHPHLD\_DEB\_SHP}$.

The **SHPHLD** pin includes both pull-up and pull-down resistors which can be controlled through register SHPHLD. Pull-up (default) is used together with a button. Pull-down can be used in Active mode to avoid a floating input pin.

Note: When rising edge detection has been selected, the external voltage on the **SHPHLD** pin must remain below VBAT to avoid leakage current towards the battery. If voltage is higher, an external series resistor or resistor divider can help to reduce the leakage.

Break-to-wake mode

Break-to-wake mode is a variant of Ship mode where wakeup happens once a connection between the **SHPHLD** pin and ground is broken. It is the second lowest current consumption ($IQ_{BREAKTOWAKE}$) mode of the device.

The **SHPHLD** pin is connected to ground using a wire or similar, and the system is set to break-to-wake mode for storage and transport. Once the wire is broken during first use, the system wakes up.

To configure Break-to-wake mode the pull-up resistor needs to be disabled and a suitable pull-up current PU_{CURR} activated in register SHPHLD. The recommended setting is `Low`. If additional leakage is present on the PCB trace connected to SHPHLD, setting `Moderate` or `High` can be used. Rising edge wakeup is set in register WAKEUP. Break-to-wake mode is then entered using task TASKS_SHIP. In addition, software has to make sure that the **SHPHLD** pin is `LOW` before activating the task.

7.3.1 Electrical specification

T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SHPHLD\_DEB\_SHP}$	Duration of SHPHLD button press to exit Ship mode	500	1000	2000	ms
t_{PWROFF}	Duration of SHPHLD button press to enter Ship mode (power OFF button)		2000		ms
R_{SHPHLD_PU}	SHPHLD pin pull-up resistor		100		kΩ
R_{SHPHLD_PD}	SHPHLD pin pull-down resistor		75		kΩ
PU_{CURR_00}	Break-to-wake mode; weakest pull-up current		19.5		nA
PU_{CURR_01}	Break-to-wake mode; low pull-up current		30		nA
PU_{CURR_10}	Break-to-wake mode; moderate pull-up current		60		nA
PU_{CURR_11}	Break-to-wake mode; high pull-up current		110		nA
V_{SHPHLD_RISE}	Rising voltage threshold on SHPHLD pin		0.6		V

Table 17: Ship mode electrical specification

7.3.2 Registers

Instances

Instance	Base address	Description
SHIP	0x00000000	SHIP Registers

Register overview

Register	Offset	Description
TASKS_SHIP	0xC0	Task for entering Ship mode
WAKEUP	0xC1	Select which edge wakes up the chip from Ship, Hibernate or Hibernate_PT modes
SHPHLD	0xC2	Configure pull-up and pull-down resistors for SHPHLD pin

7.3.2.1 TASKS_SHIP

Address offset: 0xC0

Task for entering Ship mode

Bit number									
						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	ENTER			Enter Ship mode								
			NoEffect	0	No effect								
			Trigger	1	Enter Ship mode								

7.3.2.2 WAKEUP

Address offset: 0xC1

Select which edge wakes up the chip from Ship, Hibernate or Hibernate_PT modes

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	EDGE			Select which edge wakes up the chip from Ship, Hibernate or Hibernate_PT modes								
			Falling	0	Falling edge								
			Rising	1	Rising edge								
B	RW	HIBERNATE			Select wakeup from hibernate by SHPHLD pin								
			Pin	0	Enable SHPHLD pin wakeup from Hibernate and Hibernate _PT modes								
			NoPin	1	Disable SHPHLD pin wakeup from Hibernate and Hibernate_PT modes								

7.3.2.3 SHPHLD

Address offset: 0xC2

Configure pull-up and pull-down resistors for SHPHLD pin

Bit number						7	6	5	4	3	2	1	0
ID									C	B	B	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	RESISTOR			Configure pull-up and pull-down resistors for SHPHLD pin								
			PullUp	0	Pull-up resistor active								
			None	1	No resistor								
			PullDown	2	Pull-down resistor active								
B	RW	CURR			Configure weak pull-up current								
			Weak	0	Weakest pull-up current								
			Low	1	Low pull-up current								
			Moderate	2	Moderate pull-up current								
			High	3	High pull-up current								
C	RW	PULL			Enable weak pull-up current								
			Disable	0	Weak pull-up disabled								
			Enable	1	Weak pull-up enabled								

7.4 Hibernate mode

Hibernate mode minimizes the quiescent current and provides autonomous wakeup.

The following hibernate modes are available:

- Hibernate – BOOST is running in Ultra-Low Power mode and LDOSW is available.
- Hibernate_PT – BOOST is set to Pass-through mode (VINT=VBAT). This mode can only be used when battery voltage is high enough (VBAT > $VINT_{BOR}$) to supply the chip directly without boosting. Battery and VINT voltage are not monitored and LDOSW is disabled.

Both Hibernate modes use more power than Ship mode, but provide faster wakeup (t_{SHPHLD_HIB}). Ship mode provides the lowest power consumption and slowest wakeup. Hibernate_PT mode is the third lowest power consumption mode (IQ_{HIB_PT}).

The following are alternative ways to exit both Hibernate modes:

- Exit automatically through the wakeup timer
- **SHPHLD** pin wakeup. The pin debounce time is adjustable through register DEBOUNCE.

Note: The wakeup timer must be set for longer than t_{PWRDN}.

Hibernate mode

The device enters Hibernate mode through register TASKS_HIBER. In Hibernate mode, BOOST is running (VINT > VBAT), **VOUT** is discharged to **AVSS1**, but LDOSW is possibly ON. This mode has higher power consumption than Hibernate_PT.

Wakeup is fast as VINT is already at the target voltage level. Register content remains.

Hibernate_PT mode

The device enters Hibernate_PT mode through register TASKS_HIBERPT. BOOST is set to Pass-through mode. **VOUT** is discharged to **AVSS1** and LDOSW is disabled.

Upon wakeup, the device executes full power-up sequence including register reset.

7.4.1 Electrical specification

T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
$t_{SHPHLD\_DEB\_HIB}$	SHPHLD debounce time in Hibernate and Hibernate PT modes		10, 30, 60, 100 (default), 300, 600, 1000, 3000		ms
t_{SHPHLD_HIB}	Wakeup time from Hibernate and Hibernate PT modes to Active mode using SHPHLD pin			1	ms

Table 18: Hibernate mode electrical specification

7.4.2 Registers

Instances

Instance	Base address	Description
HIBERNATE	0x00000000	HIBERNATE Registers

Register overview

Register	Offset	Description
TASKS_HIBER	0xC8	Task for entering Hibernate mode
TASKS_HIBERPT	0xC9	Task for entering Hibernate_PT mode
DEBOUNCE	0xCA	Debounce time setting for exiting Hibernate and Hibernate_PT modes

7.4.2.1 TASKS_HIBER

Address offset: 0xC8

Task for entering Hibernate mode

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	ENTER			Enter Hibernate mode								
			NoEffect	0	No effect								
			Trigger	1	Enter Hibernate mode								

7.4.2.2 TASKS_HIBERPT

Address offset: 0xC9

Task for entering Hibernate_PT mode

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	ENTER			Enter Hibernate_PT mode								
			NoEffect	0	No effect								
			Trigger	1	Enter Hibernate_PT mode								

7.4.2.3 DEBOUNCE

Address offset: 0xCA

Debounce time setting for exiting Hibernate and Hibernate_PT modes

Bit number						7	6	5	4	3	2	1	0
ID										B	B	B	A
Reset 0x07						**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	RW	ENABLE			SHPHLD debounce filter enable for exiting Hibernate and Hibernate_PT modes.								
			NoDebounce	0	Debounce filter by-passed								
			Debounce	1	Debounce filter enabled								
B	RW	TIME			SHPHLD debounce time setting for exiting Hibernate and Hibernate_PT modes. NOTE: Rising or falling edge detection is configured in Ship registers.								
			10MS	0	10 ms								
			30MS	1	30 ms								
			60MS	2	60 ms								

Bit number									7	6	5	4	3	2	1	0
ID													B	B	B	A
Reset 0x07									**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
ID	R/W	Field		Value ID		Value		Description								
				100MS		3		100 ms (default)								
				300MS		4		300 ms								
				600MS		5		600 ms								
				1000MS		6		1 s								
				3000MS		7		3 s								

7.5 Reset

The Reset button can be connected to the **PG/RESET** pin. This pin is an open drain reset input / power good output with internal pull-up. Alternatively, in so called single-button configuration, reset button can be moved to **SHPHLD** pin.

Host software and watchdog resets are also available. Reason for the reset is available in register RESET. The register needs to be cleared using TASKS_CLR.

Boot monitor is activated after each power cycle unless disabled using **SYSGDEN**.

Normal operation

A long logic-low (>$t_{RST\_DEB\_L}$) on **PG/RESET** causes a power cycle and resets the whole system. This feature is enabled by default after power-up, but can be disabled in register BUTTON.

If configured in register MAIN.INTEN_SYSTEM_SET, a short logic-low pulse on **PG/RESET** sends an interrupt to the host (> $t_{RST\_DEB\_S}$ and < $t_{RST\_DEB\_L}$). Host software reads the pin state in register MAIN.STATUS. Here the **PG/RESET** pin must not be connected to the host's reset input in order to avoid a host-only reset.

Single-button configuration

The Reset button can be assigned to the **SHPHLD** pin through register PIN. This enables a single button to be used to exit Ship mode, and as a reset button through a long press. This configuration disables reset button functionality from pin **PG/RESET**.

Host software reset

Host software can reset the device in register TASKS_RESET. As a consequence, a power cycle is performed. A reset is not possible in Ship or Hibernate mode.

Watchdog reset

Watchdog timer expiration causes either a host reset via **PG/RESET** or a complete power cycle. This can be configured in register TIMER.CONFIG.

In case of Watchdog reset the **PG/RESET** pin is toggled low for t_{PWRDN}. No internal reset occurs. Signals from the host connected to **GPIO[n]** may change state and impact the BOOST operating mode, for example. Boot monitor does not start.

A Watchdog power cycle resets all registers to defaults, toggles the **PG/RESET** pin, and switches **VOUT** OFF for t_{PWRDN}. LDOSW is disabled. (Both **VOUT** and **LSOUT/VOUTLDO** are discharged to **AVSS1**.)

Scratch registers

VBAT and VINT voltage domains contain scratch registers SCRATCHA and SCRATCHB, respectively.

SCRATCHA is only reset when VBAT falls below $VBAT_{POR\_FALLING}$. Registers WRITE and STROBE are used to store data into the SCRATCHA register and register READ is used to read it back.

SCRATCHB resets when VINT falls below $VINT_{BOR}$ or whenever the device goes to COLD START state. The register content remains in case of a watchdog reset. The register is not reset when device enters and exits Hibernate mode.

7.5.1 Electrical specification

T_J=-40°C to 105°C, VBAT=0.8 V to 3.4 V and T_J=25°C, VBAT=1.25 V for typical values (unless otherwise noted).

Symbol	Description	Min.	Typ.	Max.	Units
t_{PWRDN}	Length of reset pulse/power cycle		370		ms
$t_{RST\_DEB\_S}$	Reset button: short press debounce time		100		ms
$t_{RST\_DEB\_L}$	Reset button: long press debounce time		5, 10 (default), 30		s
R_{RST_PU}	Pull up resistor on PG/RESET pin		60		kΩ

Table 19: Reset electrical specification

7.5.2 Registers

Instances

Instance	Base address	Description
RESET	0x00000000	RESET Registers
		None

Register overview

Register	Offset	Description
TASKS_RESET	0xD0	SW reset task
TASKS_CLR	0xD1	Clear reset reason register
BUTTON	0xD2	Long press reset configuration
PIN	0xD3	Reset pin configuration
DEBOUNCE	0xD4	Debounce time setting for reset button
RESET	0xD5	Reset reason
ALTCONFIG	0xD6	LDOSW configuration in case of watchdog reset
WRITE	0xD7	Write to scratch register A
STROBE	0xD8	Strobe for scratch register A
READ	0xD9	Read from scratch register A
SCRATCHB	0xDA	Write and read scratch register B
WRITESTICKY	0xDB	Write to sticky register (requires strobing, use register STROBESTICKY)
STROBESTICKY	0xDC	Strobe for WRITESTICKY register

Register	Offset	Description
READSTICKY	0xDD	Read from sticky register (retains contents until VBAT is disconnected)
SYSGDENSTATUS	0xE2	Boot monitor and SYSGDEN pin status

7.5.2.1 TASKS_RESET

Address offset: 0xD0

SW reset task

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	SWRST			Trigger a power cycle								
			NoEffect	0	No effect								
			Trigger	1	Trigger a power cycle								

7.5.2.2 TASKS_CLR

Address offset: 0xD1

Clear reset reason register

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	CLR			Clear reset reason register								
			NoEffect	0	No effect								
			Trigger	1	Clear reset reason register (RESET.RESET)								

7.5.2.3 BUTTON

Address offset: 0xD2

Long press reset configuration

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LONGPRESS			Long press of button causes a reset								
			Enable	0	Long press reset enabled								
			Disable	1	Long press reset disabled								

7.5.2.4 PIN

Address offset: 0xD3

Reset pin configuration

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	SELECT			Select pin for reset button (reset button must be disabled in BUTTON register before configuring this register)							
			PGRESET	0	Reset button connected to PG/RESET							
			SHPHLD	1	Reset button connected to SHPHLD							

7.5.2.5 DEBOUNCE

Address offset: 0xD4

Debounce time setting for reset button

Bit number					7	6	5	4	3	2	1	0
ID											A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	TIME			Debounce time for reset button							
			10S	0	10 seconds							
			5S	1	5 seconds							
			20S	2	20 seconds							
			30S	3	30 seconds							

7.5.2.6 RESET

Address offset: 0xD5

Reset reason

Bit number					7	6	5	4	3	2	1	0
ID								B	B	B	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	R	BOR			Brown-out reset							
			NotActive	0	No brown-out reset happened							
			Active	1	Brown-out reset happened							
B	R	REASON			Reason for the previous reset (if several reasons occurred, only the first reason is stored)							
			ColdPwrUp	0	Cold power-up							
			TSD	1	Thermal shutdown							
			BootMonit	2	Boot monitor							
			Button	3	Long press reset button							
			WdRst	4	Watchdog reset							
			WdPwrCycle	5	Watchdog power cycle							
			SwReset	6	Software reset task							
			HiberPin	7	SHPHLD pin exit from Hibernate mode							
			HiberTimer	8	Timer exit from Hibernate mode							
			HiberPtPin	9	SHPHLD pin exit from Hibernate_PT mode							
			HiberPtTimer	10	Timer exit from Hibernate_PT mode							
			PowerOffButton	11	Power OFF button							
			ShipExit	12	Exit from Ship mode							
			OCP	13	Overcurrent protection (OCP)							

7.5.2.7 ALTCONFIG

Address offset: 0xD6

LDOSW configuration in case of watchdog reset

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	LDOSW			Select LDOSW behaviour in WD reset								
			ON	0	LDOSW not impacted by watchdog reset								
			OFF	1	LDOSW disabled in WD RESET state								

7.5.2.8 WRITE

Address offset: 0xD7

Write to scratch register A

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW	SCRATCHA			Scratch register data to be written (requires strobing, use register STROBE)								

7.5.2.9 STROBE

Address offset: 0xD8

Strobe for scratch register A

Bit number						7	6	5	4	3	2	1	0
ID													A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	W	SCRATCHA			Strobe for scratch A								
			NoEffect	0	No effect								
			Strobe	1	Write 1 to strobe values into scratch register A								

7.5.2.10 READ

Address offset: 0xD9

Read from scratch register A

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	SCRATCHA			Scratch register (retains contents until VBAT is disconnected).								

7.5.2.11 SCRATCHB

Address offset: 0xDA

Write and read scratch register B

Bit number					7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	DATA			Scratch register (retains contents until VINTBOR triggers)							

7.5.2.12 WRITESTICKY

Address offset: 0xDB

Write to sticky register (requires strobing, use register STROBESTICKY)

Bit number					7	6	5	4	3	2	1	0
ID										C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW	BOOTMONSEL			Boot monitor							
			NotSelected	0	Boot monitor is controlled by pin SYSGDEN							
			Selected	1	Boot monitor is controlled by BOOTMONEN register bit							
B	RW	BOOTMONEN			Boot monitor control (effective only when BOOTMONSEL=1)							
			Disabled	0	Boot monitor disabled							
			Enabled	1	Boot monitor enabled							
C	RW	PWRBUTTON			Power OFF button							
			NotDisabled	0	Enable power OFF button							
			Disabled	1	Disable power OFF button							

7.5.2.13 STROBESTICKY

Address offset: 0xDC

Strobe for WRITESTICKY register

Bit number					7	6	5	4	3	2	1	0
ID												A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	W	STROBE			Strobe for WRITESTICKY registers							
			NoEffect	0	No effect							
			Strobe	1	Write 1 to strobe values into the sticky register							

7.5.2.14 READSTICKY

Address offset: 0xDD

Read from sticky register (retains contents until VBAT is disconnected)

Bit number						7	6	5	4	3	2	1	0
ID												C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	BOOTMONSEL			Boot monitor select								
			NotSelected	0	Boot monitor controlled by pin SYSGDEN								
			Selected	1	Boot monitor controlled by BOOTMONEN register bit								
B	R	BOOTMONEN			Boot monitor control (effective only when BOOTMONSEL=1)								
			Disabled	0	Boot monitor disabled								
			Enabled	1	Boot monitor enabled								
C	R	PWRBUTTON			Power OFF button								
			NotDisabled	0	Power OFF button in use								
			Disabled	1	Power OFF button disabled								

7.5.2.15 SYSGDENSTATUS

Address offset: 0xE2

Boot monitor and SYSGDEN pin status

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	BOOTMONSTATUS			Boot monitor status								
			Disabled	0	Boot monitor disabled								
			SYSGDEN	1	Boot monitor is active unless SYSGDENSTATE=0								
B	R	SYSGDENSTATE			Latched SYSGDEN pin state								
			LOW	0	SYSGDEN was low during power-up								
			HIGH	1	SYSGDEN was high during power-up								

7.6 TWI — I^{2}C compatible two-wire interface

TWI is a two-wire interface that controls and monitors the device state through registers.

Main Features

- I^{2}C compatible up to 400 kHz
- TWI clock supports 100 kHz to 1 MHz

A GPIO pin can be set as an interrupt pin, see GPIO – General purpose input/output on page 51.

Interface supply and voltage levels

TWI is supplied by internal connection to VOUT. The external pull-up resistors must be connected to VOUT too.

Addressing

The 7-bit slave address is 111 0100 or 0x74.

The registers have 8-bit addressing and 8-bit data.

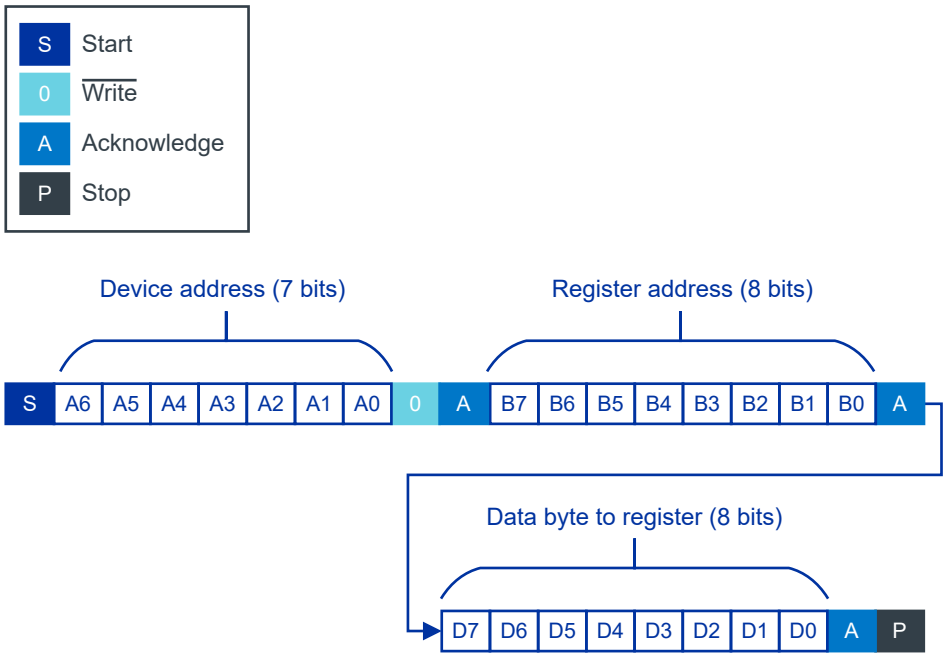


Figure 39: TWI write example

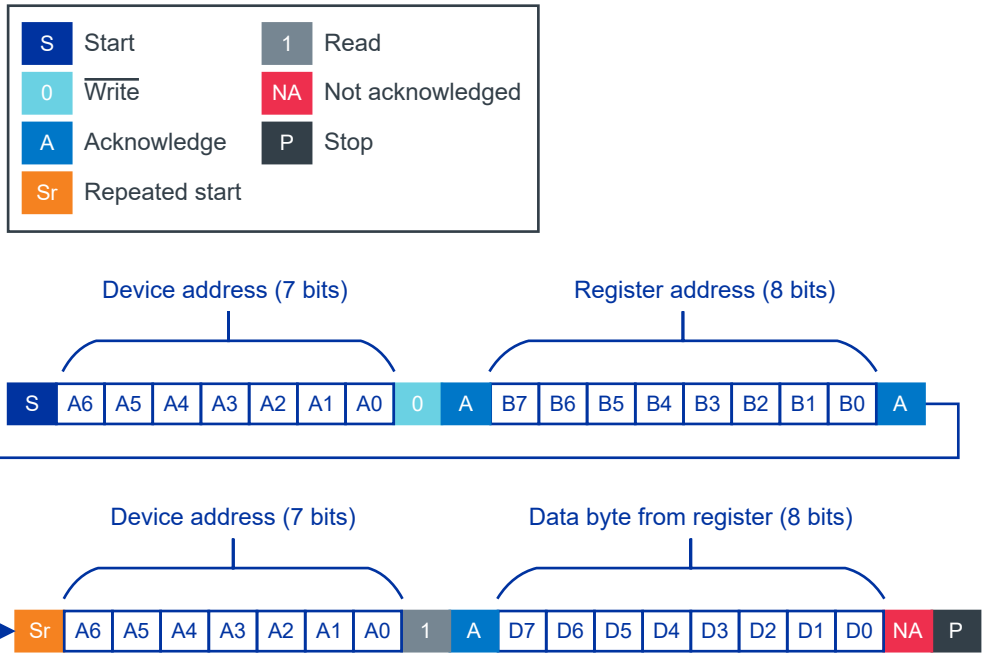


Figure 40: TWI read example

Register types and usage

Bit SET and CLR registers enable software to set and clear individual bits in a register without performing a read-modify-write operation. Writing `1` to a bit in the SET or CLR register will set or clear the same bit respectively. Writing `0` to a bit in the SET or CLR register has no effect. Reading the SET (or CLR) register returns the value of the register in question.

Tasks are used to trigger actions, such as to start or stop a particular behavior. A task is triggered when firmware writes `1` to the task register. Writing `0` to a task register has no effect. Reading the register always returns `0`.

Event SET and CLR registers enable software to read and clear individual events in a register without performing a read-modify-write operation. Reading the SET or CLR register informs software about events.

Writing 1 to the CLR register clears the event and the corresponding interrupt, respectively. Writing 1 to a SET register generates an event for debugging purposes. Writing 0 to SET or CLR register has no effect.

Most events generated by the device can be configured to generate an interrupt towards the host. Multiple events can be enabled to generate interrupts simultaneously. Because there is one single interrupt signal, all SET or CLR event registers need to be read to resolve the correct interrupt source. Event registers are located in adjacent addresses which allow for burst read.

Software can enable and disable individual interrupts through registers INTENSET and INTENCLR, without having to perform a read-modify-write operation. Writing 1 to INTENSET enables the interrupt. Writing 1 to INTENCLR disables it. Reading the INTENSET or INTENCLR register informs software about interrupts that are currently enabled. Writing 0 to INTENSET or INTENCLR register has no effect.

Interrupts are acknowledged by writing 1 to the corresponding events CLR register bit.

Status registers are read-only and indicate the current state of a signal, event, or mode.

Sticky registers retain their contents until the battery has been disconnected. See RESET registers for details.

7.6.1 TWI timing diagram

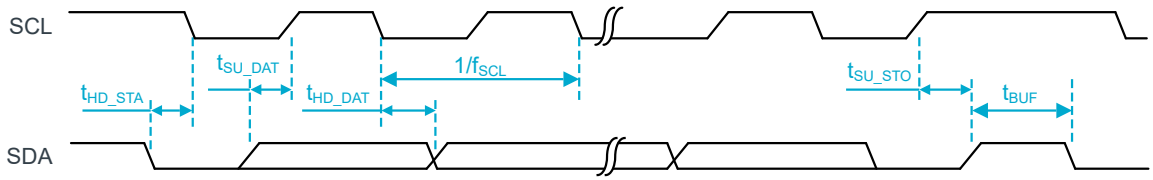


Figure 41: TWI timing diagram

7.6.2 Electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
f_{SCL}	Bit rate for TWI	100		1000	kbps
t_{SU_DAT}	Data setup time before positive edge on SCL, all modes	50			ns
t_{HD_DAT}	Data hold time after negative edge on SCL, all modes	0			ns
t_{HD_STA}	Hold time from for START condition (SDA low to SCL low), 100 kbps	260			ns
t_{SU_STO}	Setup time from SCL high to STOP condition, 100 kbps	260			ns
t_{BUF}	Bus free time between STOP and START conditions		500		ns

Table 20: TWI electrical specification

7.6.3 Registers

Instances

Instance	Base address	Description
MAIN	0x00000000	MAIN Registers

Register overview

Register	Offset	Description
EVENTS_SYSTEM_SET	0x0	System Event Set
EVENTS_ADC_SET	0x1	ADC Event Set
EVENTS_GPIO_SET	0x2	GPIO Event Set
EVENTS_BOOST_SET	0x3	BOOST Event Set
EVENTS_LDOSW_SET	0x4	LDOSW Event Set
EVENTS_SYSTEM_CLR	0x5	System Event Clear
EVENTS_ADC_CLR	0x6	ADC Event Clear
EVENTS_GPIO_CLR	0x7	GPIO Event Clear
EVENTS_BOOST_CLR	0x8	BOOST Event Clear
EVENTS_LDOSW_CLR	0x9	LDOSW Event Clear
INTEN_SYSTEM_SET	0xA	System Interrupt Enable Set
INTEN_ADC_SET	0xB	ADC Interrupt Enable Set
INTEN_GPIO_SET	0xC	GPIO Interrupt Enable Set
INTEN_BOOST_SET	0xD	BOOST Interrupt Enable Set
INTEN_LDOSW_SET	0xE	LDOSW Interrupt Enable Set
INTEN_SYSTEM_CLR	0xF	System Interrupt Enable Clear
INTEN_ADC_CLR	0x10	ADC Interrupt Enable Clear
INTEN_GPIO_CLR	0x11	GPIO Interrupt Enable Clear
INTEN_BOOST_CLR	0x12	BOOST Interrupt Enable Clear
INTEN_LDOSW_CLR	0x13	LDOSW Interrupt Enable Clear
REQUESTSET	0x14	Enable function (read current status)
REQUESTCLR	0x15	Disable function (read current status)
STATUS	0x16	Status register

7.6.3.1 EVENTS_SYSTEM_SET

Address offset: 0x0

System Event Set

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	DIETWARN			Die temperature warning. Writing 1 sets the event (for debugging).							
B	RW W1S	SHPHLDFALL			SHPHLD falling edge. Writing 1 sets the event (for debugging).							
C	RW W1S	SHPHLDRISE			SHPHLD rising edge. Writing 1 sets the event (for debugging).							
D	RW W1S	PGRESETFALL			PG/RESET falling edge. Writing 1 sets the event (for debugging).							
E	RW W1S	PGRESETRISE			PG/RESET rising edge. Writing 1 sets the event (for debugging).							
F	RW W1S	TIMER			General purpose TIMER expired. Writing 1 sets the event (for debugging).							
G	RW W1S	TIMERPREWRN			Prewarning event before TIMER expires (general purpose, boot monitor, wakeup, WD reset, WD power cycle). Writing 1 sets the event (for debugging).							
H	RW W1S	TIMERFREE			Timer free event (the event occurs when the TIMER reaches its set duration in general purpose timer mode, or if the TIMER is manually stopped via TIMER.TASK_STOP register). Writing 1 sets the event (for debugging).							

7.6.3.2 EVENTS_ADC_SET

Address offset: 0x1

ADC Event Set

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	VBATRDY			ADC VBAT conversion ready. Writing 1 sets the event (for debugging).							
B	RW W1S	DIETRDY			ADC die temperature conversion ready. Writing 1 sets the event (for debugging).							
C	RW W1S	DROOPDET			ADC droop detector conversion ready. Writing 1 sets the event (for debugging).							
D	RW W1S	VOUTRDY			ADC VOUT conversion ready. Writing 1 sets the event (for debugging).							

7.6.3.3 EVENTS_GPIO_SET

Address offset: 0x2

GPIO Event Set

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	GPIO0FALL			Falling edge on GPIO0. Writing 1 sets the event (for debugging).							
B	RW W1S	GPIO0RISE			Rising edge on GPIO0. Writing 1 sets the event (for debugging).							
C	RW W1S	GPIO1FALL			Falling edge on GPIO1. Writing 1 sets the event (for debugging).							
D	RW W1S	GPIO1RISE			Rising edge on GPIO1. Writing 1 sets the event (for debugging).							
E	RW W1S	GPIO2FALL			Reserved (falling edge on GPIO2). Writing 1 sets the event (for debugging).							
F	RW W1S	GPIO2RISE			Reserved (rising edge on GPIO2). Writing 1 sets the event (for debugging).							

7.6.3.4 EVENTS_BOOST_SET

Address offset: 0x3

BOOST Event Set

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	VBATWRNF			VBAT dropped below VBATMINH threshold. Writing 1 sets the event (for debugging).							
B	RW W1S	VBATWRNR			VBAT rose above VBATMINH threshold. Writing 1 sets the event (for debugging).							
C	RW W1S	VOUTMIN			VOUT dropped below VOUTMIN threshold. Writing 1 sets the event (for debugging).							
D	RW W1S	VOUTWRNF			VOUT dropped below VOUTWRN threshold. Writing 1 sets the event (for debugging).							
E	RW W1S	VOUTWRNR			VOUT rose above VOUTWRN threshold. Writing 1 sets the event (for debugging).							
F	RW W1S	VOUTDPSF			VOUT dropped below VOUTDPS threshold. Writing 1 sets the event (for debugging).							
G	RW W1S	VOUTDPSR			VOUT rose above VOUTDPS threshold. Writing 1 sets the event (for debugging).							
H	RW W1S	VOUTOK			VOUT reached target level after being low. Writing 1 sets the event (for debugging).							

7.6.3.5 EVENTS_LDOSW_SET

Address offset: 0x4

LDOSW Event Set

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	OCP			LDOSW overcurrent. Writing 1 sets the event (for debugging).							
B	RW W1S	VINTFAIL			VINT didn't recover during LDOSW powerup using digital stepper. Writing 1 sets the event (for debugging).							

7.6.3.6 EVENTS_SYSTEM_CLR

Address offset: 0x5

System Event Clear

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	DIETWARN			Die temperature warning. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
B	RW W1C	SHPHLDFALL			SHPHLD falling edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
C	RW W1C	SHPHLDRISE			SHPHLD rising edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
D	RW W1C	PGRESETFALL			PG/RESET falling edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
E	RW W1C	PGRESETRISE			PG/RESET rising edge. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
F	RW W1C	TIMER			General purpose TIMER expired. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
G	RW W1C	TIMERPREWRN			Prewarning event before TIMER expires (general purpose, boot monitor, wakeup, WD reset, WD power cycle). Writing 1 clears the event (e.g. to acknowledge an interrupt).							
H	RW W1C	TIMERFREE			Timer free event (the event occurs when the TIMER reaches its set duration in general purpose timer mode, or if the TIMER is manually stopped via TIMER.TASK_STOP register). Writing 1 clears the event (e.g. to acknowledge an interrupt).							

7.6.3.7 EVENTS_ADC_CLR

Address offset: 0x6

ADC Event Clear

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	VBATRDY			ADC VBAT conversion ready. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
B	RW W1C	DIETRDY			ADC die temperature conversion ready. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
C	RW W1C	DROOPDET			ADC droop detector conversion ready. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
D	RW W1C	VOUTRDY			ADC VOUT conversion ready. Writing 1 clears the event (e.g. to acknowledge an interrupt).							

7.6.3.8 EVENTS_GPIO_CLR

Address offset: 0x7

GPIO Event Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	GPIO0FALL			Falling edge on GPIO0. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
B	RW W1C	GPIO0RISE			Rising edge on GPIO0. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
C	RW W1C	GPIO1FALL			Falling edge on GPIO1. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
D	RW W1C	GPIO1RISE			Rising edge on GPIO1. Writing 1 clears the event (e.g. to acknowledge an interrupt).							
E	RW W1C	GPIO2FALL			Reserved (falling edge on GPIO2). Writing 1 clears the event (e.g. to acknowledge an interrupt).							
F	RW W1C	GPIO2RISE			Reserved (rising edge on GPIO2). Writing 1 clears the event (e.g. to acknowledge an interrupt).							

7.6.3.9 EVENTS_BOOST_CLR

Address offset: 0x8

BOOST Event Clear

Bit number						7	6	5	4	3	2	1	0
ID						H	G	F	E	D	C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1C	VBATWRNF			VBAT dropped below VBATMINH threshold. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
B	RW W1C	VBATWRNR			VBAT rose above VBATMINH threshold. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
C	RW W1C	VOUTMIN			VOUT dropped below VOUTMIN threshold. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
D	RW W1C	VOUTWRNF			VOUT dropped below VOUTWRN threshold. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
E	RW W1C	VOUTWRNR			VOUT rose above VOUTWRN threshold. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
F	RW W1C	VOUTDPSF			VOUT dropped below VOUTDPS threshold. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
G	RW W1C	VOUTDPSR			VOUT rose above VOUTDPS threshold. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
H	RW W1C	VOUTOK			VOUT reached target level after being low. Writing 1 clears the event (e.g. to acknowledge an interrupt).								

7.6.3.10 EVENTS_LDOSW_CLR

Address offset: 0x9

LDOSW Event Clear

Bit number						7	6	5	4	3	2	1	0
ID												B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	RW W1C	OCP			LDOSW overcurrent. Writing 1 clears the event (e.g. to acknowledge an interrupt).								
B	RW W1C	VINTFAIL			VINT didn't recover during LDOSW powerup using digital stepper. Writing 1 clears the event (e.g. to acknowledge an interrupt).								

7.6.3.11 INTEN_SYSTEM_SET

Address offset: 0xA

System Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	DIETWARN			Writing 1 enables interrupts from the DIETWARN event							
B	RW W1S	SHPHLDFALL			Writing 1 enables interrupts from the SHPHLDFALL event							
C	RW W1S	SHPHLDRISE			Writing 1 enables interrupts from the SHPHLDRISE event							
D	RW W1S	PGRESETFALL			Writing 1 enables interrupts from the PGRESETFALL event							
E	RW W1S	PGRESETRISE			Writing 1 enables interrupts from the PGRESETRISE event							
F	RW W1S	TIMER			Writing 1 enables interrupts from the TIMER event							
G	RW W1S	TIMERPREWRN			Writing 1 enables interrupts from the TIMERPREWRN event							
H	RW W1S	TIMERFREE			Writing 1 enables interrupts from the TIMERFREE event							

7.6.3.12 INTEN_ADC_SET

Address offset: 0xB

ADC Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	VBATRDY			Writing 1 enables interrupts from the VBATRDY event							
B	RW W1S	DIETRDY			Writing 1 enables interrupts from the DIETRDY event							
C	RW W1S	DROOPDET			Writing 1 enables interrupts from the DROOPDET event							
D	RW W1S	VOUTRDY			Writing 1 enables interrupts from the VOUTRDY event							

7.6.3.13 INTEN_GPIO_SET

Address offset: 0xC

GPIO Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	GPIO0FALL			Writing 1 enables interrupts from the GPIO0FALL event							
B	RW W1S	GPIO0RISE			Writing 1 enables interrupts from the GPIO0RISE event							
C	RW W1S	GPIO1FALL			Writing 1 enables interrupts from the GPIO1FALL event							
D	RW W1S	GPIO1RISE			Writing 1 enables interrupts from the GPIO1RISE event							
E	RW W1S	GPIO2FALL			Writing 1 enables interrupts from the GPIO2FALL event							
F	RW W1S	GPIO2RISE			Writing 1 enables interrupts from the GPIO2RISE event							

7.6.3.14 INTEN_BOOST_SET

Address offset: 0xD

BOOST Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	VBATWRNF			Writing 1 enables interrupts from the VBATWRNF event							
B	RW W1S	VBATWRNR			Writing 1 enables interrupts from the VBATWRNR event							
C	RW W1S	VOUTMIN			Writing 1 enables interrupts from the VOUTMIN event							
D	RW W1S	VOUTWRNF			Writing 1 enables interrupts from the VOUTWRNF event							
E	RW W1S	VOUTWRNR			Writing 1 enables interrupts from the VOUTWRNR event							
F	RW W1S	VOUTDPSF			Writing 1 enables interrupts from the VOUTDPSF event							
G	RW W1S	VOUTDPSR			Writing 1 enables interrupts from the VOUTDPSR event							
H	RW W1S	VOUTOK			Writing 1 enables interrupts from the VOUTOK event							

7.6.3.15 INTEN_LDOSW_SET

Address offset: 0xE

LDOSW Interrupt Enable Set

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	OCP			Writing 1 enables interrupts from the OCP event							
B	RW W1S	VINTFAIL			Writing 1 enables interrupts from the VINTFAIL event							

7.6.3.16 INTEN_SYSTEM_CLR

Address offset: 0xF

System Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	DIETWARN			Writing 1 disables interrupts from the DIETWARN event							
B	RW W1C	SHPHLDFALL			Writing 1 disables interrupts from the SHPHLDFALL event							
C	RW W1C	SHPHLDRISE			Writing 1 disables interrupts from the SHPHLDRISE event							
D	RW W1C	PGRESETFALL			Writing 1 disables interrupts from the PGRESETFALL event							
E	RW W1C	PGRESETRISE			Writing 1 disables interrupts from the PGRESETRISE event							
F	RW W1C	TIMER			Writing 1 disables interrupts from the TIMER event							
G	RW W1C	TIMERPREWRN			Writing 1 disables interrupts from the TIMERPREWRN event							
H	RW W1C	TIMERFREE			Writing 1 disables interrupts from the TIMERFREE event							

7.6.3.17 INTEN_ADC_CLR

Address offset: 0x10

ADC Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID									D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	VBATRDY			Writing 1 disables interrupts from the VBATRDY event							
B	RW W1C	DIETRDY			Writing 1 disables interrupts from the DIETRDY event							
C	RW W1C	DROOPDET			Writing 1 disables interrupts from the DROOPDET event							
D	RW W1C	VOUTRDY			Writing 1 disables interrupts from the VOUTRDY event							

7.6.3.18 INTEN_GPIO_CLR

Address offset: 0x11

GPIO Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID							F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	GPIO0FALL			Writing 1 disables interrupts from the GPIO0FALL event							
B	RW W1C	GPIO0RISE			Writing 1 disables interrupts from the GPIO0RISE event							
C	RW W1C	GPIO1FALL			Writing 1 disables interrupts from the GPIO1FALL event							
D	RW W1C	GPIO1RISE			Writing 1 disables interrupts from the GPIO1RISE event							
E	RW W1C	GPIO2FALL			Writing 1 disables interrupts from the GPIO2FALL event							
F	RW W1C	GPIO2RISE			Writing 1 disables interrupts from the GPIO2RISE event							

7.6.3.19 INTEN_BOOST_CLR

Address offset: 0x12

BOOST Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID					H	G	F	E	D	C	B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	VBATWRNF			Writing 1 disables interrupts from the VBATWRNF event							
B	RW W1C	VBATWRNR			Writing 1 disables interrupts from the VBATWRNR event							
C	RW W1C	VOUTMIN			Writing 1 disables interrupts from the VOUTMIN event							
D	RW W1C	VOUTWRNF			Writing 1 disables interrupts from the VOUTWRNF event							
E	RW W1C	VOUTWRNR			Writing 1 disables interrupts from the VOUTWRNR event							
F	RW W1C	VOUTDPSF			Writing 1 disables interrupts from the VOUTDPSF event							
G	RW W1C	VOUTDPSR			Writing 1 disables interrupts from the VOUTDPSR event							
H	RW W1C	VOUTOK			Writing 1 disables interrupts from the VOUTOK event							

7.6.3.20 INTEN_LDOSW_CLR

Address offset: 0x13

LDOSW Interrupt Enable Clear

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x00					**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	OCP			Writing 1 disables interrupts from the OCP event							
B	RW W1C	VINTFAIL			Writing 1 disables interrupts from the VINTFAIL event							

7.6.3.21 REQUESTSET

Address offset: 0x14

Enable function (read current status)

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x02					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1S	DIETEMP			Start die temperature monitoring (for thermal warning and thermal shutdown)							
			NoEffect	0	No effect							
			Trigger	1	Start die temperature monitoring							
B	RW W1S	DIETEMPENA			Enable die temperature monitoring when BOOST is in HP mode (for thermal warning and thermal shutdown)							
			NoEffect	0	No effect							
			Enable	1	Enable die temperature monitoring in HP mode							

7.6.3.22 REQUESTCLR

Address offset: 0x15

Disable function (read current status)

Bit number					7	6	5	4	3	2	1	0
ID											B	A
Reset 0x02					**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value	Description							
A	RW W1C	DIETEMP			Stop die temperature monitoring (for thermal warning and thermal shutdown)							
			NoEffect	0	No effect							
			Trigger	1	Stop die temperature monitoring							
B	RW W1C	DIETEMPENA			Disable die temperature monitoring when BOOST is in HP mode (for thermal warning and thermal shutdown)							
			NoEffect	0	No effect							
			Disable	1	Disable die temperature monitoring in HP mode							

7.6.3.23 STATUS

Address offset: 0x16

Status register

Bit number						7	6	5	4	3	2	1	0
ID											C	B	A
Reset 0x00						**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value	Description								
A	R	SHPHLD			Status of SHPHLD pin								
			Low	0	Pin low								
			High	1	Pin high								
B	R	PGRESET			Status of PG/RESET pin								
			Low	0	Pin low								
			High	1	Pin high								
C	R	DIETEMP			Status of thermal warning								
			Low	0	Die temperature below warning level								
			Active	1	Die temperature above warning level								

8 Application

The following application example uses nPM2100 and an nRF5x Bluetooth Low Energy System on Chip (SoC). For other configurations, see Reference circuitry on page 100.

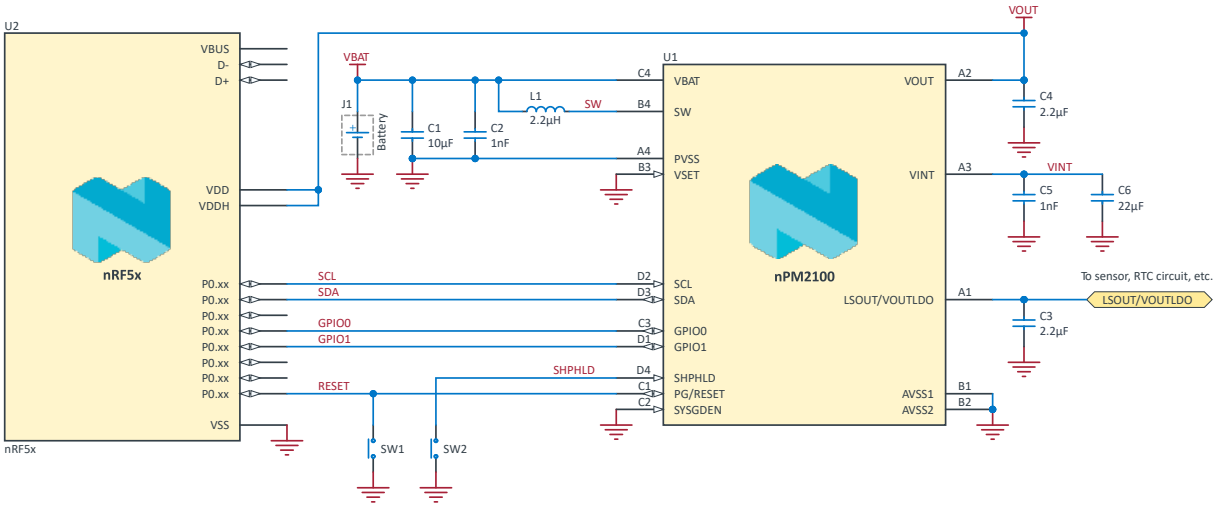


Figure 42: Application example

9 Hardware and layout

9.1 Pin assignments

The pin assignment figures and tables describe the pinouts for the product variants of the chip.

9.1.1 WLCSP ball assignments

The ball assignment figure and table describe the assignments for this variant of the chip.

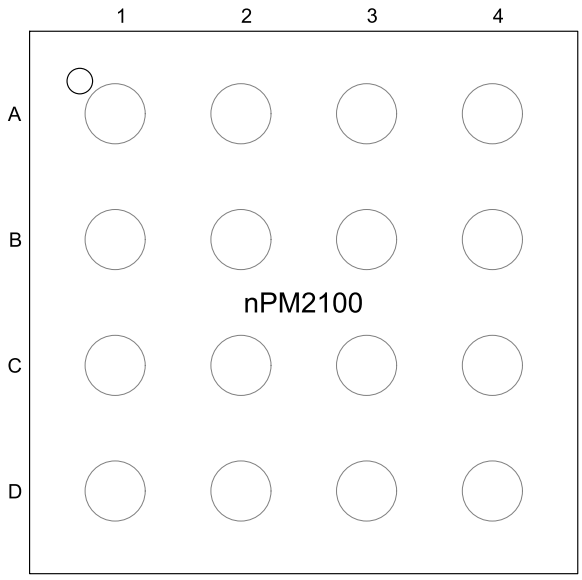


Figure 43: WLCSP ball assignments (top view)

Ball	Name	Function	Description
A1	**LSOUT/VOUTLDO**	Power	LDOSW output, can be left not connected if not used
A2	**VOUT**	Power	BOOST output for the load
A3	**VINT**	Power	BOOST output, decoupling for the internal supply. No external load is allowed.
A4	**PVSS**	Power	Power ground
B1	**AVSS1**	Power	Ground
B2	**AVSS2**	Power	Ground
B3	**VSET**	Analog input	BOOST output voltage selection, internal pull-up to VINT (leave pin not connected for 3.0 V or connect to ground for 1.8 V)
B4	**SW**	Power	Coil for BOOST

Ball	Name	Function	Description
C1	**PG/RESET**	Digital I/O, OD	Power good/reset output, reset button input (open drain, internal pull-up to VINT). Can be left not connected if not used.
C2	**SYSGDEN**	Digital input	Leave pin not connected (boot monitor enabled) or connect to ground (boot monitor disabled) externally.
C3	**GPIO0**	Digital I/O	GPIO, can be left not connected if not used
C4	**VBAT**	Power	Input supply, battery voltage
D1	**GPIO1**	Digital I/O	GPIO, can be left not connected if not used
D2	**SCL**	Digital input	TWI clock, external pull-up connected to VOUT
D3	**SDA**	Digital I/O	TWI data, external pull-up connected to VOUT
D4	**SHPHLD**	Analog input	Wakeup from Ship mode. (Also reset button input, so called single-button case). Can be left not connected if not used.

Table 21: Ball assignments

9.1.2 QFN pin assignments

The pin assignment figure and table describe the assignments for this variant of the chip.

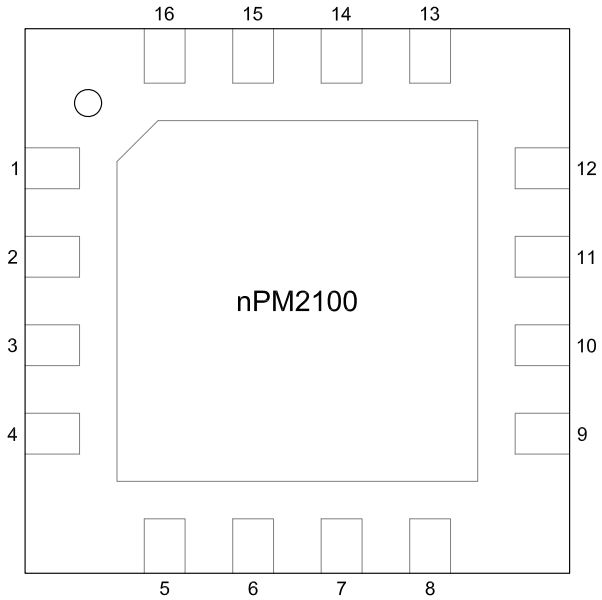


Figure 44: QFN pin assignments (top view)

Pin	Name	Function	Description
1	VSET	Analog input	BOOST output voltage selection, internal pull-up to VINT (leave pin not connected for 3.0 V or connect to ground for 1.8 V)
2	SW	Power	Coil for BOOST
3	VBAT	Power	Input supply, battery voltage
4	SHPHLD	Analog input	Wakeup from Ship mode (also reset button input, so called single-button case). Can be left not connected if not used.
5	GPIO0	Digital I/O	GPIO, can be left not connected if not used
6	SDA	Digital I/O	TWI data, external pull-up connected to VOUT
7	SCL	Digital input	TWI clock, external pull-up connected to VOUT
8	SYSGDEN	Digital IN	Leave pin not connected (boot monitor enabled) or connect to ground (boot monitor disabled) externally.
9	GPIO1	Digital I/O	GPIO, can be left not connected if not used
10	PG/RESET	Digital I/O, OD	Power good/reset output, reset button input (open drain, internal pull-up to VINT). Can be left not connected if not used.
11	AVSS2	Power	Ground
12	LSOUT/ VOUTLDO	Power	LDOSW output, can be left not connected if not used
13	VOUT	Power	BOOST output for the load
14	VINT	Power	BOOST output, decoupling for the internal supply. No external load is allowed.
15	VINT	Power	BOOST output, decoupling for the internal supply. No external load is allowed.
16	PVSS	Power	Power ground
Exposed pad	AVSS1	Power	Ground

Table 22: QFN pin assignment

9.2 Mechanical specifications

The mechanical specifications for the package shows the dimensions.

9.2.1 WLCSP package

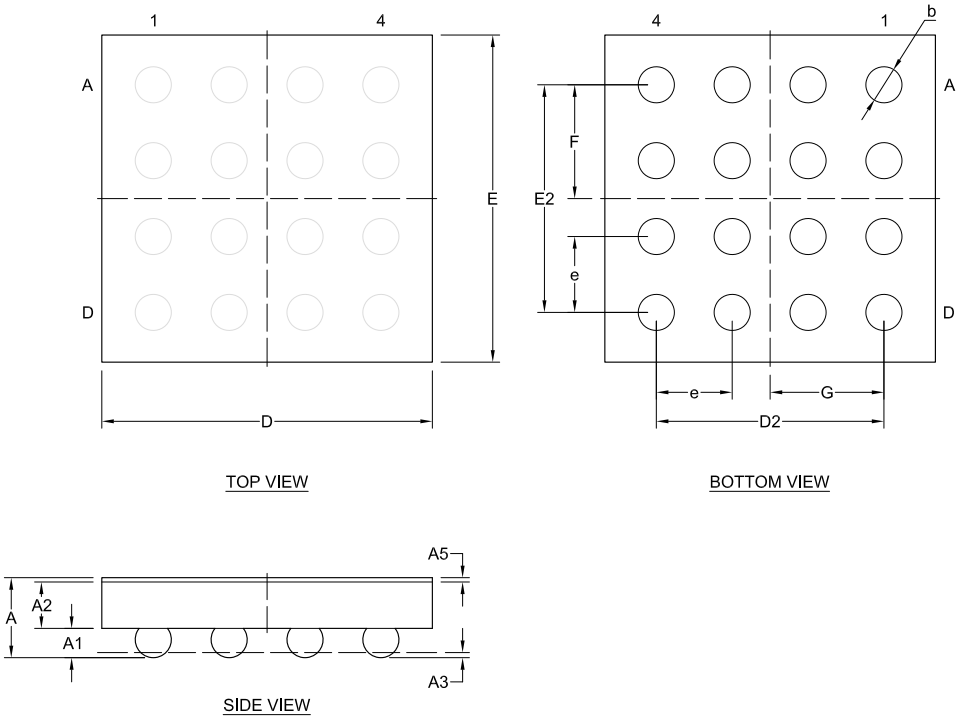


Figure 45: WLCSP 1.9x1.9 mm package

	A	A1	A2	A3	A5	D	E	D2, E2	F, G	e	b
Min.	0.406	0.14	0.244		0.022						0.19
Typ.	0.464		0.269	0.03	0.025	1.9175	1.8975	1.32	0.66	0.44	
Max.	0.522	0.2	0.294		0.028						0.25

Table 23: WLCSP dimensions in millimeters

9.2.2 QFN package

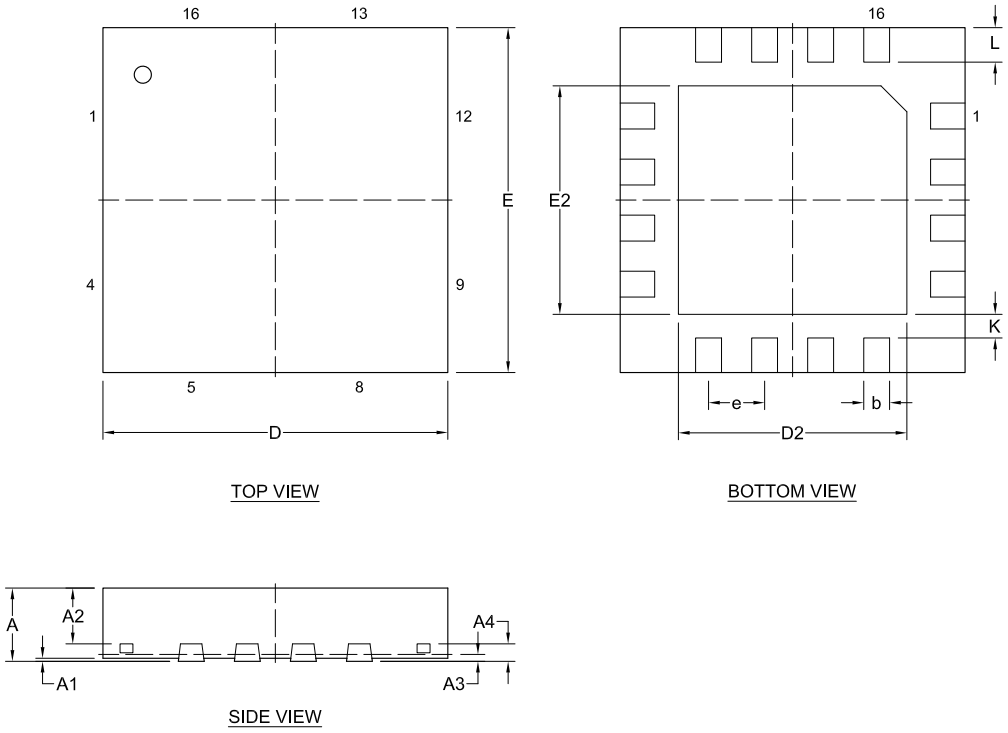


Figure 46: QFN16 4.0x4.0 mm package

	A	A1	A2	A3	A4	D, E	D2, E2	L	K	e	b
Min.	0.8	0				3.9	2.55	0.35			0.25
Typ.	0.85	0.035	0.65	0.08	0.203	4.0	2.65	0.4	0.275	0.65	0.3
Max.	0.9	0.05	0.67			4.1	2.75	0.45			0.35

Table 24: QFN dimensions in millimeters

9.3 Reference circuitry

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

The following reference circuits for nPM2100 show the schematics and components to support different configurations in a design.

	Configuration 1	Configuration 2
Battery type	Single alkaline AA/AAA	Lithium CR2032
LDOSW	Load switch	LDO regulator
VSET	Grounded	Not connected
VOUT	1.8 V	3.0 V
CVINT	10 µF	10 µF to 22 µF

Table 25: Reference circuit configuration

9.3.1 Configuration 1

The reference schematic for a configuration with a single alkaline AA/AAA battery is shown here. In this configuration VOUT is set to 1.8 V.

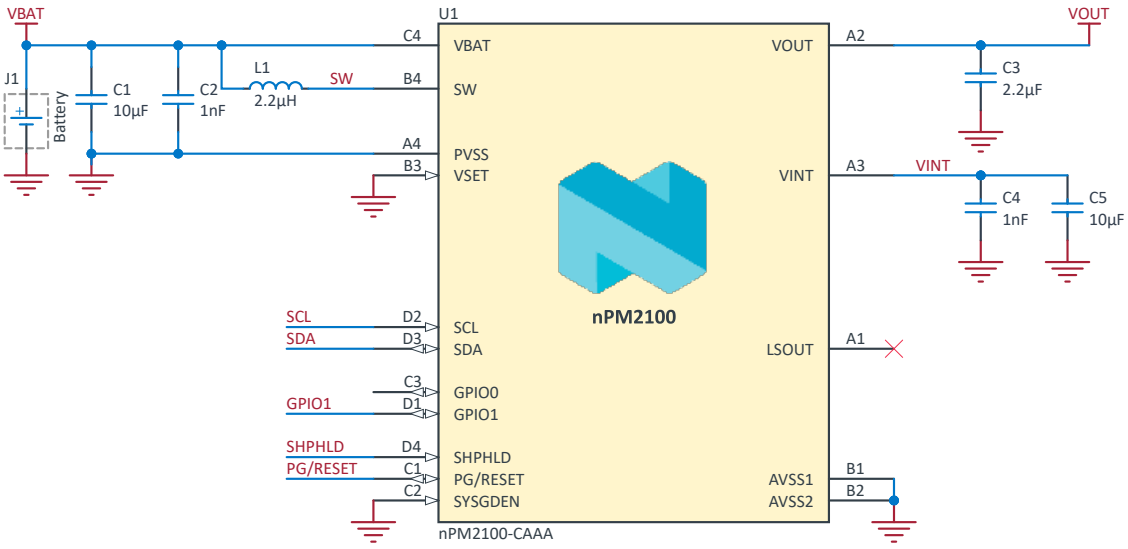


Figure 47: WLCSP schematic for configuration 1

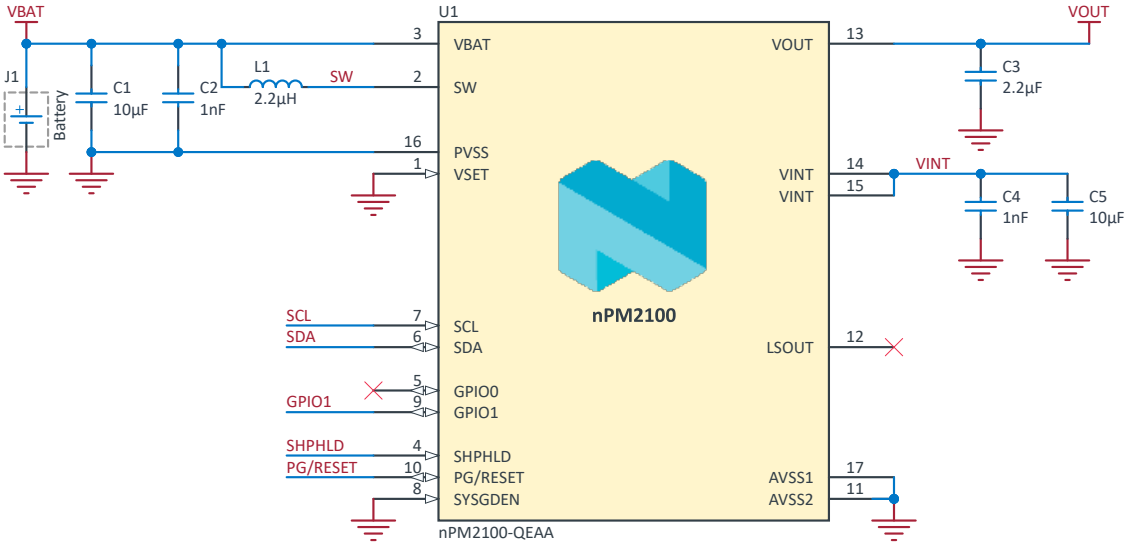


Figure 48: QFN schematic for configuration 1

Designator	Value	Description	Package
C1, C5	10 µF	Capacitor, X5R, 6 V, ±20%	0402
C2, C4	1 nF	Capacitor, X5R	0201
C3	2.2 µF	Capacitor, X5R, 6 V, ±20%	0402
L1	2.2 µH	Inductor, Isat > 0.55 A, DCR < 300 mΩ, ±20%	0603
U1	nPM2100	nPM2100	WLCSP16 or QFN16

Table 26: Bill of material for configuration 1

9.3.2 Configuration 2

The reference schematic for a configuration with a Lithium CR2032 battery is shown here. In this configuration VOUT is set to 3.0 V.

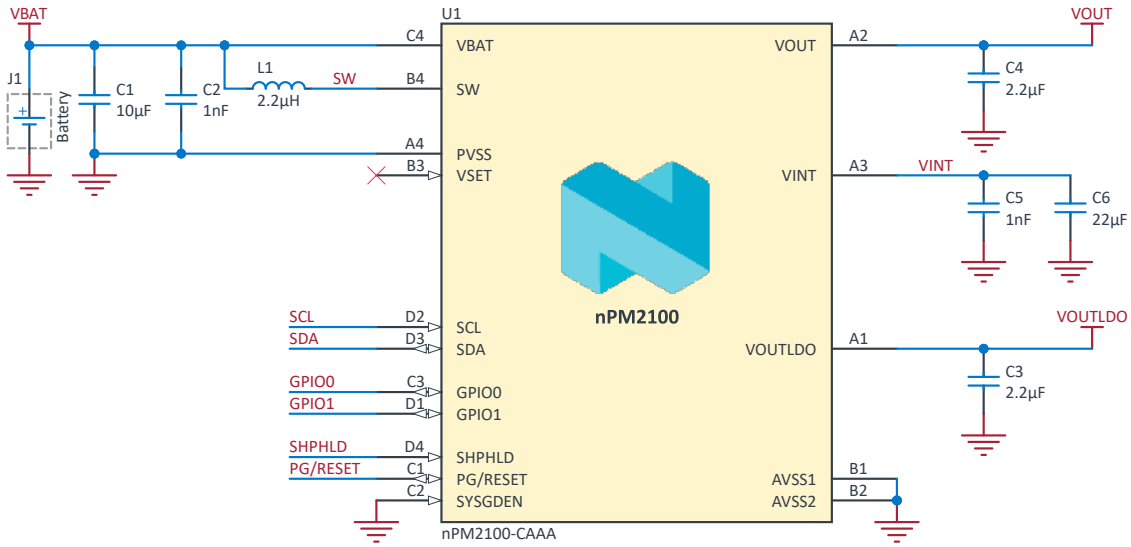


Figure 49: WLCSP schematic for configuration 2

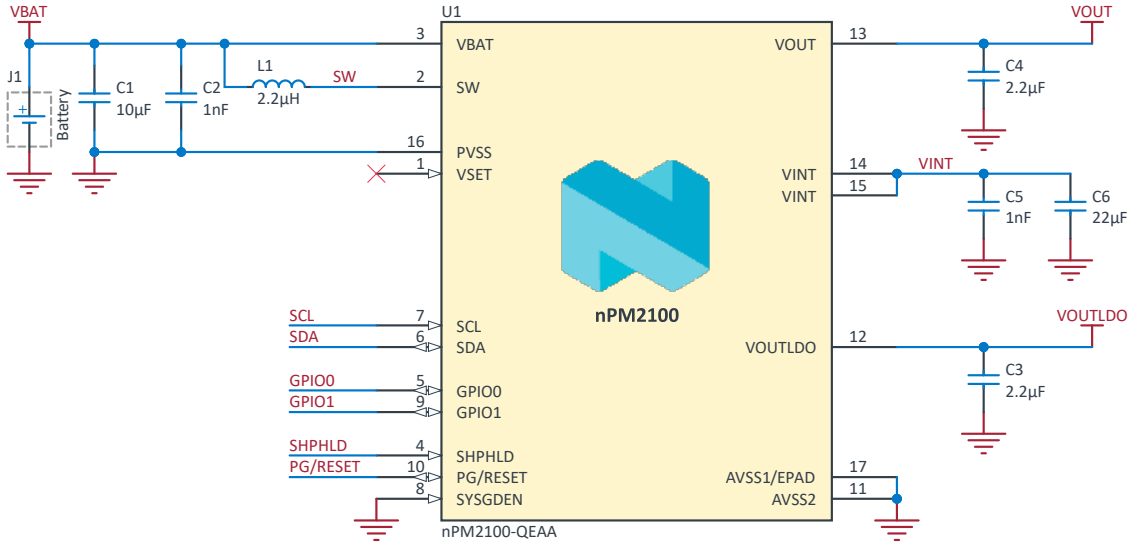


Figure 50: QFN schematic for configuration 2

Designator	Value	Description	Package
C1	10 µF	Capacitor, X5R, 6 V, ±20%	0402
C2, C5	1 nF	Capacitor, X5R	0201
C3, C4	2.2 µF	Capacitor, X5R, 6 V, ±20%	0402
C6	22 µF	Capacitor, X5R, 6 V, ±20%	0402
L1	2.2 µH	Inductor, Isat > 0.55 A, DCR < 300 mΩ, ±20%	0806
U1	nPM2100	nPM2100	WLCSP16 or QFN16

Table 27: Bill of material for configuration 2

9.3.3 PCB guidelines

A well designed PCB is necessary to achieve good performance. A poor layout can lead to loss in performance or functionality.

To ensure functionality, it is essential to follow the schematics and layout references closely.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance.

The DC supply voltage should be decoupled with high performance capacitors as close as possible to the supply pins. See the schematics in Reference circuits for recommended decoupling capacitor values.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the device.

9.3.4 PCB layout example

The PCB layouts shown here are reference layouts for configuration 2.

WLCSP PCB layout

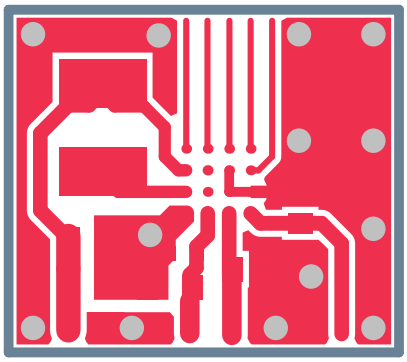


Figure 51: PCB layout, top layer

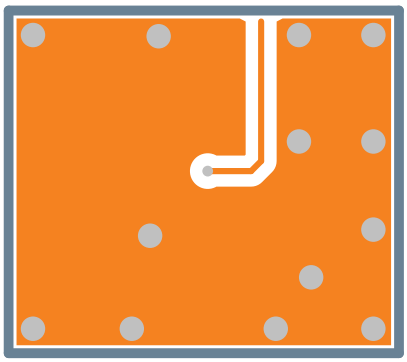


Figure 52: PCB layout, layer 2

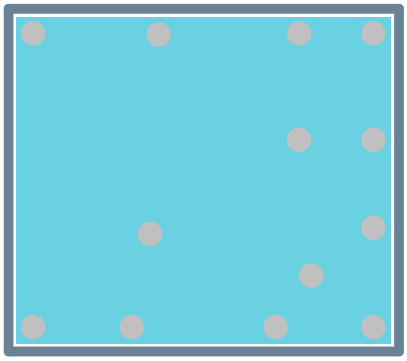


Figure 53: PCB layout, layer 3

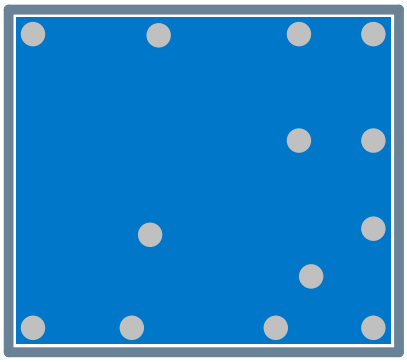


Figure 54: PCB layout, bottom layer

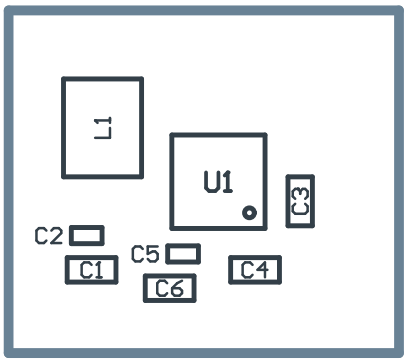


Figure 55: Component placement

QFN PCB layout

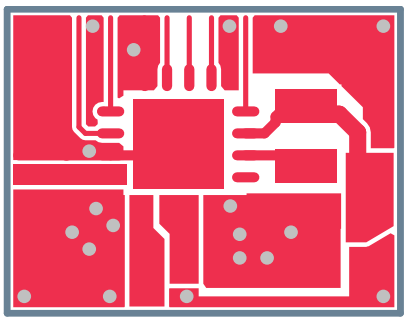


Figure 56: PCB layout, top layer

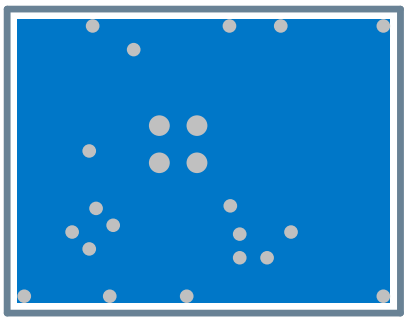


Figure 57: PCB layout, bottom layer

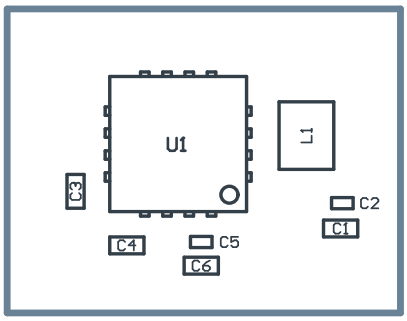


Figure 58: Component placement

10 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

10.1 IC marking

The nPM2100 PMIC package is marked as shown in the following figure.

N	P	M	2	1	0	0
<P	P>	<V	V>	<H>	<P>	
<Y	Y>	<W	W>	<L	L>	

Figure 59: IC marking

10.2 Box labels

The following figures define the box labels used for the nPM2100 device.

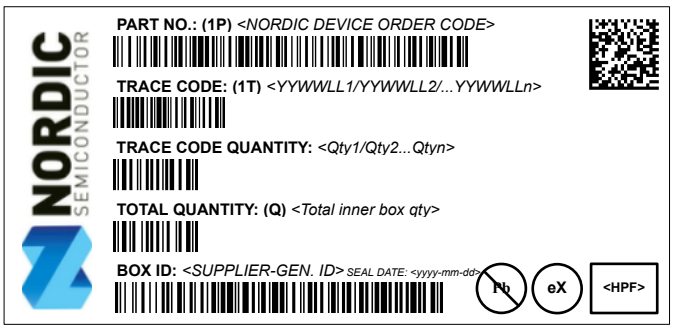


Figure 60: Inner box label

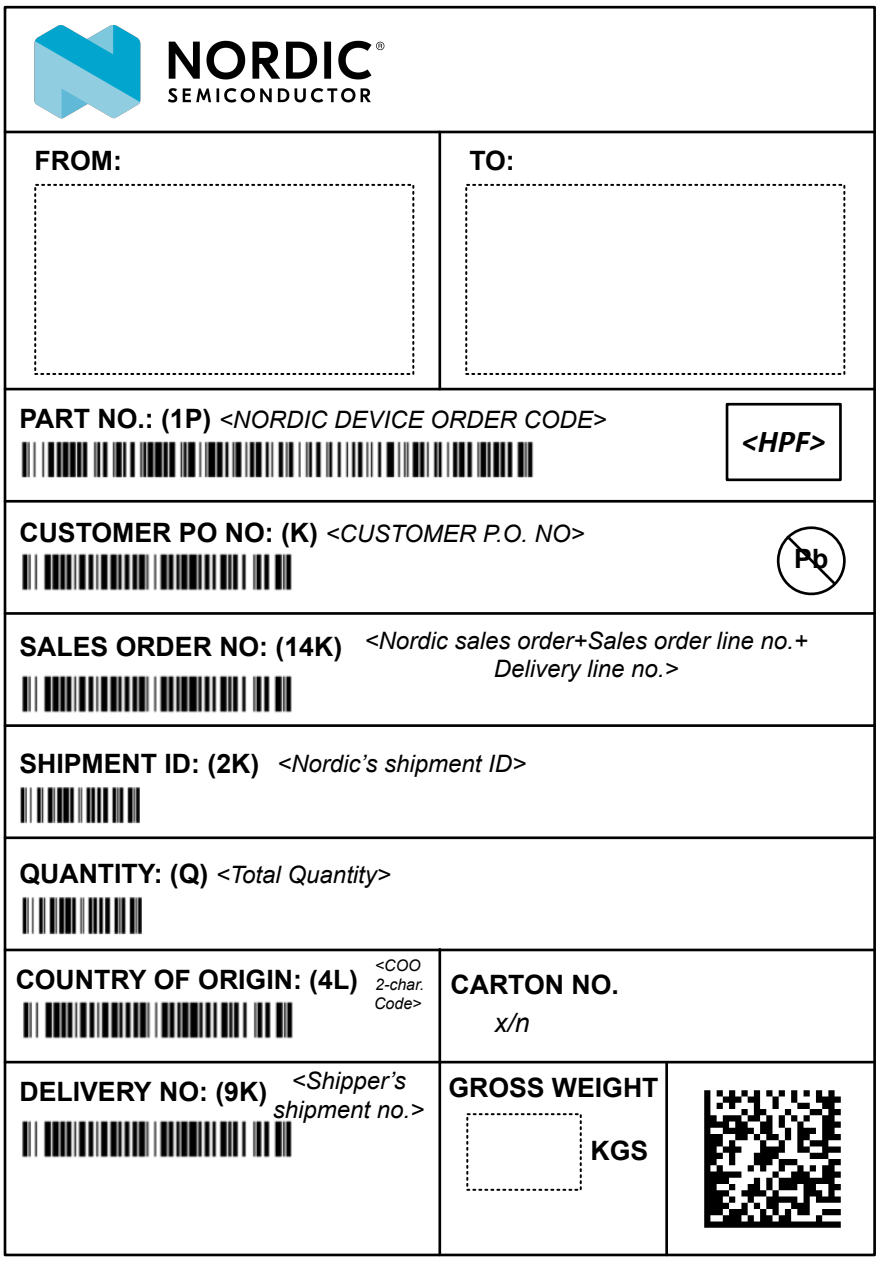


Figure 61: Outer box label

10.3 Order code

The following tables define the nPM2100 order codes and definitions.

n	P	M	2	1	0	0	-	<P	P>	<V	V>	-	<C	C>

Figure 62: Order code

Abbreviation	Definition and implemented codes
N21/nPM21	nPM21 series product
00	Part code
<PP>	Package variant code
<VV>	Function variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code
eX	2nd Level Interconnect Symbol where value of X is based on J-STD-609

Table 28: Abbreviations

10.4 Code ranges and values

The following tables define the nPM2100 code ranges and values.

<PP>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
CA	WLCSP	1.9x1.9	16	0.44
QE	QFN	4.0x4.0	16	0.65

Table 29: Package variant codes

<VV>	Flash (kB)	RAM (kB)
AA	n/a	n/a

Table 30: Function variant codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 31: Hardware version codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 32: Production configuration codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 33: Production version codes

<YY>	Description
[16 . . 99]	Production year: 2016 to 2099

Table 34: Year codes

<WW>	Description
[1 . . 52]	Week of production

Table 35: Week codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 36: Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel

Table 37: Container codes

10.5 Product options

The following tables define the nPM2100 product options.

Order code	MOQ[1]	Comment
nPM2100-CAAA-R7	1500	WLCSP
nPM2100-CAAA-R	7000	WLCSP
nPM2100-QEAA-R7	1500	QFN
nPM2100-QEAA-R	4000	QFN

Table 38: nPM2100 order codes

Order code	Description
nPM2100-EK	Evaluation kit

Table 39: Evaluation tools order code

[1] Minimum Ordering Quantity

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