Motorcomm

YT8011A/AN/AR Datasheet

AUTOMOTIVE 100/1000BASE-T1 TRANSCEIVER

Issue V1.4

Date 2025-12-11

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General Description

The YT8011A/AN/AR is a single-pair Ethernet physical layer transceiver that supports operation over Unshielded Twisted Pair (UTP). The transceiver complies with the Ethernet physical layer portion of 100/1000BASE-T1 as defined by IEEE 802.3bw and the IEEE 802.3bp standard, including auto-negotiation, link-synchronization, and OAM features.

The device supports Reduced Gigabit Media Independent Interface (RGMII) and Serial Gigabit Media Independent Interface (SGMII). YT8011A/AN/AR supports the 3.3V/2.5V/1.8V I/O signal of RGMII, and YT8011A/AN supports the signal of SGMII.

The device supports the SLEEP/WAKE function for the automotive Ethernet. The SLEEP function implements the PHY into sleep mode with lower power consumption. The WAKE function can trigger the PHY to be efficiently woken up to normal operation mode from sleep mode.

The YT8011A/AN/AR uses state-of-the-art mixed-signal technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as adaptive equalization, echo cancellation, data recovery, and error correction are implemented in the YT8011A/AN/AR to provide robust transmission and reception capabilities at 100Mbps, or 1000Mbps. It offers high Electro-Static Discharge (ESD) protection as well as excellent Electromagnetic Compatibility (EMC) performance.

Key Features

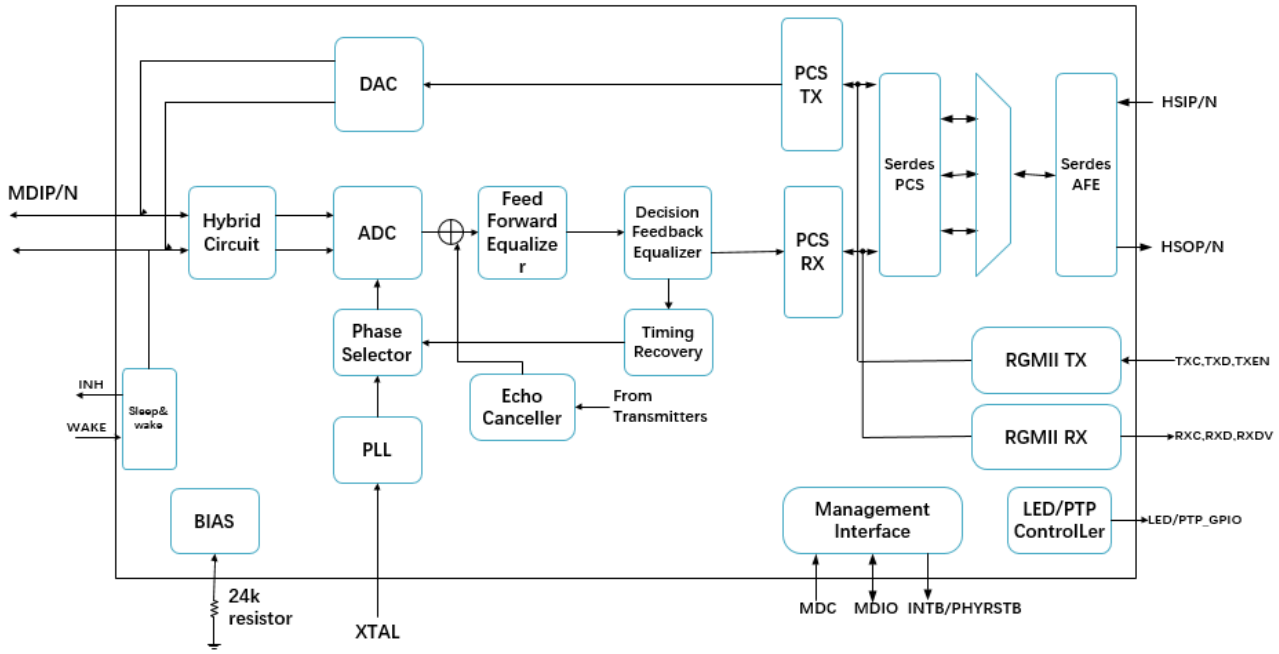
- 100/1000BASE-T1
  - Compliant with 100/1000BASE-T1 defined by IEEE 802.3bw and 802.3bp standards
  - Fast link-up time(<100ms)
  - Support full duplex
  - Support auto-negotiation
  - Link synchronization
- Interface
  - Support RGMII with optional internal delay on TX and RX path and 1.8V/2.5V/3.3V RGMII IO voltage (Only for YT8011A/AN/AR)
  - Support SGMII (Only for YT8011A/AN)
  - MDC/MDIO management interface
  - Interrupt notification
  - PTP GPIO
- Precision Time Protocol (PTP)
  - Support for Precision time protocol, including IEEE1588v1, v2, and 802.1AS
  - PTP packet parser supports layer 2 Ethernet, IPv4/UDP, IPv6/UDP packets
  - Support One-Step operation
  - Adjustable PTP clock for synchronization
  - Deterministic and low transmission latency for the PTP mechanism
  - Programmable time application interface through the PTP GPIO

- Selectable PTP clock input from the external reference clock source

- Clock
  - Support 25MHz crystal/external clock
- Power Saving
  - Support TC10 sleep and wake-up function
  - Low power consumption at sleep mode < 30μA
  - Support remote/local wake-up
- Performance
  - AEC-Q100 Grade 1 (-40°C - 125°C)
  - Low Electro-Magnetic Emission
  - Fully integrated digital adaptive equalizers, echo cancellers
  - Advanced digital baseline wander correction
- Packages
  - YT8011A/AN: 48pin QFN package (7×7)
  - YT8011AR: 40pin QFN package (6×6)

Block Diagram

Figure 1 Block Diagram



System Applications

Figure 2 YT8011A Application Diagram

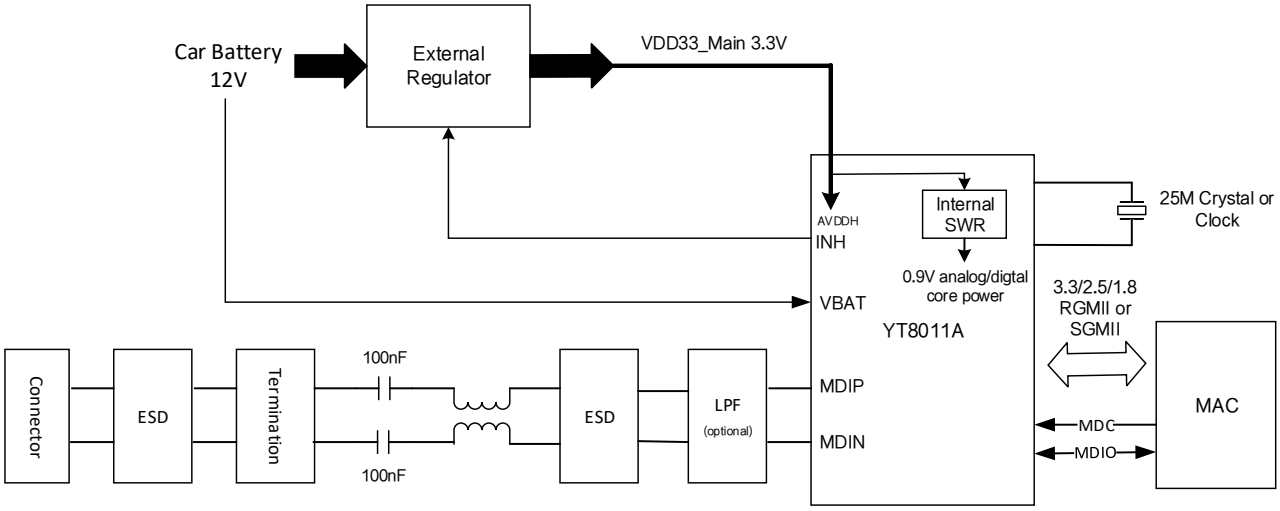


Figure 3 YT8011AN Application Diagram

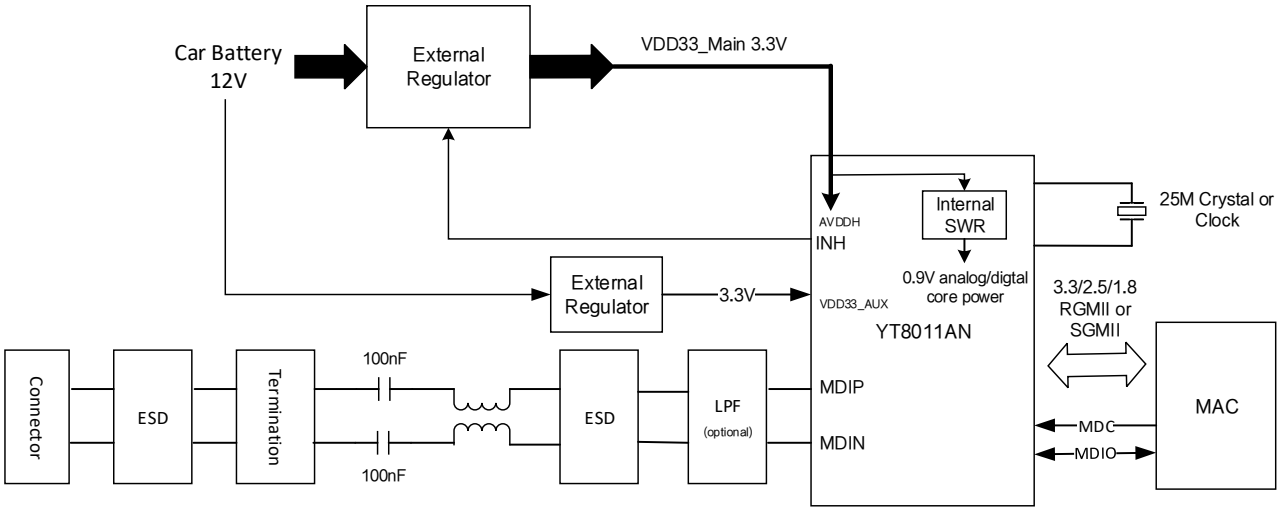
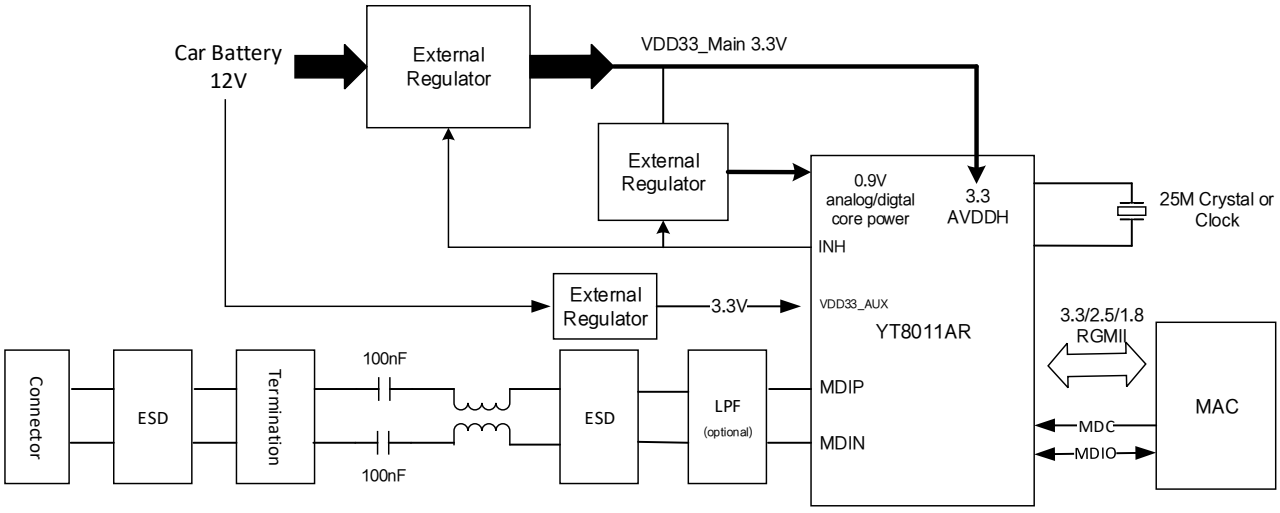


Figure 4 YT8011AR Application Diagram



Note1: YT8011A supports 12V power input on VBAT pin.

Note2: External regulator for VDD33_AUX must be independent relative to the main 3.3V due to TC10 requirement.

Note3: YT8011AR does not support SGMII and SWR. 0.9V core voltage must also come from external sources.

Revision History

Revision	Release Date	Description
V1.4	2025-12-11	• Remove the DLL delay configuration in the RGMII registers, see 4.4 Common EXT Register. • Update the description of parameters in DoS mode, see 5.2.4 RGMII Timing Delay Modes. • Update the note for power ripple in 6.2 Recommended Operating Conditions.
V1.3	2025-02-20	• Update the description of power-related pins, see 1.4.8 Power Related. • Update loopback modes schematic diagrams, see 2.12 Loopback Mode. • Update the schematic diagram in 2.18 Spread Spectrum Clock. • Update the PTP block diagram in 2.20.1 PTP Block. • Update the description of register 0x04, see 4.5.5 Auto-Negotiation Advertisement (0x04). • Update the RGMII timing, see 5.2.3 RGMII Timing Characteristics. • Update the max value of VBAT in 6.1 Absolute Maximum Ratings. • Update the min and max values of Supply Voltage 12V in 6.2 Recommended Operating Conditions. • Delete YT8011AS information.
V1.2	2024-10-24	• Add power off order in 6.3 Power Sequence. • Update Serdes eye diagram mask in 5.2.1 SGMII Differential Transmitter Characteristics. • Add operating state in 2.13 Operating State. • Update register ext2036 in 4.2.7 Loopback Config (0x2036).
V1.1	2024-06-20	• Add YT8011AS information.
V1.0	2024-04-12	• Release Version.
V0.9	2024-03-04	• Update power consumption in 6.4 Power Consumption.
V0.8	2023-11-26	• Update SGMII Characteristics in 5.2 AC Characteristics. • Update Digital IO Characteristics in 5.1 DC Characteristics. • Update the register table description in 4 Register Overview.
V0.7	2023-11-16	• Update AC/DC Characteristics, see 5 Timing and DC/AC Characteristics. • Update block diagram.
V0.6	2023-10-14	• Update AC/DC Characteristics, see 5 Timing and DC/AC Characteristics. • Add sleep/wake, PTP function description, see 2.19 Sleep and Wake Function and 2.20 Precision Time Protocol.
V0.5	2023-08-18	• Update register table in 4 Register Overview. • Add block diagram. • Add 6 Power Requirements and 7 Package Information. • Update Mechanical Information, see 8 Mechanical and Thermal.
V0.4	2023-07-14	• Add register table in 4 Register Overview.
V0.3	2023-05-03	• Add YT8011AN/AR pin assignment &descriptions.
V0.2	2023-01-06	• Change Model name. • Modify VDDL to 0.9V.

Revision	Release Date	Description
		● Update Reset timing. ● Update Pin1,2,3 description. ● Update SWR description. ● Add temperature information.
V0.1	2022-03-29	Draft version

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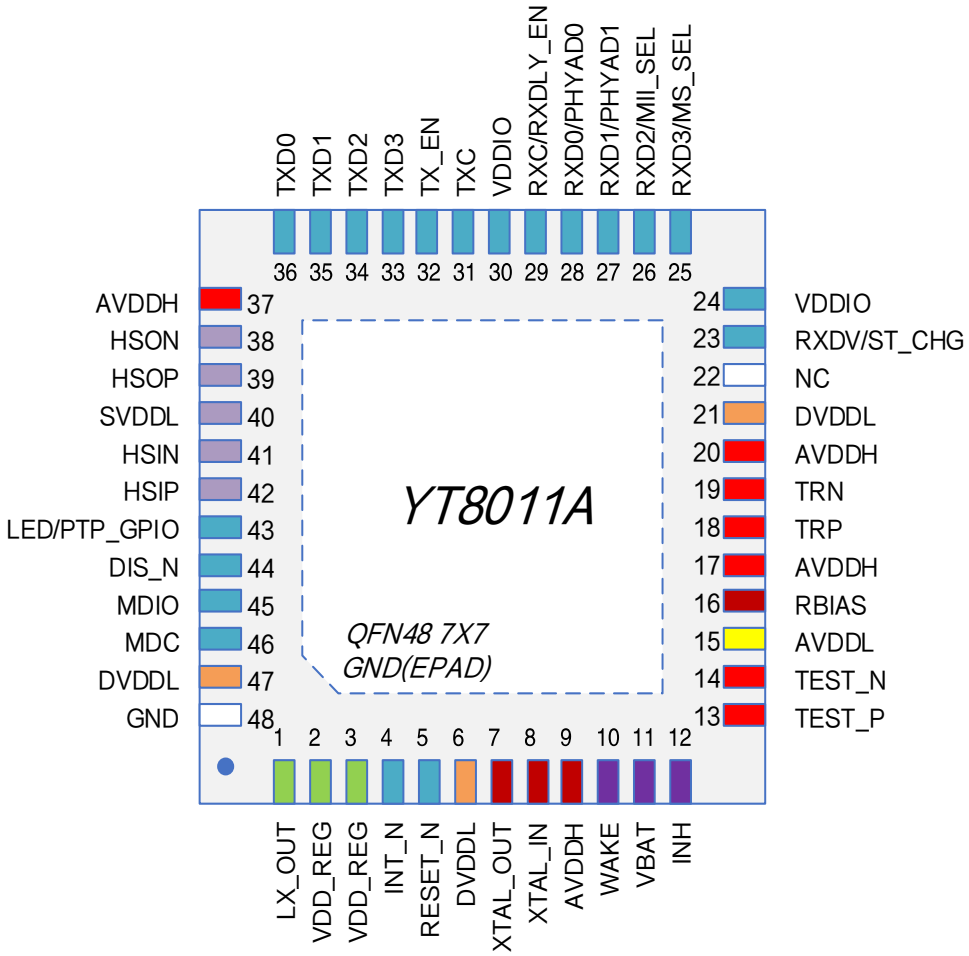
1 Pin Assignment

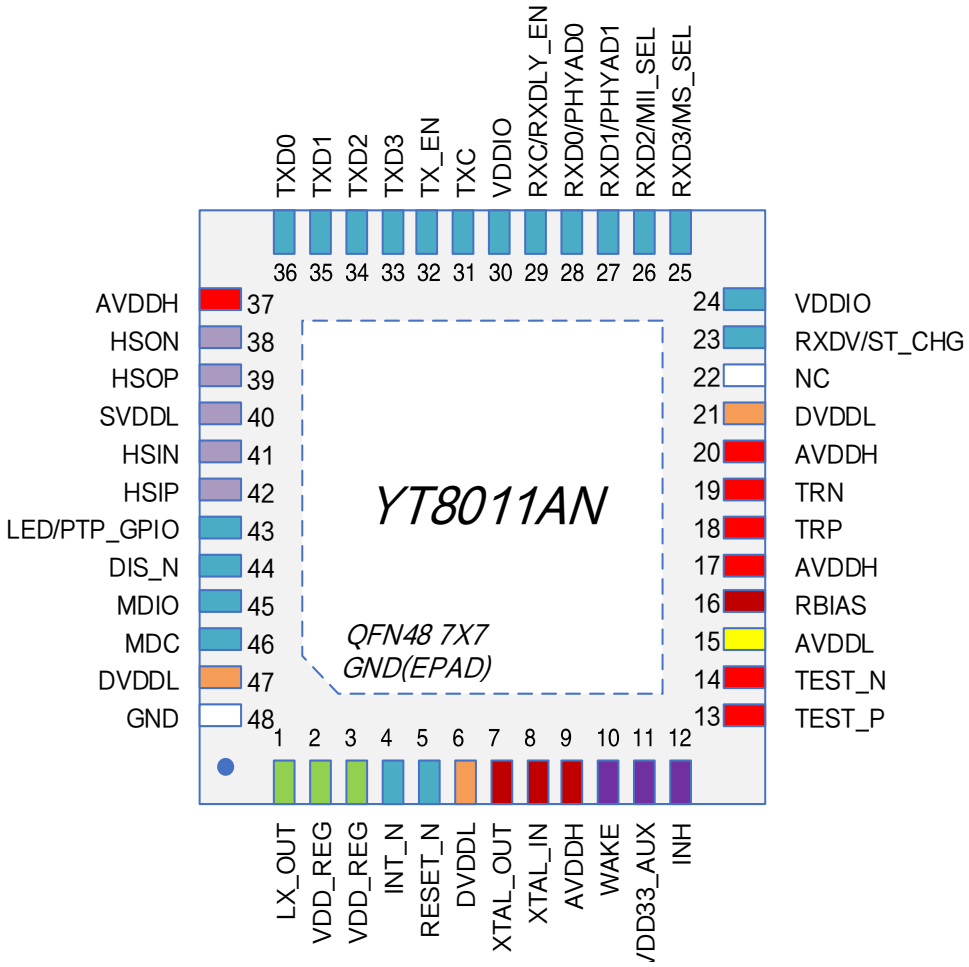
1.1 YT8011A QFN48

Figure 5 YT8011A Pin Map



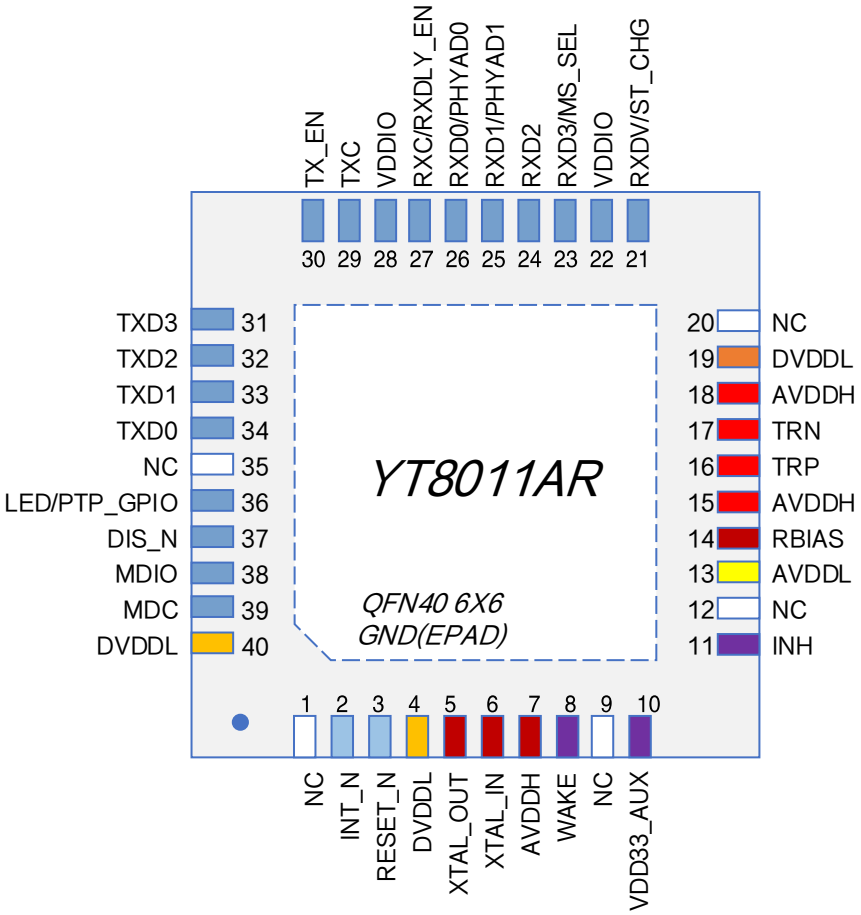
1.2 YT8011AN QFN48

Figure 6 YT8011AN Pin Map



1.3 YT8011AR QFN40

Figure 7 YT8011AR Pin Map



1.4 Pin Descriptions

- I: Input Pin
- AI: Analog Input Pin
- O: Output Pin
- AO: Analog Output Pin
- IO: Bidirectional Input/Output Pin
- AIO: Analog Bidirectional Input/Output Pin
- LI: Latched Input During Power Up or Hardware Reset
- P: Digital Power Pin
- AP: Analog Power Pin
- G: Digital Ground Pin
- AG: Analog Ground Pin
- PD: Internal Pull-Down
- PU: Internal Pull-Up
- SP: SerDes Power Pin
- SG: SerDes Ground Pin
- OD: Open Drain
- XT: Crystal Related

1.4.1 Transceiver Interface

Table 1 Transceiver Interface

No.	Model Name	Pin Name	Type	Description
18	YT8011A	TRP	AIO	Media-dependent interface, 100Ω transmission line
18	YT8011AN			
16	YT8011AR			
19	YT8011A	TRN	AIO	Media-dependent interface, 100Ω transmission line
19	YT8011AN			
17	YT8011AR			

1.4.2 Clock

Table 2 Clock

No.	Model Name	Pin Name	Type	Description
8	YT8011A	XTAL_IN	XT	25MHz Crystal Input pin. When connecting an external 25MHz oscillator or clock from another device to the XTAL_I pin, keep the XTAL_O floating.
8	YT8011AN			
6	YT8011AR			
7	YT8011A	XTAL_OUT	XT	25MHz Crystal Output pin. When connecting an external 25MHz oscillator or clock from another device to the XTAL_O pin, XTAL_I must be shorted to GND.
7	YT8011AN			
5	YT8011AR			

1.4.3 RGMII

Table 3 RGMII

No.	Model Name	Pin Name	Type	Description
33	YT8011A	TXD3	I/PD	Transmit Data. Data is transmitted from MAC to PHY via TXD[3:0].
33	YT8011AN			
31	YT8011AR			
34	YT8011A	TXD2	I/PD	
34	YT8011AN			
32	YT8011AR			
35	YT8011A	TXD1	I/PD	
35	YT8011AN			
33	YT8011AR			
36	YT8011A	TXD0	I/PD	
36	YT8011AN			
34	YT8011AR			
32	YT8011A	TX_EN	I/PD	Transmit Control Signal from the MAC.
32	YT8011AN			

No.	Model Name	Pin Name	Type	Description
30	YT8011AR			
31	YT8011A	TXC	I/PD	The transmit reference clock will be 125MHz, or 25MHz, depending on speed.
31	YT8011AN			
29	YT8011AR			
25	YT8011A	RXD3/MS_SEL	O/LI/PD	Receive Data. Data is transmitted from PHY to MAC via RXD[3:0]. ● RXD3/MS_SEL pin is the Power On Strapping for Master/slave Mode. 1: Master mode 0: Slave mode ● RXD2/MII_SEL pin is the Power On Strapping for SGMII/RGMII Mode. 1: SGMII mode 0: RGMII mode ● RXD1/PHYAD1, RXD0/PHYAD0 are Power On Strapping for PHY Address. PHY Address[1:0] Configuration: 2'b00: 0x0 2'b01: 0x1 (default) 2'b10: 0x2 2'b11: 0x3
25	YT8011AN			
23	YT8011AR			
26	YT8011A	RXD2/MII_SEL	O/LI/PD	
26	YT8011AN			
24	YT8011AR			
27	YT8011A	RXD1/PHYAD1	O/LI/PD	
27	YT8011AN			
25	YT8011AR			
28	YT8011A	RXD0/PHYAD0	O/LI/PU	
28	YT8011AN			
26	YT8011AR			
29	YT8011A	RX_CLK/ RXDLY_EN	O/LI/PU	The continuous receive reference clock will be 125MHz, or 25MHz, derived from the received data stream. RX_CLK/RXDLY_EN is the Power On Strapping for the delay to RXC for RXD latching: 1'b1: Add the delay to RXC for RXD latching. 1'b0: No delay to RXC for RXD latching.
29	YT8011AN			
27	YT8011AR			
23	YT8011A	RX_DV/ ST_CHG	O/LI/PU	Receive Control Signal to the MAC. Operating modes state change condition configuration: ● 1'b1: Auto mode (default) The PHY goes to normal mode automatically. When the device is powered on, waked up, or driven RESET_N pin from low to high. ● 1'b0: Manual mode The PHY goes to normal mode manually. When the device is powered on, waked up, or driven RESET_N pin from low to high.
23	YT8011AN			
21	YT8011AR			

1.4.4 SerDes

Table 4 SerDes

No.	Model Name	Pin Name	Type	Description
42	YT8011A	HSIP	AI	SerDes Differential Input: 1.25GHz serial interfaces to receive data from an External device that supports the SGMII interface.
42	YT8011AN			
41	YT8011A	HSIN	AI	

No.	Model Name	Pin Name	Type	Description
41	YT8011AN			The differential pair has an internal 100Ω termination resistor.
39	YT8011A	HSOP	AO	SerDes Differential Output: 1.25GHz serial interfaces to transfer data to an External device that supports the SGMII interface. Both HSOP and HSON have an internal 50Ω termination resistor to SVDDL, which means the differential impedance is 100Ω.
39	YT8011AN			
38	YT8011A	HSON	AO	
38	YT8011AN			

1.4.5 LED/PTP Default Settings

Table 5 LED/PTP Default Settings

No.	Model Name	Pin Name	Type	Description
43	YT8011A	LED/PTP_GPIO	O (LED)/ IO (PTP_GPIO)	• LED (default High Level) • PTP GPIO • PTP clock input from the external reference clock source. • GPIO Output
43	YT8011AN			
36	YT8011AR			

1.4.6 Test P/N

Table 6 Test P/N

No.	Model Name	Pin Name	Type	Description
13	YT8011A	Test_P	O	Test pin (Differential signal). This pin must be floating
13	YT8011AN			
14	YT8011A	Test_N	O	Test pin (Differential signal). This pin must be floating
14	YT8011AN			

Note: YT8011AR does not support Test_P and Test_N, which may cause the master and slave transmit clock jitter untestable. Pay attention to the MDI jitter test item and system packet loss verification.

1.4.7 Management and Control Interface

Table 7 Management and Control Interface

No.	Model Name	Pin Name	Type	Description
46	YT8011A	MDC	I/PD	Management Data Clock.
46	YT8011AN			
39	YT8011AR			
45	YT8011A	MDIO	IO/PU	Input/Output of Management Data.
45	YT8011AN			
38	YT8011AR			
44	YT8011A	DIS_N	I/PD	

No.	Model Name	Pin Name	Type	Description
44	YT8011AN			Disable packet transmission and MDIO will be read-only. Active low.
37	YT8011AR			
4	YT8011A	INT_N	O/OD	Interrupt/Output of management data. **Note:** pull up to VDDIO.
4	YT8011AN			
2	YT8011AR			
5	YT8011A	RESET_N	I/PU	Hardware reset, active low. Requires an external pull-up resistor. **Note:** pull up to VDDIO.
5	YT8011AN			
3	YT8011AR			
10	YT8011A	WAKE	I	Local wake-up input.
10	YT8011AN			
8	YT8011AR			
12	YT8011A	INH	O	Output low when PHY is in sleep mode.
12	YT8011AN			
11	YT8011AR			
16	YT8011A	RBIAS	I	Bias resistor. A 24k 1% resistor is connected between the RBIAS pin and GND.
16	YT8011AN			
14	YT8011AR			

1.4.8 Power Related

Table 8 Power Related

No.	Model Name	Pin Name	Type	Description
1	YT8011A	LX_OUT	P/O	Switching Regulator out. ● When using the internal SWR power supply for 0.9V, Pin1 is externally connected to 2.2μH inductor + 22μF and 0.1μF capacitors. ● When using the external power supply for 0.9V, keep this pin floating.
1	YT8011AN			
2, 3	YT8011A	VDD_REG	P/I	This pin should be connected to main power 3.3V. ● When using the internal SWR power supply for 0.9V, connect to 3.3V power, Pin2 is externally connected to 22μF and 0.1μF capacitors, and Pin3 is externally connected to 0.1μF capacitors. ● When using the external power supply for 0.9V, keep this pin floating.
2, 3	YT8011AN			
11	YT8011A	VBAT	P/I	Connect to 3.3V/12V, cannot float. ● If you need TC10 sleep wake-up, connect it to a 3.3V/12V constant power supply. ● If you do not need TC10 sleep wake-up, connect it to a 3.3V/12V controlled power supply.
11	YT8011AN	VDD33_AUX	P/I	

No.	Model Name	Pin Name	Type	Description
10	YT8011AR			This pin should be connected to independent power 3.3V, cannot float. ● If you need TC10 sleep wake-up, connect it to a 3.3V constant power supply. ● If you do not need TC10 sleep wake-up, connect it to a 3.3V controlled power supply.
6, 21, 47	YT8011A	DVDDL	P/I	Digital core power 0.9V, cannot float. If the internal SWR provides 0.9V, DVDDL is the internal SWR feedback point, and no magnetic beads can be added between LX_OUT and DVDDL.
6, 21, 47	YT8011AN			
4, 19, 40	YT8011AR			
9, 17, 20, 37	YT8011A	AVDDH	P/I	Analog Power 3.3V. It is powered by an external 3.3V power supply and connected to a 3.3V controlled power supply; it cannot float.
9, 17, 20, 37	YT8011AN			
7, 15, 18	YT8011AR			
15	YT8011A	AVDDL	P/I	Analog power 0.9V, cannot float.
15	YT8011AN			
13	YT8011AR			
40	YT8011A	SVDDL	P/I	Serdes power 0.9V, cannot float.
40	YT8011AN			
24, 30	YT8011A	VDDIO	P/I	I/O PAD power, support 3.3V/2.5V/1.8V, cannot float. RGMII, MDC/MDIO, INT_N, LED, DIS_N, RESET_N interface power supply, use an external 3.3V/2.5V/1.8V power supply for power according to level requirements.
24, 30	YT8011AN			
22, 28	YT8011AR			
48	YT8011A	GND	G	GND
48	YT8011AN			
49	YT8011A	EPAD	G	GND
49	YT8011AN			
41	YT8011AR			
22	YT8011A	NC	-	Keep floating.
22	YT8011AN			
1, 9, 12, 20, 35	YT8011AR			

2 Function Description

2.1 Transmitter

2.1.1 1000BASE-T1

In 1000BASE-T1 mode, YT8011A/AN/AR scrambles transmit data bytes from the MAC interfaces and encodes them into 2D-PAM3 signals. Signals are transmitted onto the 1-twisted pair at 750M Baud/s.

2.1.2 100BASE-T1

In 100BASE-T1 mode, YT8011A/AN/AR scrambles transmit data bytes from the MAC interfaces and encodes them into 2D-PAM3 signals. Signals are transmitted onto the 1-twisted pair at 66.7M Baud/s.

2.2 Receiver

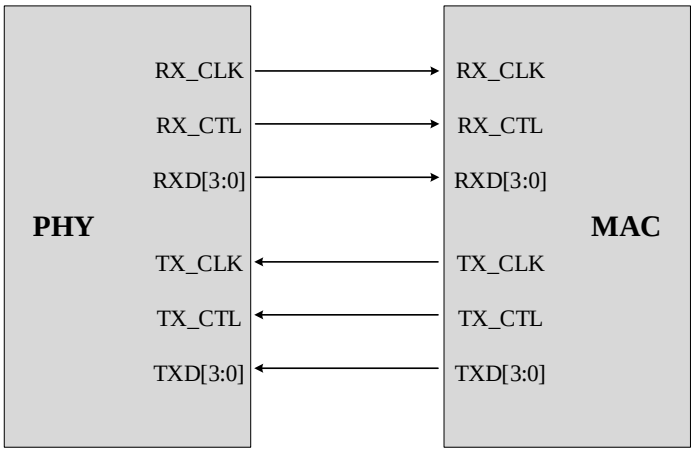
YT8011A/AN/AR receives signals from the media. A hybrid circuit is used to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalizer, Baseline Wander (BLW) canceller, echo canceller, clock recovery, and 2D-PAM3 decoding.

2.3 RGMII Interface

RGMII is a standard interface between MAC and PHY, which is used to connect a PHY to a MAC. It is a parallel bus by clocking data on both the rising and falling edges of the clock. The clock frequency is adaptive to the speed of MAC and PHY link speed so that it can work in 1000/100/10Mbps modes. For YT8011A/AN/AR, RGMII works at 1000/100Mbps mode since it only supports 1000/100BASE-T1.

- For 1000M applications, TX_CLK and RX_CLK are 125MHz.
- For 100M applications, TX_CLK and RX_CLK are 25MHz.

Figure 8 Connection Diagram of RGMII



OPEN RGMII interface definition supports two delay modes:

- Delay on Destination (DoD), in which clock, data, and control signal are transferred edge-aligned. The delay of the clock signal must be accomplished by the receiver device.
- Delay on Source (DoS), in which the transmitter device already provides a delayed clock signal.

2.4 SGMII Interface

SGMII is a standard interface between MAC and PHY. The data bit width is 1 bit, and there is a pair of differential signal lines for transmission and reception. Signals operate at 1.25G/baud and 8b/10b encoding on the serial data.YT8011A/AN supports the SGMII interface in 1000/100BASE-T1 mode.

2.5 Management Interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22, and also support MDC clock rates up to 12.5MHz.

2.6 DAC

The Digital-to-Analog Converter (DAC) transmits PAM3, and Differential Manchester Encoding (DME). The transmit DAC performs signal wave shaping that reduces Electromagnetic Interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation.

2.7 ADC

The receive channel has its own Analog-to-Digital Converter (ADC) that samples the incoming data on the receive channel and loops the output to the digital data path.

2.8 Adaptive Equalizer

The digital adaptive equalizer removes Inter-Symbol Interference (ISI) created by the channel. The equalizer accepts sampled data from the ADC on each channel and produces equalized data. The coefficients of the equalizer are adaptive to accommodate varying conditions of cable quality and cable length.

2.9 Echo-Canceller

The echo impairment is caused on each channel because of the bidirectional transceiver in 1000/100BASE-T1 mode. An echo canceller is added to remove this impairment from the ADC output. The echo canceller coefficients are adaptive to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

2.10 Clock Recovery

The clock recovery block creates the transmit and receive clocks for 1000/100BASE-T1. The two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmits and receives clocks are locked to the 25MHz crystal input. The slave

transmits and receives clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo.

2.11 Polarity Detection and Auto-Correction

YT8011A/AN/AR can detect and correct the swapping of wires within a pair in Slave mode. Polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on the pair. The polarity becomes unlocked only when the receiver loses the lock.

2.12 Loopback Mode

YT8011A/AN/AR supports four loopback modes：

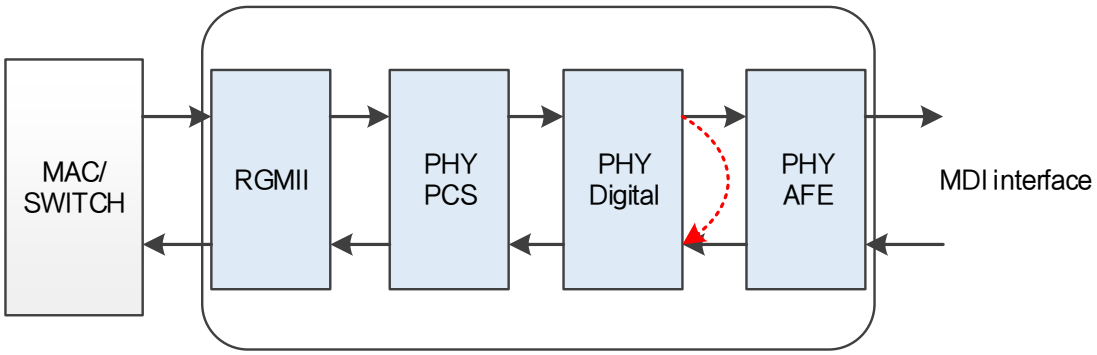
- Internal Loopback
- External Loopback
- Remote Loopback
- PCS Loopback

2.12.1 Internal Loopback

In Internal loopback mode, YT8011A/AN/AR loops transmit data to the receive path in the chip.

Configure bit 14 of the mii register (address 0x0) to enable internal loopback mode. For 1000/100BASET1, YT8011A/AN/AR loops digital PCS transmit data to PCS receiver directly.

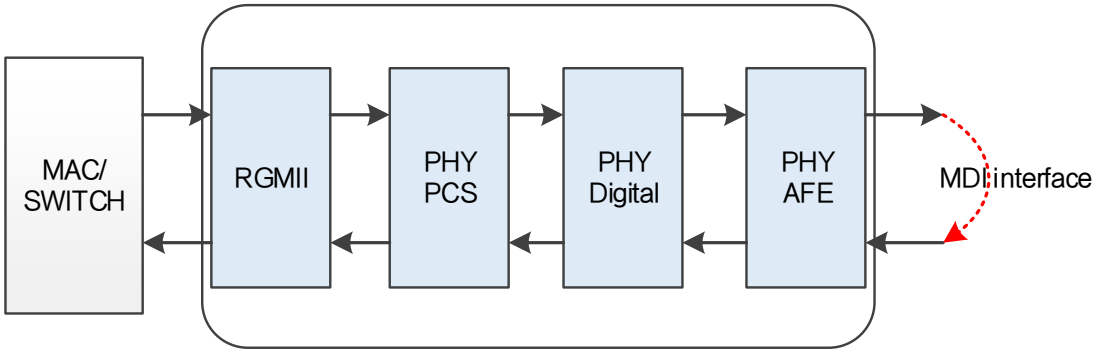
Figure 9 Internal Loopback



2.12.2 External Loopback

In external loopback mode, YT8011A/AN/AR loops transmit data to the receive path out of the chip. For 1000/100BASE-T1, configure bit 1 of the extended register (address 0x2036) to enable the external loopback and just leave TRP/TRN floating.

Figure 10 External Loopback

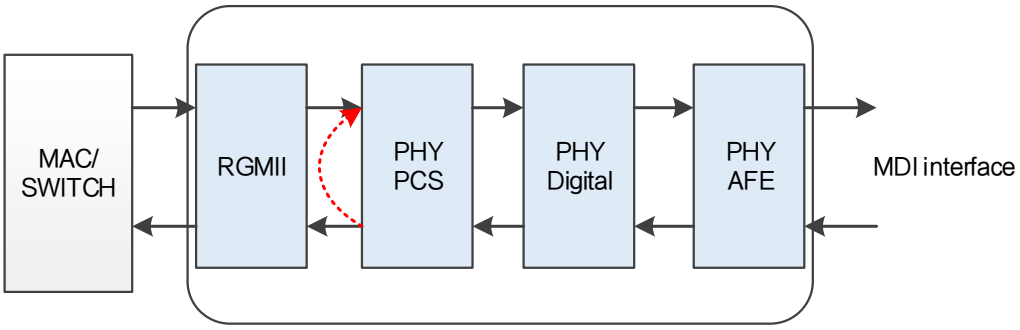


Note: If the reflected signal is too strong for external loopback, the signal may be unstable, you can turn on the echo canceller for the external loopback test (address 0x2036.bit2).

2.12.3 Remote Loopback

In remote loopback mode, YT8011A/AN/AR loops MII receive data to the transmit path in the chip. Configure bit 11 of the extended register (address 0x9030) to enable the remote loopback and TRX interface just connect to the link partner normally.

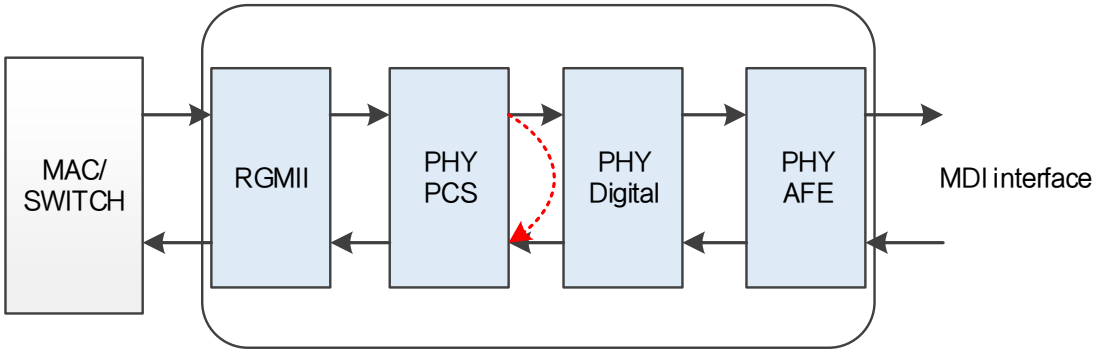
Figure 11 Remote Loopback



2.12.4 PCS Loopback

In PCS loopback mode, YT8011A/AN/AR loops PCS-TX data to the PCS-RX path in the chip. Configure bit 14 of mmd3 register (address 0x900) to enable the PCS loopback and TRX interface just connect to the link partner normally.

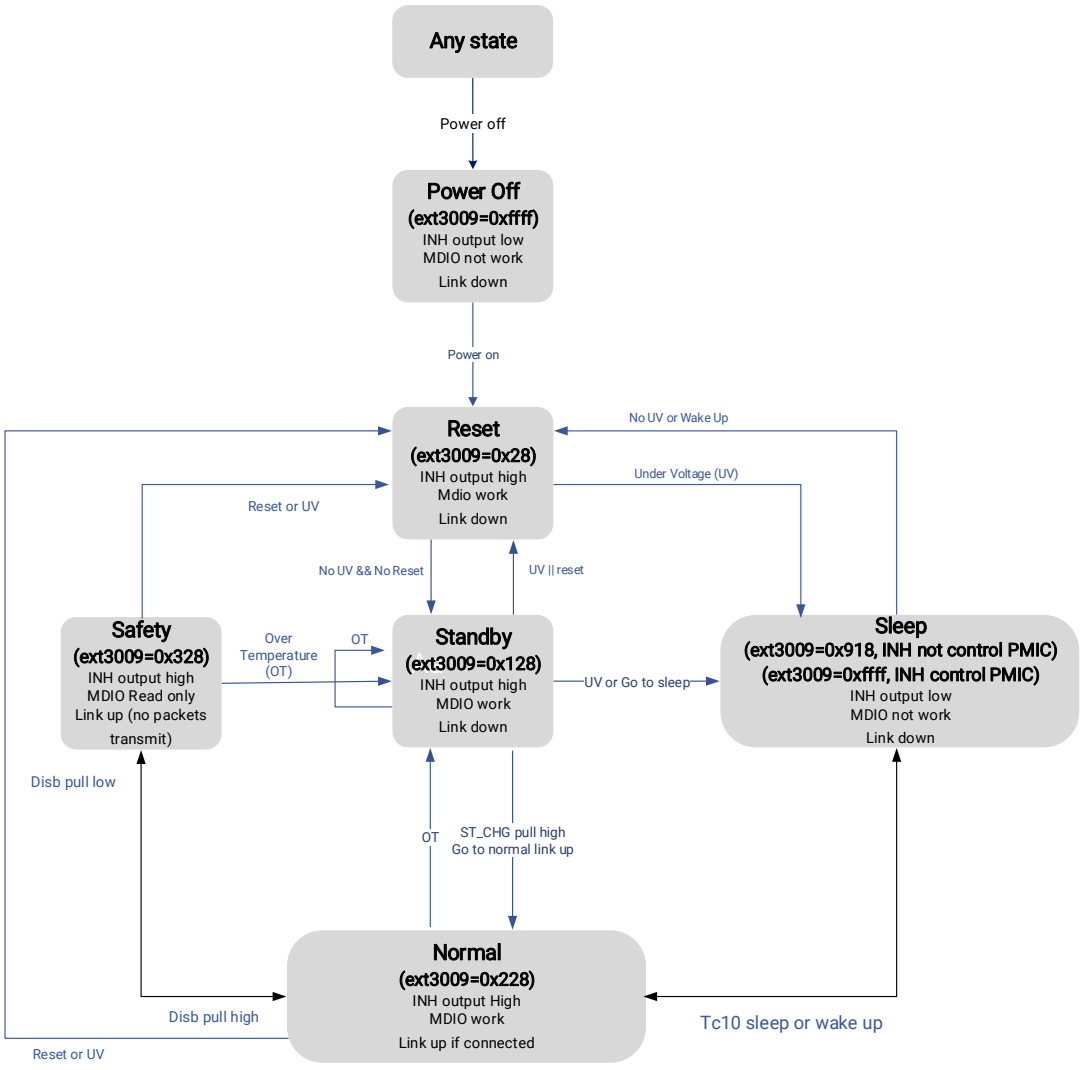
Figure 12 PCS Loopback



2.13 Operating State

YT8011A/AN/AR supports various modes, including power-off, reset, safety, normal, standby and sleep modes. The following state diagram illustrates the transition process between states.

Figure 13 Operating State



For more information on the Under Voltage (UV) and Over Temperature (OT) threshold, refer to 5.1 DC Characteristics and 5.3 Over Temperature Protection.

2.14 Interrupt

YT8011A/AN/AR provides an active low interrupt output pin (INT_N) based on the change of PHY status. Every interrupt condition is represented by the read-only general interrupt status register. The interrupts can be individually enabled or disabled by setting or clearing bits in the Interrupt Mask Register. The interrupt of the YT8011A/AN/AR is a level-triggered mechanism.

2.15 Master and Slave Configuration

Master and slave configuration is from hardware strapping or configured by bit 12 of the MMD register (address mmd1 0x834). The master-slave configuration works for both 1000BASE-T1 and 100BASE-T1 modes.

Table 9 Mode Configuration

Mode	Register Configuration
1000T1 Master	write mmd1 0x834 0xc001
1000T1 Slave	write mmd1 0x834 0x8001
100T1 Master	write mmd1 0x834 0xc000
100T1 Slave	write mmd1 0x834 0x8000

2.16 Signal Quality Indexes

YT8011A/AN/AR provides methods to monitor the quality of link. It is divided into two parts:

- Dynamic Channel Quality (DCQ)

  DCQ contains Mean Square Errors (MSE) and Signal Quality Index (SQI).

  The information for the Signal Quality Index can be obtained by reading the correspondent register address when the link is elected. Therefore, the SQI latch register is available to read the status of link ok, remote ok, local ok, scramble ok, pcs state, equalizer errors, maximum error, Signal-to-Noise Ratio (SNR), and ADC peak value simultaneously without any timing delay. YT8011A/AN/AR provides two SQIs to indicate real-time MDI signal quality information.

- Link Quality (LQ)

  LQ contains Link Training Time (LTT), Local Receiver Time (LRT), Remote Receiver Time (RRT), and Link Failures and Losses (LFL).

Table 10 SQI Register Table

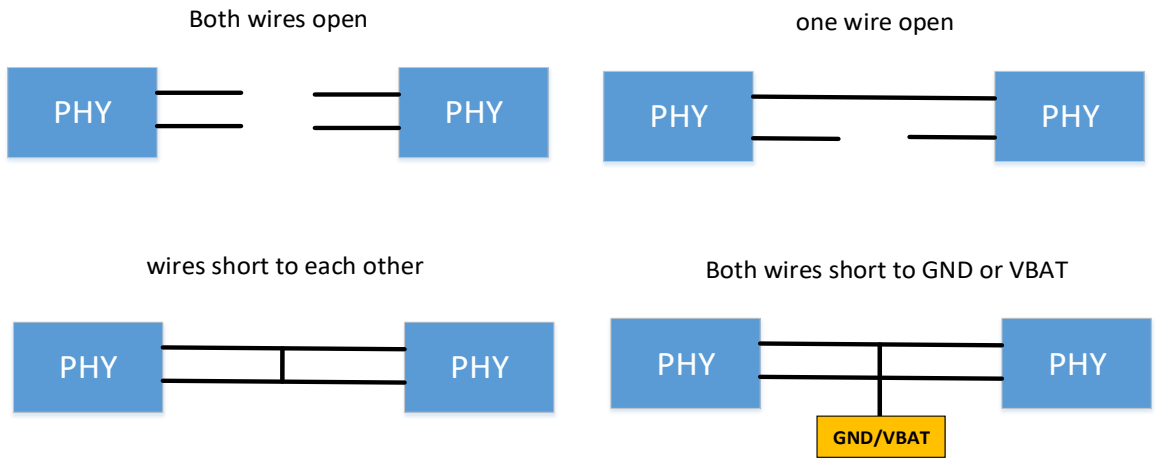
DCQ and LQ	Description
Mean Square Error (MSE)	Enter debug mode by register (write ext 0x1004 0x11ff). Read ext 0x20a0, ext 0x20a1.
Signal Quality Index (SQI)	Read ext 0x3074[2:0], SQI rank from 0 to 7.
Link Training Time (LTT)	Read ext 0x9081[10:0].
Local Receiver Time (LRT)	Read ext 0x9082[7:0].
Remote Receiver Time (RRT)	Read ext 0x9083[7:0].

DCQ and LQ	Description
Link Failures and Losses (LFL)	Link Failures counter (only 100T1), Read ext 0x9086[15:6]. Link Loss counter, Read ext 0x9086[5:0].

2.17 Cable Status Diagnostics

YT8011A/AN/AR provides a method to detect the cable status, which is described as Cable Status Diagnostics (CSD). YT8011A/AN/AR supports CSD no matter what the Master/Slave role setting is. When the PHY enters the CSD process, it transmits the cable detecting sequence rather than the normal signal. There are three cable statuses that can be detected and shown in the register: Normal, Open, and Short. If the cable is not diagnosed as Normal status, the position of the abnormal point can be indicated through the register. The following diagram shows cable status in the YT8011A/AN/AR.

Figure 14 Use Cases of Cable Status Diagnostics

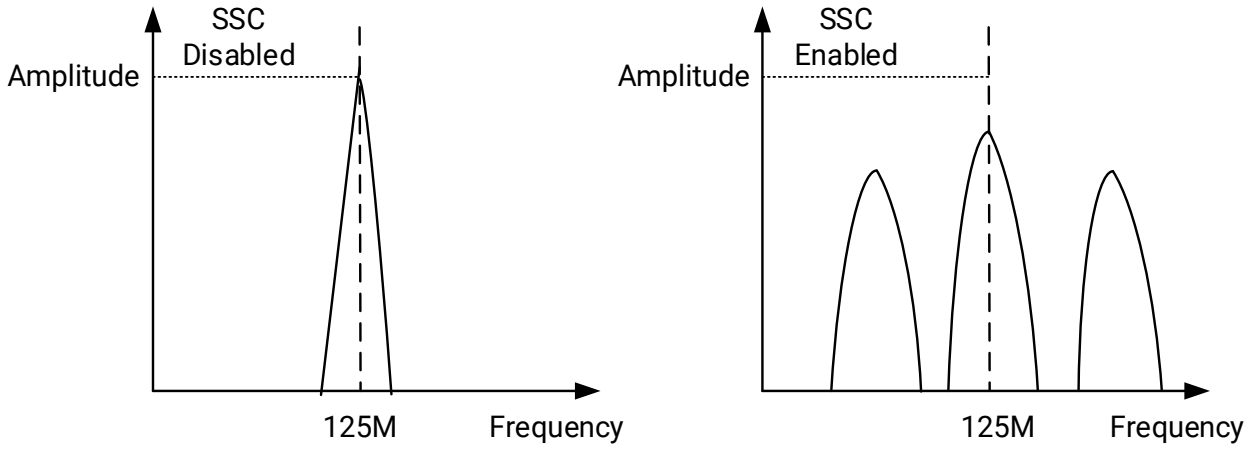


2.18 Spread Spectrum Clock

YT8011A/AN/AR supports Spread Spectrum Clock (SSC) on RGMII Clock (RXC). SSC spreads the signal over a wider bandwidth, reducing the peak radiant energy at RXC frequency, and reducing unnecessary EMI noise. YT8011A/AN/AR supports 7 levels SSC.

Note: The SSC function is disabled in YT8011A/AN/AR by default, and it will bring some variation in IPG length.

Figure 15 Spread Spectrum Clock



2.19 Sleep and Wake Function

YT8011A/AN/AR supports Sleep and wake function for automotive Ethernet based on OPEN Alliance TC10 Sleep/Wake-up. It supports a controlled link shutdown and a fast global wake-up within an Ethernet network. The sleep flow is successful if both PHYs finish sleep handshaking (transmitted and received sleep request signal) properly and enter the Sleep state. Also, the PHY can reject the sleep flow and stay in Normal operation mode. After PHY enters Sleep mode, it can be woken up by detecting a “local wake-up” event on the WAKE pin or a “remote wake-up” on MDI.

2.19.1 Sleep Function

2.19.1.1 Initial Setting

For a sleep initiator or sleep responder, enabling the sleep flow function requires the following steps.

1 Enable sleep capability (ext 0x3008[1]), and additionally enable OAM advertisement mmd1 0x902[1]) for 1000BASE-T1.

2 Set the PHY to re-establish the link. (write mii0x0[bit15] = 1 to software reset) to allow the Sleep capability to take effect.

Note: The MDI link will be re-established after the software reset, and the Sleep flow can only be started when the link between PHY and its link partner is active.

2.19.1.2 Sleep Flow for the Sleep Initiator

- Sleep Request

  If MAC wants the PHY to be the initiator of the Sleep flow, it should send a Sleep request to the PHY (Write ext 0x3008[4] = 1).

- Check Sleep Fail Interrupt

  After sending a Sleep request to the PHY, the MAC should observe whether it receives an interrupt (Read mii0x17[3]). If the readout value is 1, that indicates the sleep fail event occurred. A sleep fail event happens when the link partner does not respond to a sleep request.

- Check Sleep Success

If there is no Sleep fail interrupt, the MAC should check whether the Sleep flow is successful or not. To check, you can choose one of the following two methods.

- Check whether all standard register readout values are 0xFFFF or not.
- Check whether the INH pin of the PHY is low.

If one of the two events is detected, it means the Sleep flow is successful and the PHY is in Sleep mode.

Note: If not use the INH pin to control PMIC, you can still read the standard register, but the MDI link will be down and read ext 0x3009 (0x918 means enter sleep mode).

2.19.1.3 Sleep Flow for Sleep Responder

- Check Sleep Request from Link Partner

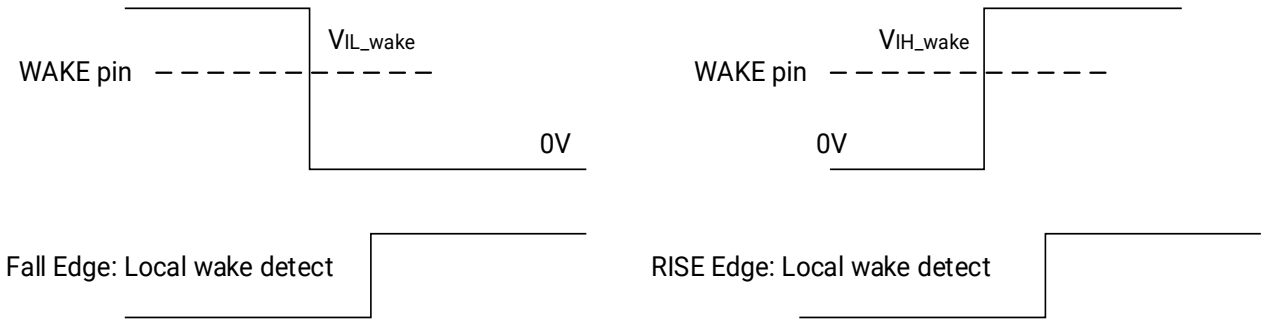
  If a PHY receives a Sleep request from its link partner, it will inform the MAC that the Sleep flow starts. The MAC can receive this Sleep event by reading interrupt (Read mii0x17[3]).

- Sleep Abort Flow

  The MAC can abort the Sleep flow by writing ext 0x3008[3]=1. If the MAC does not command the sleep responder to abort the sleep flow, the sleep responder will start sleep handshaking with the sleep initiator automatically. If the MAC accepts the Sleep request from its link partner, the rest of the process matches that of the Sleep initiator.

2.19.2 Wake Function

2.19.2.1 Local Wake Up



The PHY detects a local wake-up event when the voltage on the WAKE pin is lower/higher than VIL_WAKE/VIH_WAKE for longer than T_{det_WAKE}. Edge is chosen by register ext 0x1088[7]:

- 0 = rise edge
- 1 = fall edge

After detecting a local Wake pulse, the INH's signal rises and then turns on the external regulator. Thus, the whole chip is powered on by the voltage output of the external regulator. After a local wake-up, the PHY will remotely wake up its link partner automatically.

2.19.2.2 Remote Wake Up

The PHY detects a remote wake-up event when it detects a wake-up pulse (WUP, about 1ms width pulse) on the MDI. YT8011A/AN/AR supports sending a wake-up pulse after power on or hardware reset. After

receiving a wake-up pulse on the MDI, the INH's signal rises and then turns on the external regulator. Thus, the whole chip is powered on by the voltage output of the external regulator.

Note: The wake-up pulse is enabled by default after powering on. If performing the PMA test or cable status diagnostics, disable this function.

2.19.3 Wake-Up Electrical Interface

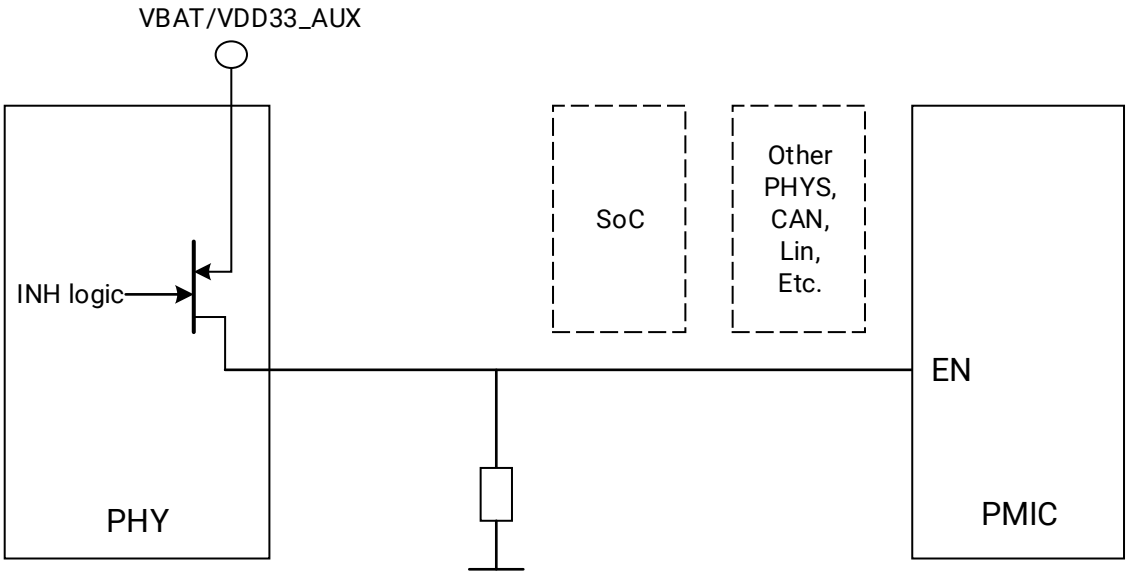
YT8011A/AN/AR supports wake-up and sleep signaling over dedicated I/O pins which follow the following guidelines. Sleep/wake-up commands are not part of the xMII interface. The following list shows examples of pins typically associated with wake-up and sleep functionality. Depending on the type of device and functionality, not all pins are relevant.

Note: INH is supplied by a standby supply which is available during sleep.

Table 11 Wake/Sleep Electrical Interface

Pin name	Direction	Function	Voltage source	Application Mandatory
INH	OUT	Prevent external regulators from shutting down	VBAT/VDD33_AUX	Recommended
WAKE	IN	Local wake input	VBAT/VDD33_AUX or other IO power	Yes
VBAT/VDD33_AUX	IN	Always-on supply, available during sleep to power wake-up detection functionality	VBAT or other available standby supply (VDD33_AUX)	Yes

Figure 16 INH Topology and Example Application

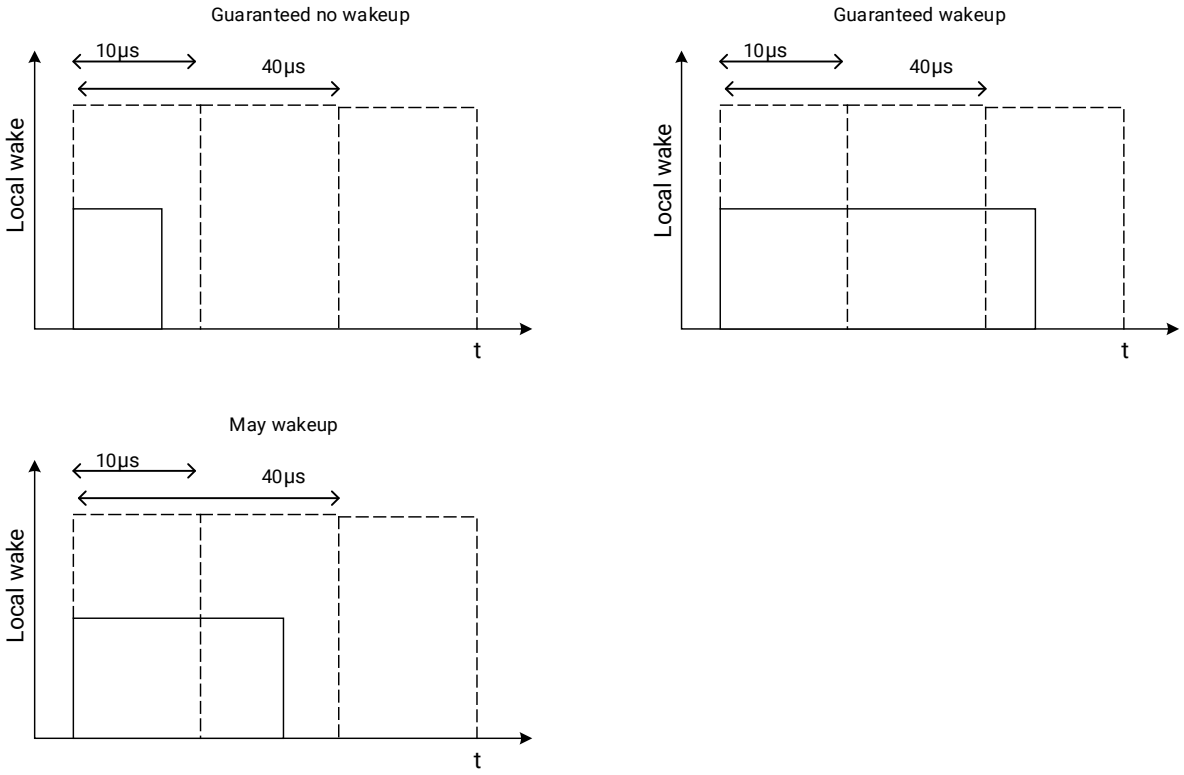


YT8011A/AN/AR supports a glitching wakeup source which is connected to the LOCAL_WAKE pin. Pulses with a duration of less than 10μs must not be detected as wake-up events and are to be ignored.

A pulse duration of more than 40μs must be guaranteed to be detected and cause a wake-up. Note that pulses in this interval are undefined.

From this follows that a local wakeup output pulse must have a duration of at least 40μs to be reliably detected. In case LOCAL_WAKE is fed through the wiring harness (support for slow legacy wake-up line) YT8011A/AN/AR has the option to increase the rejection window (minimum of 10ms).

Figure 17 Local Wake-Up Pulse Width

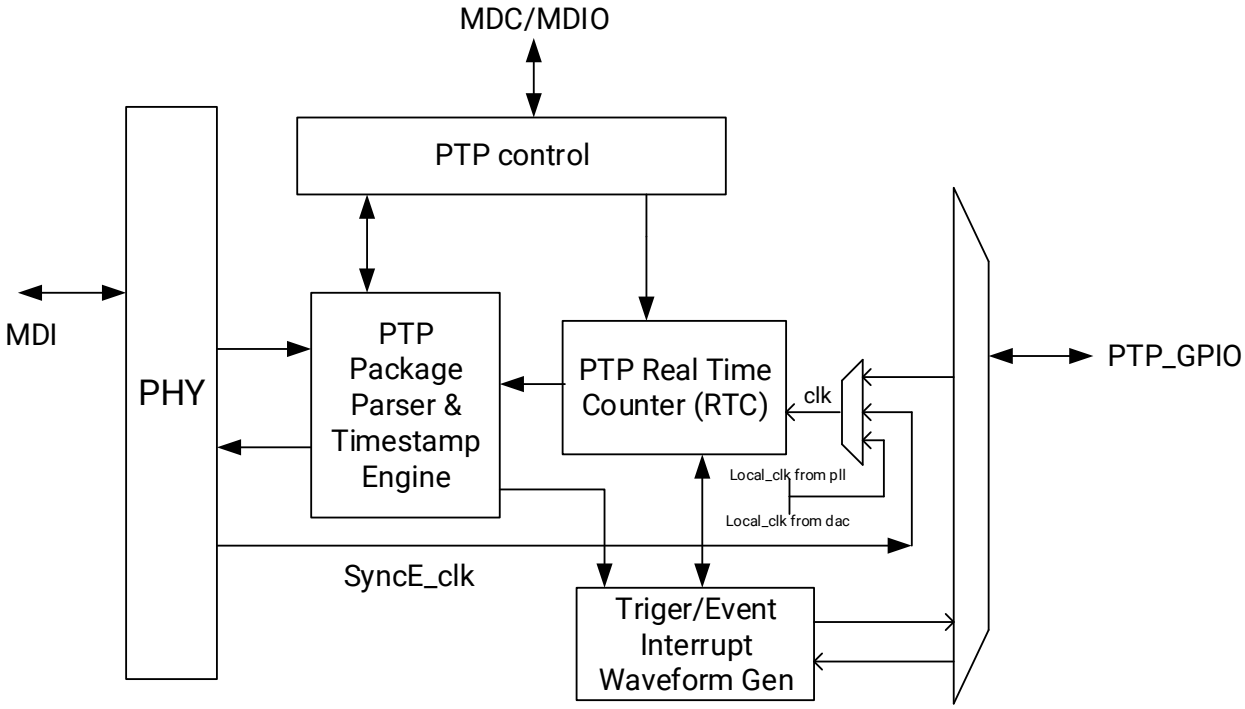


2.20 Precision Time Protocol

YT8011A/AN/AR supports the 1588v2 and 802.1as protocols and has one PTP GPIO pin. The PHY has the internal hardware to update the timestamps. It supports timestamps on IEEE 802.1AS, IEEE 1588 L2, IEEE 1588 IPV4/UDP, and IEEE 1588 IPV6/UDP packets. GPIO supports PPS out, trigger out, event capture, and Real Time Clock (RTC) from the external clock.

2.20.1 PTP Block

Figure 18 PTP Block Diagram



The Timestamp engine is connected to the GMII/MII interface. Both in TX and RX directions, the timestamp engine performs packet parsing/detection, extracts identifications of the packets on the fly, and generates timestamps. The timestamp engine can also modify related packets, insert timestamps, or add residence time, then re-calculate UDP checksum and FCS to validate the packet according to respective standards.

To decrease CPU's MDC/MDIO actions which is to access ingress/egress PTP messages timestamp during usage, 1588 IP provides options to insert the timestamp, or timestamp with truncated second field, into reserved fields of certain PTP message.

2.20.2 RTC control

There is a real-time counter in RTC, which is designed according to IEEE1588v2 standard and consists of 48 bits second field and 32 bits nanosecond field. Within a PTP domain, any slave port will update the PTP clock based on the time difference between the master clock and the slave clock.

YT8011A/AN/AR provides three ways to adjust the slave clock:

- Write the time offset to the RTC

  Once getting the offset in time between the master clock and the slave clock, the slave clock can be updated by writing the corresponding offset register.

  The offset register includes a 48-bit signed second field offset and a 32-bit signed nanosecond field offset. The MSBs of 48-bit second field offset and 32-bit nanoseconds field offset are the signed bits. So the offset register indicates a positive or negative adjustment to the current RTC value.

- Set a desired time value to the RTC directly

  This way loads an 80-bit unsigned time value to the corresponding RTC preload register. The 48-bit second field and 32-bit nanosecond field in the RTC will be overwritten.

- Correct the tick rate of the RTC

  The tick rate will be corrected by adjusting the step (increment value) on each reference clock cycle. This is a smooth and high precise way to adjust the time offset between the master clock and the slave clock. This method will also be used to compensate for the frequency difference of the reference clocks between the master clock and the slave clock.

The frequency difference is the main reason for time offset fluctuation when the network structure is stable.

The rate correction can be calculated based on the ratio of the timestamp changes on the master side to the timestamp changes on the slave side.

The step on each reference clock cycle can be adjusted by writing the corresponding increment value register.

The increment value register includes a 6-bit nanoseconds field and a 26-bit fractional nanoseconds field.

The method which is used to update the PTP clock value may depend on different applications. For example, before the synchronization process, the clock can be set with a desired time by writing the preload register. When the clocks are very close, the rate adjustment method may be the best option.

2.20.3 PTP GPIO Application

RTC has several auxiliary blocks, including a waveform generator, clock servo for the grandmaster, trigger output, and event capture.

3 Operational Description

3.1 RESET

YT8011A/AN/AR has a hardware reset pin (RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up including wakeup from sleep mode.

RESET_N is also used to enable power on strapping. After RESET_N is released, YT8011A/AN/AR latches input values on RX_DV, RXC, and RXD[3:0].

3.2 PHY Address

For YT8011A/AN/AR, RXD0/PHYAD0 and RXD1/PHYAD1 are used to configure the PHY address.

YT8011A/AN/AR always responds to PHY address 0. It also has another broadcast PHY address which is configurable through MDIO. Bit[4:0] of the extended register (address 0x0) is the broadcast PHY address and its default value is 5'b11111. Bit[5] of the extended register (address 0x0) enables control for broadcast PHY address and its default value is 1'b1.

3.3 Strapping Pins Setting

After power on or hardware reset, RX_DV, RXC, and RXD[3:0] pins are latched and the chip is configured to corresponding mode.

Table 12 Strapping Setting

Pin Name	Type	Description
RXD1/PHYAD1	O/LI/PD	PHY Address[1:0] Configuration: 2'b00: 0x0 2'b01: 0x1(default) 2'b10: 0x2 2'b11: 0x3
RXD0/PHYAD0	O/LI/PU	
RXDV/ST_CHG	O/LI/PU	Operating modes state change condition configuration ● 1'b1: Auto mode(default) The PHY goes to normal mode automatically, when the device is powered on, woken up, or driven RESET_N pin to low. ● 1'b0: Manual mode The PHY goes to normal mode manually, when the device is powered on, woken up, or driven RESET_N pin to low.
RXD3/MS_SEL	O/LI/PD	Master/Slave mode selection: 1'b1: Master 1'b0: Slave (default)
RXD2/MII_SEL	O/LI/PD	MII mode selection: 1'b1: SGMII 1'b0: RGMII (default) YT8011AR does not support.
RXC/RXDLY_EN	O/LI/PU	The delay to RXC for RXD latching: 1'b1: Add the delay to RXC for RXD latching. (default) 1'b0: No delay to RXC for RXD latching.

4 Register Overview

The YT8011 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 12.5MHz must drive the MDC pin of the YT8011. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

Notation	Description
RW	Read and Write
SC	Self-Clear
RO	Read Only
LH	Latch High
LL	Latch Low
RC	Read Clear
SWC	Software Reset Clear

4.1 PHY MII Register

4.1.1 Basic Control Register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW/SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Reserved	RW	0x0	Reserved
13	spd_sel13	RO	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = reserved
12	an_en	RW	0x0	1: Enable auto-negotiation 0: Disable auto-negotiation
11	pwr_dn	RW	0x0	Power down mode

Bit	Symbol	Access	Default	Description
10	isolate	RW	0x0	Isolate PHY from RGMII/SGMII. 1'b0: Normal mode 1'b1: Isolate mode
9	re_atneg	RW	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8:7	reserved	RO	0x2	Reserved
6	spd_sel6	RO	0x0	See bit13.
5:0	Reserved	RO	0x0	Reserved

4.1.2 Basic Status Register1 (0x01)

Bit	Symbol	Access	Default	Description
15:6	Reserved	RO	0x0	Reserved
5	aneg_cmplt	RO	0x0	1'b0: Auto-negotiation process not completed 1'b1: Auto-negotiation process completed
4	rmt_fault	RC	0x0	Remote fault 1'b0: No Remote fault 1'b1: Remote fault
3	Reserved	RO	0x1	Reserved
2	link_status	RO	0x0	Link status 1'b0: Link is down 1'b1: Link is up
1	jab_detect	RC	0x0	Jabber detection 1'b0: No jabber detection 1'b1: Jabber detection
0	Reserved	RO	0x1	Reserved

4.1.3 Identification Register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x4f51	Bits 3 to 18 of the Organizationally Unique Identifier

4.1.4 Identification Register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x3A	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x30	6 bits manufacturer's type number

Bit	Symbol	Access	Default	Description
3:0	Revision_No	RO	0x1	4 bits manufacturer's revision number

4.1.5 Debug Register's Data Register (0x10)

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	0x0	Reserved
4	int_polar_sel	RW	0x0	Polarity for interrupt pin 0: Active low 1: Active high
3:0	Reserved	RO	0x0	Reserved

4.1.6 Debug Register's Data Register (0x12)

Bit	Symbol	Access	Default	Description
15:0	int_mask	RW	0x0	Interrupt mask, mapping reg 0x13

4.1.7 Debug Register's Data Register (0x13)

Bit	Symbol	Access	Default	Description
15	auto_neg_err_int	RC	0x0	Error occurred during auto-negotiation
14	spd_chg_int	RC	0x0	Speed changed
13	Reserved	RW	0x0	Reserved
12	page_received_int	RC	0x0	Page received during auto-negotiation
11	link_fail_int	RC	0x0	Link down for PHY
10	link_success_int	RC	0x0	Link up for PHY
9	int_1588_misc	RC	0x0	PTP MISC event detected
8	int_1588_rx_ptp	RC	0x0	Ingress PTP message detected
7	int_1588_tx_ptp	RC	0x0	Egress PTP message detected
6	Reserved	RC	0x0	Reserved
5	autospd_dngrd_p_int	RC	0x0	Downgrade occurred
4	crc_err_int	RO	0x0	CRC error occurred
3	link_fail_sds_int	RC	0x0	Link fail for Serdes
2	link_success_sds_int	RC	0x0	Link up for Serdes
1	polar_chg_int	RC	0x0	Polarity changed
0	jabber_int	RC	0x0	Jabber packet received

4.1.8 Debug Register's Data Register (0x16)

Bit	Symbol	Access	Default	Description
15:11	Reserved	RO	0x0	Reserved
10:0	int_mask	RW	0x0	Interrupt mask, mapping reg 0x17

4.1.9 Debug Register's Data Register (0x17)

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	0x0	Reserved
8	Reserved	RC	0x0	Reserved
7	link_status_change_int	RC	0x0	Link status changed
6	loc_rcvr_status_change_int	RC	0x0	Local receiver status changed
5	rem_rcvr_status_change_int	RC	0x0	Remote receiver status changed
4	trainning_failed_int	RC	0x0	Training failed
3	lps_recv_int	RC	0x0	Receive lower-power sleep
2	wake_recv_int	RC	0x0	Receive remote wake
1	sleep_fail_int	RC	0x0	Sleep fail
0	over_temp_int	RC	0x0	Over temperature

4.2 PHY EXT Register

4.2.1 DAC Config Register1 (0x1018)

Bit	Symbol	Access	Default	Description
4:0	dac_lpfil_adj	RW	0x5	DAC driver

4.2.2 DAC Config Register2 (0x1019)

Bit	Symbol	Access	Default	Description
14:8	dac_imsb_cfg_100	RW	0x3b	DAC config in 100M mode
6:0	dac_imsb_cfg_1000	RW	0x12	DAC config in 1000M mode

4.2.3 DAC Config Register3 (0x101a)

Bit	Symbol	Access	Default	Description
14:8	dac_imid_cfg_100	RW	0x3b	DAC config in 100M mode
6:0	dac_imid_cfg_1000	RW	0x13	DAC config in 1000M mode

4.2.4 PTP CLK EN (0x1072)

Bit	Symbol	Access	Default	Description
8	en_clk_1588	RW	0x0	Enable clock for IEEE1588 module
7:4	clk_1588_ctr1	RW	0x4	CLK divider config for IEEE1588 module
1:0	clk_1588_ctr2	RW	0x2	CLK divider config for IEEE1588 module

4.2.5 Sleep&Wake Config1 (0x1088)

Bit	Symbol	Access	Default	Description
9:8	ao_wakeup_cfg	RW	0x0	Remote wake threshold
7	ao_wakeup_rise_fall	RW	0x0	wake up edge 0: Rising edge 1: Falling edge
6	ao_sleep_mode_en	RW	0x0	Enable sleep mode, enter sleep with rising edge
5	ao_reg_w_en	RW	0x0	Write enable for wake up related Register
4	ao_inh_io_sel	RW	0x0	Internal use
3	ao_por_dig	RO	0x0	Internal use
2	ao_loc_act_detect	RO	0x0	Remote wake-up indication 1: MDI is active 0: MDI is in-active
1	ao_wake_dig	RO	0x1	Status of WAKE pin
0	ao_inh_dig	RO	0x1	Status of INH pin

4.2.6 Sleep&Wake Config2 (0x1089)

Bit	Symbol	Access	Default	Description
1	ao_wakeup_time_sel	RW	0x0	Deglitch time of wake-up 0: 20μs 1: 10ms
0	ao_wakeup_vih_sel	RW	0x0	VIH swap threshold

4.2.7 Loopback Config (0x2036)

Bit	Symbol	Access	Default	Description
3	echo_cancel_en_el_100	RW	0x1	Echo canceller for 100M
2	echo_cancel_en_el_1000	RW	0x0	Echo canceller for 1000M
1	ext_lpbk	RW	0x0	External loopback
0	int_lpbk	RW	0x0	Internal loopback

4.2.8 Sleep Control1 (0x3008)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	bypass_pll_calib_done	RW	0x0	
10	power_dn	RW	0x0	Power down
9	power_up	RW	0x0	Power up
8	st_chg	RW	0x0	Status change 1: Change status automatically 0: Change status manually
7	Reserved	RO	0x0	Reserved
6	tc_start_link_ctrl	RW	0x1	
5	loc_wake_req	RW	0x0	Local wake request This bit will automatically clear 0 after the function takes effect
4	loc_sleep_req	RW	0x0	Local sleep request This bit will automatically clear 0 after the function takes effect
3	loc_sleep_abort	RW	0x0	Local sleep abort This bit will automatically clear 0 after the function takes effect
2	sleep_mode_en	RW	0x0	Force in sleep mode
1	en_sleep_cap	RW	0x1	Enable sleep function
0	bypass_power_control	RW	0x0	Bypass power control function

4.2.9 Sleep Control2 (0x3009)

Bit	Symbol	Access	Default	Description
12	manu_exit_sleep	SC	0x0	Exit sleep manually
11:8	State_power	RO	0x2	Power state
7:6	Reserved	RO	0x0	Reserved
5	INH	RO	0x1	INH state
4	sleep	RO	0x0	Sleep state
3	bp_fast_linkdown	RW	0x1	No use
2:0	fl_timer_sel	RW	0x0	No use

4.2.10 MSE Debug1 (0x3070)

Bit	Symbol	Access	Default	Description
9:0	dcq_mse_latch	RL	0x0	dcq_mse value

4.2.11 MSE Debug2 (0x3071)

Bit	Symbol	Access	Default	Description
9:0	dcq_mse_wc_latch	RLC	0x0	dcq_mse value in worst case

4.2.12 MSE Debug3 (0x3072)

Bit	Symbol	Access	Default	Description
5:0	dcq_pmse_latch	RL	0x0	Peak dcq_mse value

4.2.13 MSE Debug4 (0x3073)

Bit	Symbol	Access	Default	Description
5:0	dcq_pmse_wc_latch	RLC	0x0	Peak dcq_mse value in the worst case

4.2.14 Pkg Config1 (0x4038)

Bit	Symbol	Access	Default	Description
14	en_pkg_odd_prm	RW	0x0	1 = Enable UTP pkg sent odd number preamble
13	pkgen_lpi	RW	0x0	Enable send LPI idle pattern
12	en_pkgen_da_sa	RW	0x0	Enable send packets with DA/SA
11	pkgen_brdcst	RW	0x0	Enable PKG to send broadcast packets
10	pkgchk_txsrc_sel	RW	0x0	1 = TX check select the packet from PKG 0 = TX check select the packet from UTP source
9	pkgen_en_az	RW	0x0	To send AZ LPI pattern during IPG
8:0	pkgen_in_az_t	RW	0x1ff	IN AZ LPI pattern time

4.2.15 Pkg Config2 (0x4039)

Bit	Symbol	Access	Default	Description
15:8	pkgen_pre_az_t	RW	0x20	PRE AZ LPI pattern time
7:0	pkgen_aft_az_t	RW	0x19	POST AZ LPI pattern time

4.2.16 Pkg Config3 (0x403a)

Bit	Symbol	Access	Default	Description
15:8	pkgen_sa	RW	0x0	Source address
7:0	pkgen_da	RW	0x0	Destination address

4.2.17 Pkg Config4 (0x40a0)

Bit	Symbol	Access	Default	Description
15	Pkg_chk_en	RW	0x0	1: Enable RX/TX package checker. RX checker checks the MII data at the transceiver's PCS RX; TX checker checks the MII data at mii_bridge's TX.
14	Pkg_en_gate	RW	0x1	1: Enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0; 0: No gate the clocks.
13	Bp_pkg_gen	RW	0x1	1: Normal mode, send xMII TX data from PAD; 0: Test mode, send out the MII data generated by pkg_gen module.
12	Pkg_gen_en	RW/SC	0x0	1: Enable pkg_gen generating MII packages. But the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0. If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0; Otherwise, after the expected packages are generated, pkg_gen will stop, and pkg_gen_en will be self-cleared.
11:8	Pkg_prm_lth	RW	0x8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only supports >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	Pkg_ipg_lth	RW	0xC	The IPG of the generated packages, in Byte unit. Pkg_gen function only supports >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	Xmit_mac_force_gen	RW	0x0	1: Enable pkg_gen to send out the generated data even when the link is not established.
2	Pkg_corrupt_crc	RW	0x0	1: Make pkg_gen to send out CRC error packages. 0: pkg_gen sends out CRC good packages.
1:0	Pkg_payload	RW	0x0	Control the payload of the generated packages. 00: Increased Byte payload; 01: Random payload; 10: Fix pattern 0x5AA55AA5... 11: Fix pattern defined by EXT 0x40b7 bit11:4.

4.2.18 Pkg Config5 (0x40a1)

Bit	Symbol	Access	Default	Description
15:0	Pkg_length	RW	0x40	To set the length of the generated packages.

4.2.19 Pkg Config6 (0x40a2)

Bit	Symbol	Access	Default	Description
15:0	Pkg_burst_size	RW	0x0	To set the number of packages in a burst of package generation. 0: continuous packages will be generated.

4.2.20 Checker Register1 (0x40a3)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_valid_high	RO	0x0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length >=64Byte and <=1518Byte.

4.2.21 Checker Register2 (0x40a4)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_valid_low	RO	0x0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length >=64Byte and <=1518Byte.

4.2.22 Checker Register3 (0x40a5)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_os_good_high	RO	0x0	Pkg_ib_os_good[31:16], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length >1518Byte.

4.2.23 Checker Register4 (0x40a6)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_os_good_low	RO	0x0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length >1518Byte.

4.2.24 Checker Register5 (0x40a7)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_us_good_high	RO	0x0	Pkg_ib_us_good[31:16], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length <64Byte.

4.2.25 Checker Register6 (0x40a8)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_us_good_low	RO	0x0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length >1518Byte.

4.2.26 Checker Register7 (0x40a9)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_err	RO	0x0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length >=64Byte, <=1518Byte.

4.2.27 Checker Register8 (0x40aa)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_os_bad	RO	0x0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length >=1518Byte.

4.2.28 Checker Register9 (0x40ab)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_frag	RO	0x0	pkg_ib_frag is the number of RX packages from wire whose length <64Byte.

4.2.29 Checker Register10 (0x40ac)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ib_nosfd	RO	0x0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

4.2.30 Checker Register11 (0x40ad)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_valid_high	RO	0x0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length >=64Byte and <=1518Byte.

4.2.31 Checker Register12 (0x40ae)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_valid_low	RO	0x0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length >=64Byte and <=1518Byte.

4.2.32 Checker Register13 (0x40af)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_os_good_high	RO	0x0	Pkg_ob_os_good[31:16], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length >1518Byte.

4.2.33 Checker Register14 (0x40b0)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_os_good_low	RO	0x0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length >1518Byte.

4.2.34 Checker Register15 (0x40b1)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_us_good_high	RO	0x0	Pkg_ob_us_good[31:16], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length <64Byte.

4.2.35 Checker Register16 (0x40b2)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_us_good_low	RO	0x0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length >1518Byte.

4.2.36 Checker Register17 (0x40b3)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_err	RO	0x0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length >=64Byte, <=1518Byte.

4.2.37 Checker Register18 (0x40b4)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_os_bad	RO	0x0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length >=1518Byte.

4.2.38 Checker Register19 (0x40b5)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_frag	RO	0x0	pkg_ob_frag is the number of TX packages from MII whose length <64Byte.

4.2.39 Checker Register20 (0x40b6)

Bit	Symbol	Access	Default	Description
15:0	Pkg_ob_nosfd	RO	0x0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

4.3 PHY MMD Register

4.3.1 PMA Control Register1 (MMD 1,0x00)

Bit	Symbol	Access	Default	Description
15	pma_rst	RW SC	0x0	Set this bit will set all PMA/PMD registers to their default states. This action also initiates a reset in MMD3 and MMD7.
14	reserved	RO	0x0	Reserved
13	bt1_spd_mode[0]	RO	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Bit6 bit13 1 1 = reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = reserved
12	reserved	RO	0x0	Reserved
11	low_power_mode	RW	0x0	1: Low power mode 0: Normal operation
10:7	reserved	RO	0x0	Reserved
6	bt1_spd_mode[1]	RO	0x0	See bit13.
5:0	reserved	RO	0x0	Reserved

4.3.2 PMA Status Register1 (MMD 1,0x1)

Bit	Symbol	Access	Default	Description
15:3	reserved	RO	0x0	Reserved
2	link_up_pma_ll	RO	0x0	PMA local receiver status, latch low
1:0	reserved	RO	0x2	Reserved

4.3.3 PMA Speed Ability (MMD 1,0x4)

Bit	Symbol	Access	Default	Description
15:0	reserved	RO	0x30	Reserved

4.3.4 PMA Device in Package1 (MMD 1,0x5)

Bit	Symbol	Access	Default	Description
15:0	reserved	RO	0x8b	Reserved

4.3.5 PMA Device in Package2 (MMD 1,0x7)

Bit	Symbol	Access	Default	Description
15:6	reserved	RO	0x0	Reserved
5:0	type_sel	RW	0x3d	

4.3.6 PMA Status Register2 (MMD 1,0x8)

Bit	Symbol	Access	Default	Description
15:0	reserved	RO	0x8000	Reserved

4.3.7 PMA Transmit Disable Register (MMD 1,0x9)

Bit	Symbol	Access	Default	Description
15:1	reserved	RO	0x0	Reserved
0	transmit_disable	RW	0x0	Disable transmitter

4.3.8 PMA Extended Ability Register (MMD 1,0x12)

Bit	Symbol	Access	Default	Description
15:0	reserved	RO	0x3	Reserved

4.3.9 Base-T1 PMA Control Register (MMD 1,0x834)

Bit	Symbol	Access	Default	Description
15	reserved	RO	0x1	reserved
14	force_config	RW	0x1	1: Force master 0: Force slave
13:4	reserved	RO	0x0	reserved
3:0	force_phy_type	RW	0x1	4'b0001: 1000BASE-T1 4'b0000: 100BASE-T1

4.3.10 100BASE-T1 PMA Test Control Register (MMD 1,0x836)

Bit	Symbol	Access	Default	Description
15:13	test_mode_100bt1	RW	0x0	Test mode for 100BASE-T1
12:0	reserved	RO	0x0	Reserved

4.3.11 1000BASE-T1 PMA Control Register (MMD 1,0x900)

Bit	Symbol	Access	Default	Description
15	pma_rst	RW SC	0x0	Set this bit will set all PMA/PMD registers to their default states. This action also initiates a reset in MMD3 and MMD7.
14	transmit_disable	RW	0x0	Disable transmitter
13:12	reserved	RO	0x0	Reserved
11	low_power_mode	RW	0x0	1: Low power mode 0: Normal operation
10:0	reserved	RO	0x0	Reserved

4.3.12 1000BASE-T1 PMA Status Register (MMD 1,0x901)

Bit	Symbol	Access	Default	Description
10:3	reserved	RO	0x1b0	Reserved
2	rx_pol	RO	0x0	1: Receive polarity is reversed 0: Receive polarity is not reversed
1	receive_fault	RO	0x0	1: Fault condition detected 0: Fault condition not detected
0	link_up_pma_ll	RO/LL	0x0	PMA local receiver status, latch low

4.3.13 1000BASE-T1 Training Register (MMD 1,0x902)

Bit	Symbol	Access	Default	Description
15:11	reserved	RO	0x0	Reserved
10:4	user_field	RW	0x0	7-bit user-defined field to send to the link partner
3:2	reserved	RO	0x0	Reserved
1	oam_adv	RW	0x0	1: 1000BASE-T1 OAM ability advertised to link partner 0: 1000BASE-T1 OAM ability not advertised to link partner
0	eee_adv	RW	0x0	1: 1000BASE-T1 EEE ability advertised to link partner 0: 1000BASE-T1 EEE ability not advertised to link partner

4.3.14 1000BASE-T1 LP Training Register (MMD 1,0x903)

Bit	Symbol	Access	Default	Description
15:11	reserved	RO	0x0	Reserved
10:4	user_field_lp	RO	0x0	7-bit user-defined field received from the link partner
3:2	reserved	RO	0x0	Reserved
1	oam_adv_lp	RO	0x0	1: Link partner has 1000BASE-T1 OAM ability 0: Link partner does not have 1000BASE-T1 OAM ability
0	eee_adv_lp	RO	0x0	1: Link partner has 1000BASE-T1 EEE ability 0: Link partner does not have 1000BASE-T1 EEE ability

4.3.15 1000BASE-T1 Test Mode Control Register (MMD 1,0x904)

Bit	Symbol	Access	Default	Description
15:13	test_mode_1000bt1	RW	0x0	test mode for 1000BASE-T1 3'b111: test mode 7 3'b110: test mode 6 3'b101: test mode 5 3'b100: test mode 4 3'b011: reserved 3'b010: test mode 2 3'b001: test mode 1 3'b000: normal mode
12:0	reserved	RO	0x0	Reserved

4.3.16 PCS Control Register1 (MMD 3,0x00)

Bit	Symbol	Access	Default	Description
15	pcs_rst	RW SC	0x0	Set this bit will set all PCS registers to their default states. This action also initiates a reset in MMD1 and MMD7.
14	pcs_lpbk	RW	0x0	1: Enable PCS loopback mode.
13:11	Reserved	RO	0x0	Reserved
10	clock_stoppable	RW	0x0	
9:0	Reserved	RO	0x0	Reserved

4.3.17 PCS Control Register2 (MMD 3,0x900)

Bit	Symbol	Access	Default	Description
15	pcs_rst	RW SC	0x0	Set this bit will set all PCS registers to their default states. This action also initiates a reset in MMD1 and MMD7.
14	pcs_lpbk	RW	0x0	1: Enable PCS loopback mode.
13:0	Reserved	RO	0x0	Reserved

4.3.18 PCS Control Register3 (MMD 3,0x901)

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	0x0	Reserved
11	Tx_lpi_rxed	RO LH	0x0	When read as 1, it indicates that the transmit PCS has received low-power idle signaling one or more times since the register was last read. Latch High.
10	Rx_lpi_rxed	RO LH	0x0	When read as 1, it indicates that the received PCS has received low-power idle signaling one or more times since the register was last read. Latch High.
9	Tx_lpi_indic	RO	0x0	When read as 1, it indicates that the transmit PCS is currently receiving a low-power idle signal.
8	Rx_lpi_indic	RO	0x0	When read as 1, it indicates that the received PCS is currently receiving a low-power idle signal.
7:3	Reserved	RO	0x0	Reserved
2	Pcsrx_lnk_status	RO LL	0x0	PCS status, latch low.
1:0	Reserved	RO	0x0	Reserved

4.3.19 PCS Status Register (MMD 3,0x902)

Bit	Symbol	Access	Default	Description
15:11	Reserved	RO	0x0	Reserved
10	pcs_link_status	RO	0x0	1: PCS receives link up 0: PCS receives link down
9	pcs_high_ber	RO	0x0	1: PCS reporting a high BER 0: PCS not reporting a high BER
8	pcs_block_lock	RO	0x0	1: PCS locked to received blocks 0: PCS not locked to received blocks
7	latched_high_ber	RO/LH	0x0	1: PCS has reported a high BER 0: PCS has not reported a high BER
6	latched_block_lock	RO/LL	0x0	1: PCS has a block lock 0: PCS does not have a block lock
5:0	ber_count	RO/NR	0x0	BER counter

4.3.20 OAM Register1 (MMD 3,0x904)

Bit	Symbol	Access	Default	Description
15	oam_vld	RW/SC	0x0	This bit is used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit shall self-clear when registers are loaded by the state machine. 1: Message data in registers are valid 0: Message data in registers are not valid
14	tog_val	RO	0x0	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.
13	oam_rx	RO/LH	0x0	This bit shall self-clear on read. 1: 1000BASE-T1 OAM message received by link partner 0: 1000BASE-T1 OAM message not received by link partner
12	tog_val_rx	RO	0x0	Toggle value of message that was received by link partner as indicated in 3.2308.13.
11:8	message_num	RW	0x0	User-defined message number to send
7:4	Reserved	RO	0x0	Reserved
3	ping_rx	RO	0x0	Received PingTx value from latest good 1000BASE-T1 OAM frame received
2	ping_tx	RW	0x0	Ping value to send to link partner
1:0	loc_snr	RO	0x0	2'b00: PHY link is failing and will drop link and relink within 2ms to 4ms after the end of the current 1000BASE-T1 OAM frame. 2'b01: LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 2'b10: PHY SNR is marginal.

Bit	Symbol	Access	Default	Description
				2'b11: PHY SNR is good.

4.3.21 OAM Register2 (MMD 3,0x905)

Bit	Symbol	Access	Default	Description
15:0	mr_tx_message[15:0]	RW	0x0	TX message [15:0]

4.3.22 OAM Register3 (MMD 3,0x906)

Bit	Symbol	Access	Default	Description
15:0	mr_tx_message[31:16]	RW	0x0	TX message [31:16]

4.3.23 OAM Register4 (MMD 3,0x907)

Bit	Symbol	Access	Default	Description
15:0	mr_tx_message[47:32]	RW	0x0	TX message [47:32]

4.3.24 OAM Register5 (MMD 3,0x908)

Bit	Symbol	Access	Default	Description
15:0	mr_tx_message[63:48]	RW	0x0	TX message [63:48]

4.3.25 OAM Register6 (MMD 3,0x909)

Bit	Symbol	Access	Default	Description
15	lp_oam_vld	RO/SC	0x0	This bit is used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are stored and ready to be read. This bit shall self-clear when register 3.2317 is read. 1: Message data in registers are valid 0: Message data in registers are not valid
14	lp_tog_val	RO	0x0	Toggle value received with message
13:12	Reserved	RO	0x0	Reserved
11:8	lp_message_num	RO	0x0	Message number from the link partner
7:2	Reserved	RO	0x0	Reserved
1:0	lp_loc_snr	RO	0x0	2'b00: The link partner link is failing and will drop link and relink within 2ms to 4ms after the end of the current 1000BASE-T1 OAM frame.

Bit	Symbol	Access	Default	Description
				2'b01: LPI refresh is insufficient to maintain link partner SNR. The link partner requests the local device to exit LPI and send idles (used only when EEE is enabled). 2'b10: Link partner SNR is marginal. 2'b11: Link partner SNR is good.

4.3.26 OAM Register7 (MMD 3,0x90a)

Bit	Symbol	Access	Default	Description
15:0	lp_tx_message[15:0]	RO	0x0	Link partner TX message [15:0]

4.3.27 OAM Register8 (MMD 3,0x90b)

Bit	Symbol	Access	Default	Description
15:0	lp_tx_message[31:16]	RO	0x0	Link partner TX message [31:16]

4.3.28 OAM Register9 (MMD 3,0x90c)

Bit	Symbol	Access	Default	Description
15:0	lp_tx_message[47:32]	RO	0x0	Link partner TX message [47:32]

4.3.29 OAM Register10 (MMD 3,0x90d)

Bit	Symbol	Access	Default	Description
15:0	lp_tx_message[63:48]	RO	0x0	Link partner TX message [63:48]

4.3.30 AN Control Register1 (MMD 7,0x200)

Bit	Symbol	Access	Default	Description
15	An_rst	RW/SC	0x0	Set this bit will set all AN Registers to their default states. This action also initiates a reset in MMD1 and MMD3.
14:13	Reserved	RO	0x0	Reserved
12	an_en	RW	0x0	1: enable Auto-negotiation process 0: disable Auto-Negotiation process
11:10	Reserved	RO	0x0	Reserved
9	re_atneg	RW/SC	0x0	1: Restart the Auto-negotiation process. 0: Auto-Negotiation in process, disabled, or not supported

Bit	Symbol	Access	Default	Description
8:0	Reserved	RO	0x0	Reserved

4.3.31 AN Status Register2 (MMD 7,0x201)

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	0x0	Reserved
6	page_rcved	RO/LH	0x0	1: A page has been received. 0: A page has not been received
5	an_cmplt	RO	0x0	1: Auto-negotiation process completed. 0: Auto-Negotiation process not completed
4	Remote fault	RO/LH	0x0	1: Remote fault condition detected. 0: No remote fault condition detected
3	Auto-nego ability	RO	0x1	1: PHY can perform Auto-Negotiation 0: PHY can not perform Auto-Negotiation
2	link_status	RO/LL	0x0	1: Link up 0: Link down
1:0	Reserved	RO	0x0	Reserved

4.4 Common EXT Register

4.4.1 SMI_SDS_PHY (0x9000)

Bit	Symbol	Access	Default	Description
15	smi_sds_phy	RW	0x0	Control access whether PHY register or SDS register. 1: Access SDS; 0: Access PHY.

4.4.2 RGMII Config Register1 (0x9001)

Bit	Symbol	Access	Default	Description
15	reserved	RW	0x0	reserved
14	en_fine_code_gen	RW	0x0	Not used
13	reserved	RW	0x0	reserved
12	reserved	RW	0x0	reserved
10	phy_48pin	RW	0x0	Not used
9	tx_clk_sel	RW	0x0	1=Invert the GMII clock phase to sample the RGMII data from PAD
8	rx_clk_delay_en	RW/STRAP	0x1	1=Enable RXC 2ns delay
7:4	tx_delay_sel	RW	0x1	Config the delay of RGMII TXC clock from PAD

Bit	Symbol	Access	Default	Description
3:0	reserved	RW	0x0	reserved

4.4.3 Common Control Register1 (0x9030)

Bit	Symbol	Access	Default	Description
15:14	comb_wait_timer_sel	RW	0x0	Not used
13	bp_gmii_fatal_rst	RW	0x1	1=bypass the GMII FIFO reset when fatal happens
12	uldata_rloopback	RW	0x0	1=remain upload data when rem LPBK is set for PHY or SDS
11	rem_lpbk_phy	RW	0x0	1=set remote loopback for SDS
10	rem_lpbk_sds	RW	0x0	1=set remote loopback for PHY
9	jumbo_enable_u2f	RW	0x0	Not used
8	jumbo_enable	RW	0x0	1=Enable Jumbo frame
7	fiber_high_pri_cmb	RW	0x0	Not used
6	en_chk_fx100_u2f_an	RW	0x0	Not used
5	en_u2f_an	RW	0x0	Not used
4	sleeping	RW	0x0	1=Set Serdes to sleep manually, only when bit3 was set to 1
3	en_sds_sleep	RW	0x0	1=Enable Serdes manually sleep
0	mii_sel	RW/STRAP	0x0	1=Chip works in SGMII mode 0=Chip works in RGMII mode

4.4.4 RGMII Config Register2 (0x9038)

Bit	Symbol	Access	Default	Description
15:8	csr_rg_rfu_da	RW	0x0	Reserved for internal usage
7:0	csr_rg_rfu_dh	RW	0x10	Reserved for internal usage

4.4.5 RGMII Config Register3 (0x903b)

Bit	Symbol	Access	Default	Description
6:4	csr_rg_dr_rout_cfg	RW	0x4	Reserved for internal usage
1:0	csr_rg_ic_lvlsft_cfg	RW	0x0	Reserved for internal usage

4.4.6 RGMII Config Register4 (0x903c)

Bit	Symbol	Access	Default	Description
3:2	csr_dr_cc_cfg_rxd	RW	0x3	Reserved for internal usage

Bit	Symbol	Access	Default	Description
1:0	csr_dr_cc_cfg_rxc	RW	0x3	Reserved for internal usage

4.4.7 RGMII Config Register5 (0x903d)

Bit	Symbol	Access	Default	Description
15:14	csr_dr_chg_tf_cfg_rxd	RW	0x0	Reserved for internal usage
13:12	csr_dr_chg_tf_cfg_rxc	RW	0x0	Reserved for internal usage
11:10	csr_dr_chg_tr_cfg_rxd	RW	0x0	Reserved for internal usage
9:8	csr_dr_chg_tr_cfg_rxc	RW	0x1	Reserved for internal usage
1:0	csr_rg_io_lvl_cfg	RW	0x0	config the RGMII io voltage level 00=RGMII works in 3.3V mode 10=RGMII works in 2.5V mode 11=RGMII works in 1.8V mode

4.4.8 RGMII Config Register6 (0x903e)

Bit	Symbol	Access	Default	Description
15:8	csr_dr_chg_main_cfg_rxd	RW	0x3b	Reserved for internal usage
7:0	csr_dr_chg_main_cfg_rxc	RW	0x3b	Reserved for internal usage

4.4.9 RGMII SSC Config Register7 (0x9051)

Bit	Symbol	Access	Default	Description
8	En_ssc_tx_fifo	RW	0x0	1=Enable SSC TX FIFO
7	pi_ssc_clk_sel	RW	0x1	1=Revert the internal clock phase of the PI clock
6	revert_pi_ssc	RW	0x0	1=Revert the PI code of SSC
5	rot_dir_phy	RW	0x0	Config the rot direction of the SSC PI code
4	en_rgmii_ssc	RW	0x0	1=Enable RGMII SSC on RXC clock
3:2	ssc_cycle	RW	0x3	Config the SSC period: 11=32μs 10=16μs 01=8μs 00=4μs
1:0	ssc_ppm	RW	0x3	Config the SSC modulation depth: 11=1.56% 10=0.78% 01=0.39% 00=0.195%

4.4.10 LED Control Register1 (0x9063)

Bit	Symbol	Access	Default	Description
13	Led_act_blk_ind_1	RW	0x0	When traffic is present, make LED0 BLINK no matter if the previous LED0 status is ON or OFF, or make LED0 blink only when the previous LED0 is ON.
12	Led_fdx_on_en_1	RW	0x0	1: If BLINK status is not activated, when PHY link up and duplex mode is full duplex, LED0 will be ON.
11	Led_hdx_on_en_1	RW	0x0	If BLINK status is not activated, when PHY link up and duplex mode is half-duplex
10	Led_txact_blk_en_1	RW	0x1	1: If bit13 is 1, or bit13 is 0 and ON at a certain speed or duplex more is/are activated, when PHY link up and TX is active
9	Led_rxact_blk_en_1	RW	0x1	If bit13 is 1, or bit13 is 0 and ON at a certain speed or duplex more is/are activated, when PHY link up and RX is active
8	Led_txact_on_en_1	RW	0x0	1 = If BLINK status is not activated, when PHY link up and TX is active, make LED0 ON at least 10ms
7	Led_rxact_on_en_1	RW	0x0	1 = If BLINK status is not activated, when PHY link up and RX is active, make LED0 ON at least 10ms;
6	Led_gt_on_en_1	RW	0x1	1 = If BLINK status is not activated, when PHY link up and speed mode is 1000M, make LED0 ON;
5	Led_ht_on_en_1	RW	0x1	1 = If BLINK status is not activated, when PHY link up and speed mode is 100M, make LED0 ON;
4	Led_bt_on_en_1	RW	0x0	Not used
3	Led_col_blk_en_1	RW	0x0	Not used
2	Led_gt_blk_en_1	RW	0x0	1 = If PHY link up and speed mode is 1000M, make LED0 BLINK
1	Led_ht_blk_en_1	RW	0x0	1 = If PHY link up and speed mode is 100M, make LED0 BLINK
0	Led_bt_blk_en_1	RW	0x0	Not used

4.4.11 LED Control Register2 (0x9064)

Bit	Symbol	Access	Default	Description
15:14	freq_sel_f2	RW	0x1	Select the frequency of Blink Mode2: 00: 2Hz; 01: 4Hz; 10: 8Hz; 11: 16Hz.
13:12	freq_sel_f1	RW	0x2	Select the frequency of Blink Mode1: 00: 2Hz; 01: 4Hz;

Bit	Symbol	Access	Default	Description
				10: 8Hz; 11: 16Hz.
9	dis_led_an_try	RW	0x0	1=disable LED when AN tries to link up
8:0	led_force_ctrl	RW	0x0	LED force mode control

4.4.12 Cable Status Diagnostics Register1 (0x9090)

Bit	Symbol	Access	Default	Description
15	csd_ca_en	OC	0x0	1=Enable CSD detection, when detect finished, it was self-cleared
14	open_flag_ca	RO	0x0	1=Open point was detected on cable
13	short_flag_ca	RO	0x0	1=Short point was detected on cable
9	csd_ca_clr	RC	0x0	Not Used
8:0	length_ca	RO	0x0	Detect results to indicate the open/short position on cable

4.4.13 Cable Status Diagnostics Register2 (0x9092)

Bit	Symbol	Access	Default	Description
15:7	csd_ca_shift_to	RW	0xc8	
6:0	csd_ca_prm_thres	RW	0x46	

4.4.14 Cable Status Diagnostics Register3 (0x9095)

Bit	Symbol	Access	Default	Description
15:8	csd_ca_cor_thres_med_m	RW	0x3a	
7:0	csd_ca_cor_thres_sht_m	RW	0x3a	

4.4.15 Cable Status Diagnostics Register4 (0x9096)

Bit	Symbol	Access	Default	Description
15:8	csd_ca_cor_thres_sht_s	RW	0x3a	
7:0	csd_ca_cor_thres_lng_m	RW	0x1a	

4.4.16 Cable Status Diagnostics Register5 (0x9097)

Bit	Symbol	Access	Default	Description
15:8	csd_ca_cor_thres_lng_s	RW	0x1a	
7:0	csd_ca_cor_thres_med_s	RW	0x3a	

4.4.17 Cable Status Diagnostics Register6 (0x9099)

Bit	Symbol	Access	Default	Description
9:8	pi_clktx_hs_ctr_csd	RW	0x3	
6:0	tx_mux_cfg_csd	RW	0x31	

4.4.18 Cable Status Diagnostics Register7 (0x909a)

Bit	Symbol	Access	Default	Description
5:4	pi_clkrx_ctr2_csd	RW	0x2	
3:0	pi_clkrx_ctr1_csd	RW	0x6	

4.4.19 Cable Status Diagnostics Register8 (0x909c)

Bit	Symbol	Access	Default	Description
6:0	near_echo_positon	RW	0x13	

4.4.20 LED Control Register3 (0x90a0)

Bit	Symbol	Access	Default	Description
15	led_enable	RW	0x1	1= Enable LED
14	led_polar	RW/STRAP	0x1	LED polarity config 1=Output high, LED active low; 0=output low, LED active high.
13	led_rtct	RW	0x0	1=Enable LED blink when VCT done
12	led_func_oen	RW	0x0	Config OEN of LED PAD manually
11:6	LED_RSVD	RW	0x18	Not used
5:4	led_blink_duty	RW	0x2	Select the duty cycle of Blink: 000: 50% ON and 50% OFF; 001: 67% ON and 33% OFF; 010: 75% ON and 25% OFF; 011: 83% ON and 17% OFF; 100: 50% ON and 50% OFF; 101: 33% ON and 67% OFF; 110: 25% ON and 75% OFF; 111: 17% ON and 83% OFF.
3:2	led_blink_freq	RW	0x1	Not used
1	led_act	RW	0x1	1=Enable LED work in packet active mode
0	led_link	RW	0x1	1=Enable LED works in Link indication mode

4.4.21 RGMII Config Register8 (0x9110)

Bit	Symbol	Access	Default	Description
15:8	csr_rg_rfu_da_2p5	RW	0x0	Reserved for internal usage
7:0	csr_rg_rfu_dh_2p5	RW	0x10	Reserved for internal usage

4.4.22 RGMII Config Register9 (0x9111)

Bit	Symbol	Access	Default	Description
2:0	csr_rg_dr_rout_cfg_2p5	RW	0x5	Reserved for internal usage

4.4.23 RGMII Config Register10 (0x9112)

Bit	Symbol	Access	Default	Description
3:2	csr_dr_cc_cfg_rxd_2p5	RW	0x3	Reserved for internal usage
1:0	csr_dr_cc_cfg_rxc_2p5	RW	0x3	Reserved for internal usage

4.4.24 RGMII Config Register11 (0x9113)

Bit	Symbol	Access	Default	Description
7:6	csr_dr_chg_tf_cfg_rxd_2p5	RW	0x0	Reserved for internal usage
5:4	csr_dr_chg_tf_cfg_rxc_2p5	RW	0x0	Reserved for internal usage
3:2	csr_dr_chg_tr_cfg_rxd_2p5	RW	0x0	Reserved for internal usage
1:0	csr_dr_chg_tr_cfg_rxc_2p5	RW	0x1	Reserved for internal usage

4.4.25 RGMII Config Register12 (0x9114)

Bit	Symbol	Access	Default	Description
15:8	csr_dr_chg_main_cfg_rxd_2p5	RW	0x39	Reserved for internal usage
7:0	csr_dr_chg_main_cfg_rxc_2p5	RW	0x39	Reserved for internal usage

4.4.26 RGMII Config Register13 (0x9115)

Bit	Symbol	Access	Default	Description
15:8	csr_rg_rfu_da_1p8	RW	0x0	Reserved for internal usage
7:0	csr_rg_rfu_dh_1p8	RW	0x10	Reserved for internal usage

4.4.27 RGMII Config Register14 (0x9116)

Bit	Symbol	Access	Default	Description
2:0	csr_rg_dr_rout_cfg_1p8	RW	0x6	Reserved for internal usage

4.4.28 RGMII Config Register15 (0x9117)

Bit	Symbol	Access	Default	Description
3:2	csr_dr_cc_cfg_rxd_1p8	RW	0x3	Reserved for internal usage
1:0	csr_dr_cc_cfg_rxc_1p8	RW	0x3	Reserved for internal usage

4.4.29 RGMII Config Register16 (0x9118)

Bit	Symbol	Access	Default	Description
7:6	csr_dr_chg_tf_cfg_rxd_1p8	RW	0x0	Reserved for internal usage
5:4	csr_dr_chg_tf_cfg_rxc_1p8	RW	0x0	Reserved for internal usage
3:2	csr_dr_chg_tr_cfg_rxd_1p8	RW	0x0	Reserved for internal usage
1:0	csr_dr_chg_tr_cfg_rxc_1p8	RW	0x0	Reserved for internal usage

4.4.30 RGMII Config Register17 (0x9119)

Bit	Symbol	Access	Default	Description
15:8	csr_dr_chg_main_cfg_rxd_1p8	RW	0x39	Reserved for internal usage
7:0	csr_dr_chg_main_cfg_rxc_1p8	RW	0x39	Reserved for internal usage

4.5 SDS MII Register

4.5.1 Basic Control Register (0x00)

Bit	Symbol	Access	Default	Description
15	Reset	RW/SC	0x0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically.
14	Loopback	RW	0x0	Internal loopback control
13	Speed_Selection(LSB)	RW	0x0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero.
12	Autoneg_En	RW	0x1	1: Enable auto-negotiation;

Bit	Symbol	Access	Default	Description
11	Power_down	RW	0x0	1 = Power down
10	Isolate	RW	0x0	Isolate PHY from RGMII/SGMII/FIBER.
9	Re_Autoneg	RW/SC	0x0	Auto-Negotiation automatically restarts after hardware or software reset regardless of bit[9] RESTART.
8	Duplex_Mode	RW	0x1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.
7	Collision_Test	RW	0x0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted.
6	Speed_Selection(MSB)	RW	0x1	See bit13.
5	mr_unidirectional	RW	0x0	
4:0	Reserved	RO	0x0	Reserved. Write as 0, ignore on read

4.5.2 Basic Status Register (0x01)

Bit	Symbol	Access	Default	Description
15	100BASE-T4	RO	0x0	PHY doesn't support 100BASE-T4
14	100BASE-X_Fd	RO	0x1	PHY supports 100BASE-X_FD
13	100BASE-X_Hd	RO	0x0	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	0x0	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	0x0	PHY supports 10Mbps_Hd
10	100BASE-T2_Fd	RO	0x0	PHY doesn't support 100BASE-T2_Fd
9	100BASE-T2_Hd	RO	0x0	PHY doesn't support 100BASE-T2_Hd
8	Extended_Status	RO	0x1	Whether support extended status register in 0Fh
7	Unidirect_Ability	RO	0x1	1'b0: PHY can transmit from MII only when the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	0x1	1'b0: PHY will not accept management frames with preamble suppressed
5	Autoneg_Complete	RO	0x0	1'b0: Auto-negotiation process not completed
4	Remote_Fault	RO RC SWC LH	0x0	1'b0: No remote fault condition detected
3	Autoneg_Ability	RO	0x1	1'b0: PHY can not perform Auto-negotiation
2	Link_Status	RO SWC LL	0x0	Link status
1	Jabber_Detect	RO	0x0	always 0
0	Extended_Capability	RO	0x1	To indicate whether support extended registers, to access from address register 1Eh and data register 1Fh

4.5.3 SDS Identification Register1 (0x02)

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	0x4f51	Bits 3 to 18 of the Organizationally Unique Identifier

4.5.4 SDS Identification Register2 (0x03)

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	0x3A	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	0x30	6 bits manufacturer's type number
3:0	Revision_No	RO	0x1	4 bits manufacturer's revision number

4.5.5 Auto-Negotiation Advertisement (0x04)

Bit	Symbol	Access	Default	Description
15	NEXT_Page	RW	0x0	Reserved. NEXT page exchange of SGMII/1000BASE-X Auto-negotiation is not supported in this IC.
14	Ack	RO	0x0	Always 0
13:12	Remote_Fault	RO	0x0	Always 0
11:9	Reserved	RO	0x0	Reserved
8	Asymmetric_Pause	RW	0x1	This bit is updated immediately after the writing operation; However, the configuration does not take effect until any of the following occurs: ● Software reset is asserted by writing register 0x0 bit[15] ● Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] ● The port is switched from power down to normal operation by writing register 0x0 bit[11] ● Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
7	Pause	RW	0x1	This bit is updated immediately after the writing operation; However, the configuration does not take effect until any of the following occurs: ● Software reset is asserted by writing register 0x0 bit[15] ● Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] ● The port is switched from power down to normal operation by writing register 0x0 bit[11]

Bit	Symbol	Access	Default	Description
				● Link goes down 1 = Symmetric Pause 0 = No symmetric Pause
6	Half_duplex	RW	0x0	Half duplex ability
5	Full_duplex	RW	0x1	Full duplex ability
4:0	Reserved	RO	0x0	Reserved

4.5.6 Auto-Negotiation Link Partner Ability (0x05)

Bit	Symbol	Access	Default	Description
15	NEXT Page	RO SWC	0x0	NEXT page. Received Code Word Bit 15
14	ACK	RO SWC	0x0	Acknowledge. Received Code Word Bit 14
13:12	REMOTE_FAULT	RO SWC	0x0	Remote Fault. Received Code Word Bit 13:12
11:9	RESERVED	RO	0x0	Reserved.
8:7	PAUSE	RO SWC	0x0	Pause. Received Code Word Bit 8:7
6	HALF_DUPLEX	RO SWC	0x0	Half duplex. Received Code Word Bit 6
5	FULL_DUPLEX	RO SWC	0x0	Full duplex. Received Code Word Bit 5
4:0	RESERVED	RO	0x0	Reserved.

4.5.7 Auto-Negotiation Expansion Register (0x06)

Bit	Symbol	Access	Default	Description
15:3	Reserved	RO	0x0	Reserved
2	Local NEXT Page able	RO	0x0	1 = Local Device supports NEXT Page
1	Page received	RO RC LH	0x0	1 = A new page is received
0	Reserved	RO	0x0	Reserved

4.5.8 Auto-Negotiation NEXT Page Register (0x07)

Bit	Symbol	Access	Default	Description
15:0	NEXT Page	RO	0x0	always be 0

4.5.9 Auto-Negotiation Link Partner Received NEXT Page Register (0x08)

Bit	Symbol	Access	Default	Description
15:0	Link Partner NEXT Page	RO	0x0	always be 0

4.5.10 Extended Status Register (0x0F)

Bit	Symbol	Access	Default	Description
15	1000BASE-X Full Duplex	RO	0x1	1 = PHY supports 1000BASE-X Full Duplex
14	1000BASE-X Half Duplex	RO	0x0	1 = PHY supports 1000BASE-X Half Duplex
13	1000BASE-T Full Duplex	RO	0x0	1 = PHY supports 1000BASE-T Full Duplex
12	1000BASE-T Half Duplex	RO	0x0	1 = PHY supports 1000BASE-T Half Duplex
11:0	Reserved	RO	0x0	Always 0

4.5.11 SDS Specific Status Register (0x11)

Bit	Symbol	Access	Default	Description
15:14	Speed_mode[1:0]	RO	0x0	These status bits are valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
13	Duplex	RO	0x0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled.
12:11	Pause	RO	0x0	Pause to mac
10	Link status real-time	RO	0x0	1 = Link up
9	Speed_mode[2]	RO	0x0	
8	Duplex_error	RO	0x0	Realtime duplex error
7	En_flowctrl_rx	RO	0x0	Realtime en_flowctrl_rx
6	En_flowctrl_tx	RO	0x0	Realtime en_flowctrl_tx
5:4	Reserved	RO	0x0	Reserved
3:1	Xmit	RO	0x0	Realtime transmit state machine. 001: Xmit Idle 010: Xmit Config 100: Xmit Data
0	Syncstatus	RO	0x0	Realtime sync status

4.5.12 Receive Error Counter MON(0x15)

Bit	Symbol	Access	Default	Description
15:0	error_counter_rx	RO	0x0	Receive error counter

4.5.13 Link Fail Counter MON (0x16)

Bit	Symbol	Access	Default	Description
15	Reserved	RO	0x0	Reserved
14:12	i3_xmit_tx	RO	0x0	State of SGMII TX state machine
11:8	Reserved	RO	0x0	Reserved

Bit	Symbol	Access	Default	Description
7:0	Link_fail_cnt	RO SC	0x0	Link fail counter

4.5.14 Dummy (0x17)

Bit	Symbol	Access	Default	Description
15:0	dummy_mii_reg17	RW	0x0	Reserved for dummy usage

4.6 SDS EXT Register

4.6.1 bp_serdes_link_rst (0x00)

Bit	Symbol	Access	Default	Description
15	bp_serdes_link_rst	RW	0x0	1: to not reset the bridge between PHY and Serdes when Serdes is link down; 0: to reset the bridge.
14	sgtx_fifo_en	RW	0x0	1: to enable the SGMII TX FIFO so the preamble will not be dropped to align tx_even; 0: to bypass the SGMII TX FIFO.
13	en_swrst_selfclr	RW	0x0	1: Serdes SW reset in ext.2.15 is self-cleared; 0: It's not self-cleared, should be written as 0 to clear.
12	en_pcsrst_selfclr	RW	0x0	1: Serdes PCS SW reset in ext.2.8 is self-cleared; 0: It's not self-cleared, should be written as 0 to clear.
11	en_sw_reset_ana	RW	0x0	1: Enable Serdes SW reset to reset analog TX/RX divider, TX/RX data path, and PI code; 0: disable Serdes SW reset to reset analog TX/RX divider, TX/RX data path, and PI code.
10	en_an_on_align_done	RW	0x1	1: Enable SGMII/1000BASE-X restart auto-negotiation when RX alignment is done; 0: Disable.
9	en_reset_ana_aft_en	RW	0x1	1: Enable the analog reset toggle after power on
8:4	Reserved	RO	0x0	Reserved
3	Bp_lnkdn_clk_gating	RW	0x0	For internal use
2	Bp_gmii_fatal_rst	RW	0x1	Not used
1	bp_sgrx_link_failed	RW	0x0	0=when sync status loss SGMII RX go to WAIT_FOR_K; 1=when sync status loss SGMII RX go to LINK_FAILED
0	en_chk_S_inlpi	RW	0x0	

4.6.2 SDS Analog Digital Interface CFG (0x2)

Bit	Symbol	Access	Default	Description
15	Sw_reset	RW	0x0	SDS software reset, high active, self-clear
14	Tx_clk_sel	RW	0x0	Select TX clock phase from analog. 1: Inverted; 0: Non-inverted.
13	Rx_clk_sel	RW	0x1	Select RX clock phase from analog, 1: Inverted; 0: Non-Inverted.
12	Rx_clk_cdr_sel	RW	0x1	Select CDR's RX clock phase from analog 1: Inverted; 0: Non-Inverted.
11	Rot_clk_sel	RW	0x0	Select RX clock phase used to latch the rotator setting 1: Inverted; 0: Non-Inverted.
10	Loopback	RW	0x0	SDS internal loopback
9	Reserved	RO	0x0	always 0.
8	pcs_sw_rst	RW	0x0	SerDes PCS software reset, high active; ext.0.12 control it to be self-clear or not, by default it's not self-clear.
7	Tx_data_mlsb_sel	RW	0x0	1: SWAP MSB and LSB for TX data to analog
6	Rx_data_mlsb_sel	RW	0x1	1: SWAP MSB and LSB of RX data from analog, For FPGA, this is 1'b0 due to PMD difference between FPGA and chip
5	Tx_data_pol_sel	RW	0x0	1: 1 map to 0 and 0 map to 1 for TX data to analog
4	Rx_data_pol_sel	RW	0x0	1: 1 map to 0 and 0 map to 1 for RX data from analog
3	Cdr_data_mlsb_sel	RW	0x0	1: SWAP MSB and LSB of RX data for CDR from analog
2:0	Reserved	RO	0x0	Reserved

4.6.3 SDS PRBS CFG2 (0x5)

Bit	Symbol	Access	Default	Description
15	En_prbs	RW	0x0	Enable TX PRBS or self-defined pattern, the pattern type is determined by bit7:5 test_mode.
14	En_bert	RW	0x0	Enable Bit Error Rate Test;
13	Prbs_invert	RW	0x0	TX error injection function, it has the highest polarity than prbs_err_once and prbs_err_cont. 1: Send polarity inverted PRBS or self-defined pattern;

Bit	Symbol	Access	Default	Description
12	Prbs_err_cont	RW	0x0	TX error injection function has the lowest polarity. 1: Inject error on TX pattern continuously and periodic, the period is controlled by prbs_err_rate.
11:10	Prbs_err_rate	RW	0x0	It's valid only when prbs_err_cont is 1. 2'b00: Inject one error every 1024 cycles; 2'b01: Inject one error every 2048 cycles; 2'b10: Inject one error every 4096 cycles; 2'b11: Inject one error every 8192 cycles;
9	Prbs_err_once	RW	0x0	TX error injection function. At the rising of this bit, to send polarity inverted PRBS or self-defined pattern for one cycle;
8	Test_mode_prbs31	RW	0x0	1: PRBS31, bit7:5 test_mode[2:0] has no effect.0: not PRBS31, bit7:5 test_mode[2:0] take effect then.
7:5	Test_mode	RW	0x0	Control the TX pattern in test mode: 0x0, PRBS7; 0x1, PRBS10; 0x2, Fix pattern, the fix pattern is controlled by Ext.6; 0x3, 010101…; 0x4, 00110011…; 0x5, 00000_11111_00000_11111…; 0x6, 0000_0000_00_1111_1111_11…; 0x7, Increase pattern, 0->1023->0->1023…
4	Duration_check_en	RW	0x0	Enable fixed number of bits check define in SDS EXT BA/BB
3:0	Reserved	RO	0x0	Reserved

4.6.4 SDS PRBS CFG2 (0x6)

Bit	Symbol	Access	Default	Description
15:10	Reserved	RO	0x0	Reserved
9:0	Fix_pattern_9_0	RW	0x0	Fix pattern transmitted in test_mode 2

4.6.5 SDS PRBS MON1 (0x8)

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	0x0	Reserved
8	Err	RO	0x0	Error flag after PRBS has synchronized
7:2	Reserved	RO	0x0	Reserved
1	Bitsync_latch	RO LL	0x0	PRBS test synchronization status, once the sync is lost, this bit will latch low, until it's been read out.

Bit	Symbol	Access	Default	Description
0	Bitsync	RO	0x0	Real-time synchronization status

4.6.6 SDS PRBS MON2 (0x9)

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_15_0	RO	0x0	Real-time lowest 16 bits received error bit counter

4.6.7 SDS PRBS MON3 (0xa)

Bit	Symbol	Access	Default	Description
15:0	Err_cnt_31_16	RO	0x0	Real-time highest 16 bits received error bit counter

4.6.8 SDS PRBS MON4 (0xb)

Bit	Symbol	Access	Default	Description
15:0	Good_cnt_15_0	RO	0x0	Real-time lowest 16 bits received good bit counter

4.6.9 SDS PRBS MON5 (0xc)

Bit	Symbol	Access	Default	Description
15:0	Good_cnt_31_16	RO	0x0	Real-time highest 16 bits received good bit counter

4.7 PTP Register

4.7.1 PTP Config Register1 (0x8000)

Bit	Symbol	Access	Default	Description
12	EN_1588_ADDR_INCR	RW	0x0	Enable address increase automatically for 1588 reg access to speed up
11	SW_RST_1588	RW	0x0	Soft reset 1588-related function.
10	EN_IGNORE_MAC_ADDR	RW	0x0	Enable ignore MAC packet address.
9	EN_IGNORE_IPV4_ADDR	RW	0x0	Enable ignore IPV4 packet address.
8	EN_IGNORE_IPV6_ADDR	RW	0x0	Enable ignore IPV6 packet address.
7	EN_GATE_1588	RW	0x1	Enable gating 1588 clock domain.
6	EN_IPV6_CHKSUM_FIX0	RW	0x0	Enable force IPV6 UDP checksum to 0.
5	EN_IPV4_CHKSUM_FIX0	RW	0x0	Enable force IPV4 UDP checksum to 0.
4	BP_1588	RW	0x1	0 = PTP timestamp engine normal operation.

Bit	Symbol	Access	Default	Description
				1 = Bypass IEEE1588v2 related functions.
3:2	RTC_CLK_SEL	RW	0x0	RTC clock source: 2'b00: ADC clock, after rotator; 2'b01: DAC clock; 2'b10: ADC clock, before rotator; 2'b11: SYNC_IN.
1:0	PTP_CLK_TYPE	RW	0x0	PTP clock mode setting 00 = Ordinary/boundary two-step clock 01 = Ordinary/boundary one-step clock 10 = Transparent two-step clock 11 = Transparent one-step clock

4.7.2 PTP Config Register2 (0x8001)

Bit	Symbol	Access	Default	Description
8:5	GPIO_MODE_SEL	RW	0x0	Select PTP pin input/output: 0000 = PPS input 0001 = PPS pulse output 0010 = 10ms pulse output 0011 = Frequency variable waveform output 0100 = External clock input 0101 = Trigger output 0110 = Event input 0111 = Reserved
4	PTP_MODE_SEL	RW	0x0	1: PTP mode 0: gPTP mode (802.1AS)
3	EN_FIX_IGS_DLY	RW	0x0	Enable config fixed ingress time delay.
2	EN_FIX_EGS_DLY	RW	0x0	Enable config fixed egress time delay.
1	EN_EMB_PRSPTS_2FU	RW	0x0	1 = In two step clock, embed the time stamp of the last egressed Pdelay_resp message to the next Pdelay_followup message.
0	EN_EMB_SYNCTS_2FU	RW	0x0	1 = In two step clock, embed the time stamp of the last egressed Sync message to the next follow up message.

4.7.3 PTP Config Register3 (0x8002)

Bit	Symbol	Access	Default	Description
3	EMB_TS_2PRSP_CF_MSB	RW	0x0	1 = Embed the time stamp of Pdelay_resp message correction field
2	EN_EMB_IGS_TS_PRSP	RW	0x0	1 = Embed the time stamp of the ingress Pdelay_resp message to the same message forwarding to MAC.

Bit	Symbol	Access	Default	Description
1	EN_EMB_IGS_TS_PREQ	RW	0x0	1 = Embed the time stamp of ingress Pdelay_req message to the same message forwarding to MAC.
0	EN_EMB_IGS_TS_SYNC	RW	0x0	1 = Embed the time stamp of ingress Sync message to the same message forwarding to MAC.

4.7.4 PTP Config Register4 (0x8003)

Bit	Symbol	Access	Default	Description
15:0	EGS_DLY	RW	0x0	The egress latency that from the plane measuring the egress time stamp to the reference plane.

4.7.5 PTP Config Register5 (0x8004)

Bit	Symbol	Access	Default	Description
15:0	IGS_DLY	RW	0x0	The ingress latency that from the reference plane to the plane measuring the egress time stamp.

4.7.6 PTP Config Register6 (0x8016)

Bit	Symbol	Access	Default	Description
15:0	igs_ts_i[79:64]	RO	0x0	8016h~8019h store the LOW 64-bit of the timestamp for the last received 1588 event packet.

4.7.7 PTP Config Register7 (0x8017)

Bit	Symbol	Access	Default	Description
15:0	igs_ts_i[63:48]	RO	0x0	See description in 8016h.

4.7.8 PTP Config Register8 (0x8018)

Bit	Symbol	Access	Default	Description
15:0	igs_ts_i[47:32]	RO	0x0	See description in 8016h.

4.7.9 PTP Config Register9 (0x8019)

Bit	Symbol	Access	Default	Description
15:0	igs_ts_i[31:16]	RO	0x0	See description in 8016h.

4.7.10 PTP Config Register10 (0x801a)

Bit	Symbol	Access	Default	Description
15:0	igs_ts_i[15:0]	RO	0x0	See description in 8016h.

4.7.11 PTP Config Register11 (0x801b)

Bit	Symbol	Access	Default	Description
15:12	igs_msg_type_i[3:0]	RO	0x0	The message type of the last received 1588 event packet.
11:0	igs_ts_frc_i[19:8]	RO	0x0	Store the 20-bit fraction part of the timestamp of the last received 1588 event packet. (801c[7:0])

4.7.12 PTP Config Register12 (0x801c)

Bit	Symbol	Access	Default	Description
7:0	igs_ts_frc_i[7:0]	RO	0x0	Igs_ts_frc[19:0] is the fractional part of the ingress time stamp.

4.7.13 PTP Config Register13 (0x8026)

Bit	Symbol	Access	Default	Description
15:0	egs_ts_i[79:64]	RO	0x0	8026h~8029h store the LOW 64-bit of the timestamp of the last transmitted 1588 event packet.

4.7.14 PTP Config Register14 (0x8027)

Bit	Symbol	Access	Default	Description
15:0	egs_ts_i[63:48]	RO	0x0	See description in 8026h.

4.7.15 PTP Config Register15 (0x8028)

Bit	Symbol	Access	Default	Description
15:0	egs_ts_i[47:32]	RO	0x0	See description in 8026h.

4.7.16 PTP Config Register16 (0x8029)

Bit	Symbol	Access	Default	Description
15:0	egs_ts_i[31:16]	RO	0x0	See description in 8026h.

4.7.17 PTP Config Register17 (0x802a)

Bit	Symbol	Access	Default	Description
15:0	egs_ts_i[15:0]	RO	0x0	See description in 8026h.

4.7.18 PTP Config Register18 (0x802b)

Bit	Symbol	Access	Default	Description
15:12	egs_msg_type_i[3:0]	RO	0x0	Parserd egress PTP message type.
11:0	egs_ts_frc_i[19:8]	RO	0x0	Egs_ts_frc[19:0] is the fractional part of the ingress PTP message's time stamp.

4.7.19 PTP Config Register19 (0x802c)

Bit	Symbol	Access	Default	Description
7:0	egs_ts_frc_i[7:0]	RO	0x0	Egs_ts_frc[19:0] is the fractional part of the ingress PTP message's time stamp.

4.7.20 PTP Config Register20 (0x8030)

Bit	Symbol	Access	Default	Description
15:0	ORG_CORRECT[15:0]	RW	0x0	Config origin correction field value.

4.7.21 PTP Config Register21 (0x8040)

Bit	Symbol	Access	Default	Description
15:0	RTC_STEP[31:16]	RW	0x0	The integer part of the RTC step[31:26], MSB 10bits of the decimal part of the RTC step[25:16].

4.7.22 PTP Config Register22 (0x8041)

Bit	Symbol	Access	Default	Description
15:0	RTC_STEP[15:0]	RW	0x0	LSB 16bits of the decimal part of the RTC step.

4.7.23 PTP Config Register23 (0x8042)

Bit	Symbol	Access	Default	Description
15:0	OFFSET_NANO[31:16]	RW	0x0	Nanosecond field of RTC offset.

4.7.24 PTP Config Register24 (0x8043)

Bit	Symbol	Access	Default	Description
15:0	OFFSET_NANO[15:0]	RW	0x0	Nanosecond field of RTC offset.

4.7.25 PTP Config Register25 (0x8044)

Bit	Symbol	Access	Default	Description
15:0	OFFSET_SEC[47:32]	RW	0x0	Second field of RTC offset.

4.7.26 PTP Config Register26 (0x8045)

Bit	Symbol	Access	Default	Description
15:0	OFFSET_SEC[31:16]	RW	0x0	Second field of RTC offset.

4.7.27 PTP Config Register27 (0x8046)

Bit	Symbol	Access	Default	Description
15:0	OFFSET_SEC[15:0]	RW	0x0	Second field of RTC offset.

4.7.28 PTP Config Register28 (0x8060)

Bit	Symbol	Access	Default	Description
9	RTC_INT_WIDTH_SEL	RW	0x0	To select IEEE1588 interrupt's pulse width. 0 = 10ms. 1 = 1/128=7.8125ms.
8:6	OUT_WAVE_SEL	RW	0x0	Select the final output of 1588 frequency output pin.

Bit	Symbol	Access	Default	Description
				000 = variable frequency output. The period is specified in 3.1095~3.1097 WAVE_PERIOD; 010 = 10ms pulse output, 50% duty cycle; 101 = Trigger channel 0 output; 111 = Ingress TS valid; others = 0.
5	RTC_RECORD_WAY	RW	0x0	0 = Normally read mode. 1 = Snapshot mode.
4	TRIG_RTC	D2/SC	0x0	Set it to 1 snapshot RTC value to rtc_real_time registers 3.1048~3.104E. This bit is self-clearing and always reads back as 0. This bit is valid only when RTC_RECORD_WAY is 1.
3	SYNC_ASYNC_ACT_INCVAL	RW	0x0	The mode of how RTC_STEP 3.1040~1.1041 takes effect: 0 = RTC_STEP takes effect asynchronously. 1 = RTC_STEP takes effect synchronously after EN_INCVAL is set.
2	EN_INCVAL	D2/SC	0x0	Set it to 1 generates a high pulse to indicate the RTC_STEP is valid. This bit is self-clearing and always reads back as 0. This bit is valid only when SYNC_ASYNC_ACT_INCVAL is 1.
1	CLEAR_RTC	D2/SC	0x0	Set it to 1 clears RTC to 0. This bit is self-clearing and always reads back as 0.
0	LOAD_RTC	D2/SC	0x0	Set it to 1 load value 8061~8065 RTC_PRELOAD to RTC. This bit is self-clearing and always reads back as 0.

4.7.29 PTP Config Register29 (0x8070)

Bit	Symbol	Access	Default	Description
6	EN_GM_MODE	RW	0x0	RTC grandmaster mode select. 0 = RTC is not in grandmaster mode. 1 = RTC is in grandmaster mode.
5	RTC_SYNC_W_PPS	RW	0x0	0 = RTC runs at the local reference clock. 1 = RTC runs at reference clock driven by SYNC_IN input.
4	HW_SW_GM_PLL	RW	0x0	The way digital PLL is implemented in grandmaster mode. 0 = PLL implemented by software. 1 = PLL implemented by hardware.
3:0	GM_MAXFREQ_OFFSET	RW	0x0	Maximum frequency offset of RTC reference clock from SYNC_IN input clock source in Grandmaster mode. 0000=1PPM. 0001=10PPM. 0010=50PPM. 0011=100PPM. 0100=150PPM.

Bit	Symbol	Access	Default	Description
				0101=200PPM. 0110=250PPM. 0111=300PPM. Other=0PPM.

4.7.30 PTP Config Register30 (0x8071)

Bit	Symbol	Access	Default	Description
13:8	GM_PLL_C0	RW	0x0	Base 2 logarithm of proportional part coefficient of hardware digital PLL GM_PLL_C0 [5] control C0 be >1 or <1: 0 = Left shift, >1; 25= Right shift, <1; GM_PLL_C0 [4:0] is the shift count. Usually, C0 being 1/2 or 1 (right shift by 1 or no shift) will have good performance.
5:0	GM_PLL_C1	RW	0x0	Base 2 logarithm of integral part coefficient of hardware digital PLL GM_PLL_C1[5] control C1 be >1 or <1: 0 = Left shift, >1; 26= Right shift, <1. GM_PLL_C1[4:0] is the shift bits. Usually, C1 being 1/8 or 1/16 (right shift 3 or 4) will have good performance.

4.7.31 PTP Config Register31 (0x80a0)

Bit	Symbol	Access	Default	Description
8	TRIG0_START	D2/SC	0x0	1 = Start trigging time stamp
7	TRIG0_FORCE	D2/SC	0x0	1 = Force trigger finished
6:0	TRIG0_CTR	RW	0x0	Bit0 = Enable Trigger Bit1 = Force trigger output is a fixed value Bit2 = Trigger interrupt Bit[5:3] = Config trigger pattern Bit6 = 0, Don't trigger anything; Bit6 = 1, trigger immediately

4.7.32 PTP Config Register32 (0x80a1)

Bit	Symbol	Access	Default	Description
3:0	trig0_status_i	RO	0x0	Bit0 = Trigger finished flag Bit1 = Trigger active flag Bit[3:2] = Trigger error flag

4.7.33 PTP Config Register33 (0x80a4)

Bit	Symbol	Access	Default	Description
15:0	TRIG0_TIME[79:64]	RW	0x0	The time that “Trig0” will trigger.

4.7.34 PTP Config Register34 (0x80a5)

Bit	Symbol	Access	Default	Description
15:0	TRIG0_TIME[63:48]	RW	0x0	See description in 80a4h.

4.7.35 PTP Config Register35 (0x80a6)

Bit	Symbol	Access	Default	Description
15:0	TRIG0_TIME[47:32]	RW	0x0	See description in 80a4h.

4.7.36 PTP Config Register36 (0x80a7)

Bit	Symbol	Access	Default	Description
15:0	TRIG0_TIME[31:16]	RW	0x0	See description in 80a4h.

4.7.37 PTP Config Register37 (0x80a8)

Bit	Symbol	Access	Default	Description
15:0	TRIG0_TIME[15:0]	RW	0x0	See description in 80a4h.

5 Timing and DC/AC Characteristics

5.1 DC Characteristics

5.1.1 Digital IO Characteristics

Table 13 Digital IO Characteristics

Symbol	Description	Min	Typ	Max	Unit
V_{OH} (3.3V)	Minimum High Level Output Voltage	2.6	-	3.63	V
V_{OL} (3.3V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
V_{OH} (2.5V)	Minimum High Level Output Voltage	2.0	-	2.8	V
V_{OL} (2.5V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
V_{OH} (1.8V)	Minimum High Level Output Voltage	1.6	-	2.1	V
V_{OL} (1.8V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
V_{IH} (3.3V)	Minimum High Level Input Voltage	2	-	-	V
V_{IL} (3.3V)	Maximum Low Level Input Voltage	-	-	0.8	V
V_{IH} (2.5V)	Minimum High Level Input Voltage	1.7	-	-	V
V_{IL} (2.5V)	Maximum Low Level Input Voltage	-	-	0.7	V
V_{IH} (1.8V)	Minimum High Level Input Voltage	1.3	-	-	V
V_{IL} (1.8V)	Maximum Low Level Input Voltage	-	-	0.5	V
I_H	Leakage Current, Power on 3.3V	0	-	65	μA
I_L	Leakage Current, Power off	-	0	12	μA

Note: Digital IO pins include MDC, MDIO, INTB, PHYRSTB, DISB, LED/PTP_GPIO, TXC, TXEN, TXD[3:0], RXC, RXDV, and RXD[3:0].

5.1.2 Under Voltage DC Characteristics

Table 14 Under Voltage DC Characteristics

Symbol	Description	Min	Typ	Max	Unit
Pin VDD33_AUX(YT8011AN/AR)					
$V_{uvd\_VDD33\_AUX}$	Under voltage detection voltage on VDD33_AUX pin	-	2.77	-	V
$V_{uvr\_VDD33\_AUX}$	Under voltage recovery voltage on VDD33_AUX pin	-	2.82	-	V
$V_{uvhys\_VDD33\_AUX}$	Under voltage hysteresis voltage on VDD33_AUX pin	-	50	-	mV
Pin AVDD33					
V_{uvd_AVDD33}	Under voltage detection voltage on AVDD33 pin	-	3.03	-	V
V_{uvr_AVDD33}	Under voltage recovery voltage on AVDD33 pin	-	3.08	-	V
V_{uvhys_AVDD33}	Under voltage hysteresis voltage on AVDD33 pin	-	50	-	mV
T_{uvd_AVDD33}	Under voltage detection time	-	16	-	μs
T_{uvr_AVDD33}	Under voltage recovery time	-	8	-	μs
T_{tout_AVDD33}	Under voltage timeout to Sleep	-	100	-	ms
Pin AVDD09/DVDD09					
V_{uvd_AVDD09}	Under voltage detection voltage on AVDD09 pin	-	0.82	-	V

Symbol	Description	Min	Typ	Max	Unit
V_{uvr_AVDD09}	Under voltage recovery voltage on AVDD09 pin	-	0.84	-	V
V_{uvhys_AVDD09}	Under voltage hysteresis voltage on AVDD09 pin	-	20	-	mV
T_{uvd_AVDD09}	Under voltage detection time	-	16	-	μs
T_{uvr_AVDD09}	Under voltage recovery time	-	8	-	μs
T_{tout_AVDD09}	Under voltage timeout to Sleep	-	100	-	ms
Pin DVDDIO (3.3V)					
V_{uvd_DVDDIO}	Under voltage detection voltage on DVDDIO pin	-	3.03	-	V
V_{uvr_DVDDIO}	Under voltage recovery voltage on DVDDIO pin	-	3.06	-	V
V_{uvhys_DVDDIO}	Under voltage hysteresis voltage on DVDDIO pin	-	30	-	mV
T_{uvd_DVDDIO}	Under voltage detection time	-	16	-	μs
T_{uvr_DVDDIO}	Under voltage recovery time	-	8	-	μs
T_{tout_DVDDIO}	Under voltage timeout to Sleep	-	100	-	ms
Pin DVDDIO (2.5V)					
V_{uvd_DVDDIO}	Under voltage detection voltage on DVDDIO pin	-	2.28	-	V
V_{uvr_DVDDIO}	Under voltage recovery voltage on DVDDIO pin	-	2.31	-	V
V_{uvhys_DVDDIO}	Under voltage hysteresis voltage on DVDDIO pin	-	30	-	mV
T_{uvd_DVDDIO}	Under voltage detection time	-	16	-	μs
T_{uvr_DVDDIO}	Under voltage recovery time	-	8	-	μs
T_{tout_DVDDIO}	Under voltage timeout to Sleep	-	100	-	ms
Pin DVDDIO (1.8V)					
V_{uvd_DVDDIO}	Under voltage detection voltage on DVDDIO pin	-	1.64	-	V
V_{uvr_DVDDIO}	Under voltage recovery voltage on DVDDIO pin	-	1.65	-	V
V_{uvhys_DVDDIO}	Under voltage hysteresis voltage on DVDDIO pin	-	10	-	mV
T_{uvd_DVDDIO}	Under voltage detection time	-	16	-	μs
T_{uvr_DVDDIO}	Under voltage recovery time	-	8	-	μs
T_{tout_DVDDIO}	Under voltage timeout to Sleep	-	100	-	ms

5.1.3 Sleep Mode DC Characteristics

Table 15 WAKE/INH DC Characteristics

Symbol	Description	Min	Typ	Max	Unit
Pin INH(YT8011AN/AR)					
V_{OH_INH}	High level output voltage IOH=-1mA, VDD33_AUX=3.3V	VDD33_AUX-0.3	-	VDD33_AUX	V
V_{OH_INH}	High level output voltage IOH=-4mA, VDD33_AUX=3.3V	VDD33_AUX-2	-	VDD33_AUX	V
$I_{leakage}$	Leakage current, power off	-	-	12	μA
Pin WAKE(YT8011AN/AR)					
V_{IH_WAKE}	High level input voltage, sleep mode	2.6	-	-	V
V_{IL_WAKE}	Low level input voltage, sleep mode	-	-	0.5	V
T_{det_wake1}	Local WAKE event detection time 1	40	-	-	μs
T_{det_wake2}	Local WAKE event detection time 2	10	-	-	ms

Symbol	Description	Min	Typ	Max	Unit
T_{det_rwake}	Remote WAKE event detection time, through MDIP and MDIN	-	-	2	ms

Note: Wake event detection edge and time can be changed by registers in 4.2 PHY EXT Register.

5.1.4 Transmitter DC Characteristics

Table 16 1000BASE-T1 Template Requirement

Symbol	Description	Min	Typ	Max	Unit
Clock Frequency	TX Clock Frequency	124.9875	-	125.0125	MHz
	TX Symbol Frequency	749.925	-	750.075	MHz
MDI Jitter	MDI Jitter RMS	-	-	5	ps
	MDI Jitter Pk-Pk	-	-	50	ps
Output Droop	Positive Output Droop	-	-	10	%
	Negative Output Droop	-	-	10	%
Power Spectral Density and Power Level	TX Power Spectral Density	-	-	0	Hits
	Power Level	-	-	5	dBm
Peak Differential Output	TX Peak Diff Output	-	-	1.3	VPP
Master Jitter	Master Jitter RMS	-	-	5	ps
	Master Jitter Pk-Pk	-	-	50	ps
Slave Jitter	Slave Jitter RMS	-	-	10	ps
	Slave Jitter Pk-Pk	-	-	100	ps
Distortion	TX Distortion	-	-	15	mV
Clock Frequency	TX Clock Frequency	124.9875	-	125.0125	MHz
Return loss	MDI Return loss	-	-	0	Hits
	MDI conversion mode loss	-	-	0	Hits

Table 17 100BASE-T1 Template Requirement

Symbol	Description	Min	Typ	Max	Unit
Clock Frequency	TX Clock Frequency	66.6603	-	66.6736	MHz
Output Droop	Positive Output Droop	-	-	45	%
	Negative Output Droop	-	-	45	%
Power Spectral Density and Power Level	TX Power Spectral Density	-	-	0	Hits
Peak Differential Output	TX Peak Diff Output	-	-	2.2	VPP
Master Jitter	Master Jitter	-	-	50	ps
Slave Jitter	Slave Jitter	-	-	150	ps
Distortion	TX Distortion	-	-	15	mV
Return loss	MDI Return loss	-	-	0	Hits
	MDI conversion mode loss	-	-	0	Hits

Note: Return loss is strongly related to the test environment and is affected by factors such as the impedance of the test board and the quality of the fixture signal.

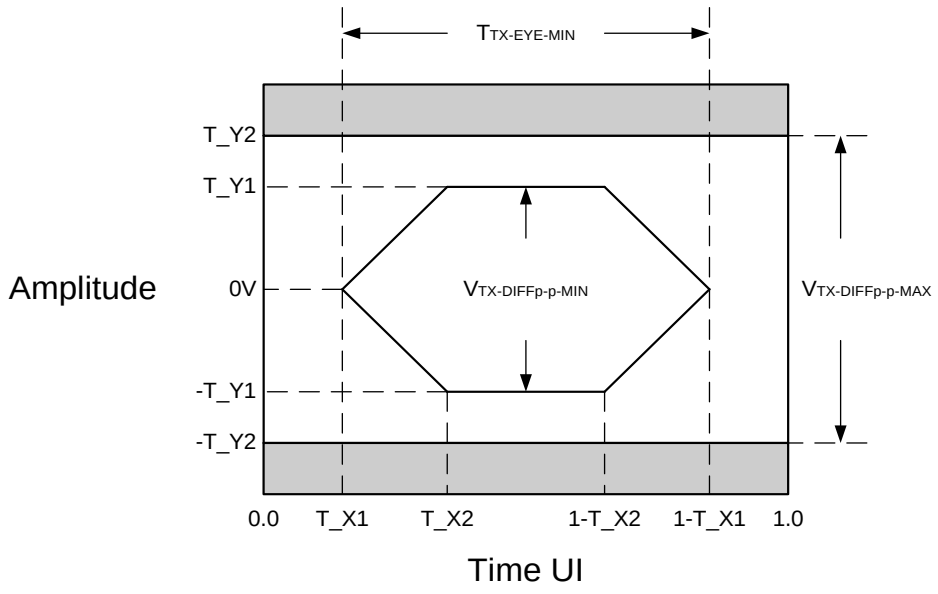
5.2 AC Characteristics

5.2.1 SGMII Differential Transmitter Characteristics

Table 18 SGMII Differential Transmitter Characteristics

Symbol	Description	Min	Typ	Max	Unit	Note
UI	Unit Interval	-	800	-	ps	800ps±100ppm
T_X1	Eye Mask	-	-	0.15	UI	
T_X2	Eye Mask	-	-	0.4	UI	
T_Y1	Eye Mask	150	-	-	mV	
T_Y2	Eye Mask	-	-	0.6*SAVDDL	mV	
$V_{TX-DIFFp-p}$	Output Differential Voltage	0.8*SAVDDL	SAVDDL	1.2*SAVDDL	mV	
T_{TX-EYE}	Minimum TX Eye Width	0.7	-	-	UI	
$T_{TX-JITTER}$	Output Jitter	-	-	0.3	UI	
$T_{TX-RISE}$	Output Rise Time	0.15	-	-	UI	20%~80%
$T_{TX-FALL}$	Output Fall Time	0.15	-	-	UI	20%~80%
R_{TX}	Differential Resistance	80	100	120	ohm	
C_{TX}	AC Coupling Capacitor	80	100	120	nF	
L_{TX}	Transmit Length in PCB(FR4)	-	-	20	inch	

Figure 19 SGMII Differential Transmitter Eye Diagram

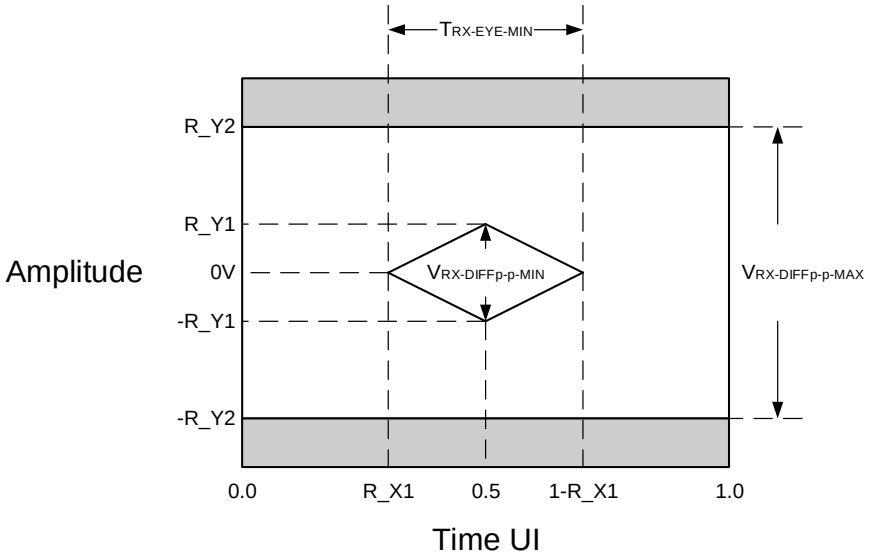


5.2.2 SGMII Differential Receiver Characteristics

Table 19 SGMII Differential Receiver Characteristics

Symbol	Description	Min	Typ	Max	Unit	Note
UI	Unit Interval	-	800	-	ps	800ps ± 100ppm
R_X1	Eye Mask	-	-	0.3	UI	
R_Y1	Eye Mask	100	-	-	mV	
R_Y2	Eye Mask	-	-	600	mV	
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	1200	mV	
R_{RX}	Differential Resistance	80	100	120	ohm	

Figure 20 SGMII Differential Receiver Eye Diagram



5.2.3 RGMII Timing Characteristics

Figure 21 RGMII Timing Characteristics

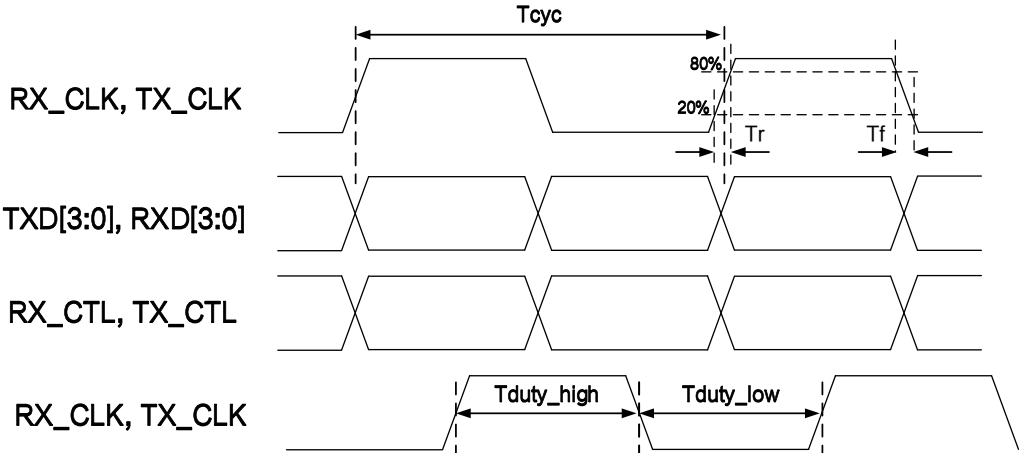


Table 20 RGMII Timing Characteristics in TX/RX Path

Symbol	Description	Min	Typ	Max	Unit
T_{cyc_G}	Clock cycle duration for 1000M	7.2	8.0	8.8	ns
T_{cyc_T}	Clock cycle duration for 100M	36	40	44	ns
Duty_G	Duty cycle for 1000M	45	50	55	%
Duty_T	Duty cycle for 100M	40	50	60	%
T_{duty_high}	Clock duty cycle high min time	3.6	-	-	ns
T_{duty_low}	Clock duty cycle low min time	3.6	-	-	ns
T_r	TXC/RXC Rise Time (20%~80%)	-	-	1	ns
T_f	TXC/RXC Fall Time (20%~80%)	-	-	1	ns
C_{loadR_max}	Max capacitive load of the signal at the receiver			5	pF

5.2.4 RGMII Timing Delay Modes

Figure 22 Signal Timing Parameters at Signal Source in DoD Mode

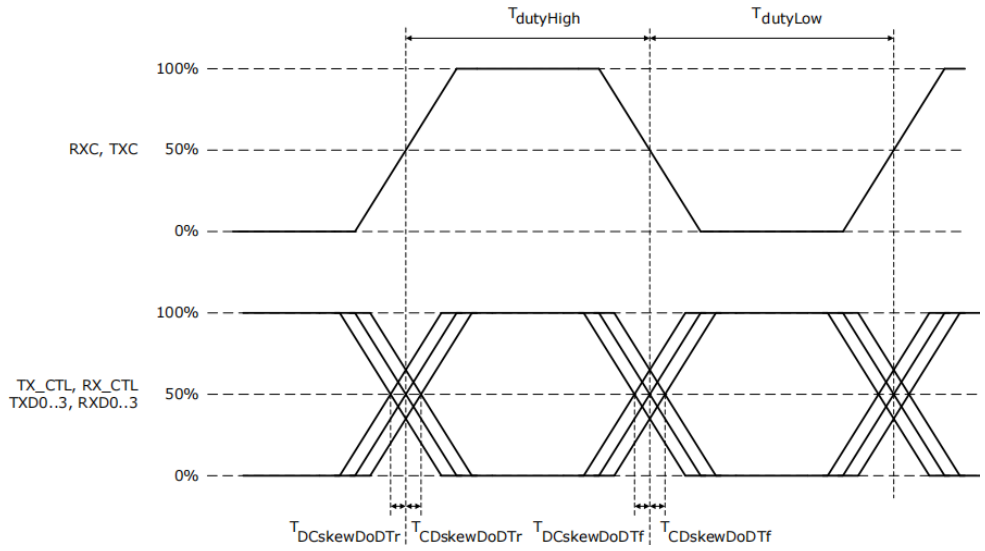


Figure 23 Signal Timing Parameters at Signal Destination in DoD Mode

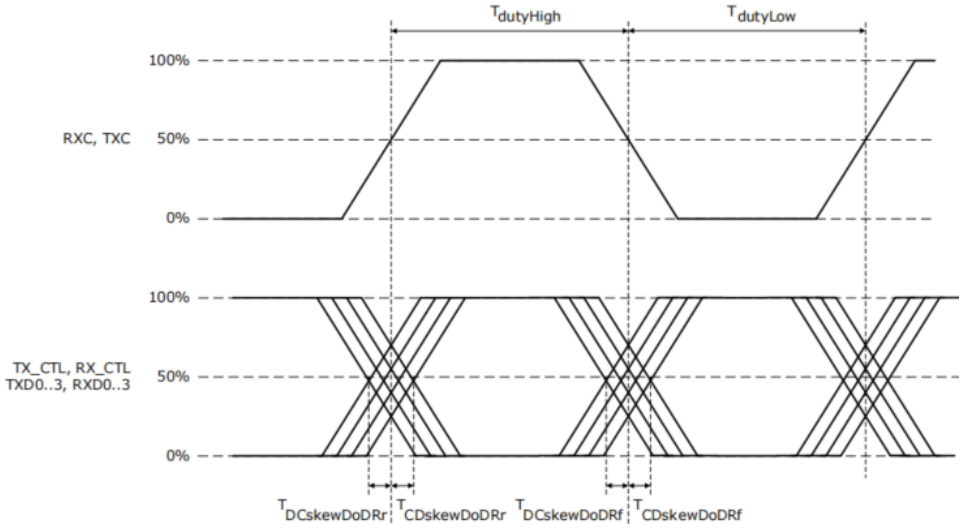


Table 21 Skews at Signal Source in DoD Mode

Symbol	Description	Min	Typ	Max	Unit
$T_{DCskewDoDTr}$	Data to Clock skew in Delay on Destination mode at signal Source rising edge.	-	-	0.5	ns
$T_{CDskewDoDTr}$	Clock to Data skew in Delay on Destination mode at signal Source rising edge.	-	-	0.5	ns
$T_{DCskewDoDTf}$	Data to Clock skew in Delay on Destination mode at signal Source falling edge.	-	-	0.5	ns
$T_{CDskewDoDTf}$	Clock to Data skew in Delay on Destination mode at signal Source falling edge.	-	-	0.5	ns

Table 22 Skews at Signal Destination in DoD Mode

Symbol	Description	Min	Typ	Max	Unit
$T_{DCskewDoDRr}$	Data to Clock skew in Delay on Destination mode at signal Destination rising edge.	-	-	0.65	ns
$T_{CDskewDoDRr}$	Clock to Data skew in Delay on Destination mode at signal Destination rising edge.	-	-	0.65	ns
$T_{DCskewDoDRf}$	Data to Clock skew in Delay on Destination mode at signal Destination falling edge.	-	-	0.65	ns
$T_{CDskewDoDRf}$	Clock to Data skew in Delay on Destination mode at signal Destination falling edge.	-	-	0.65	ns

Figure 24 Signal Timing Parameters at Signal Source in DoS Mode

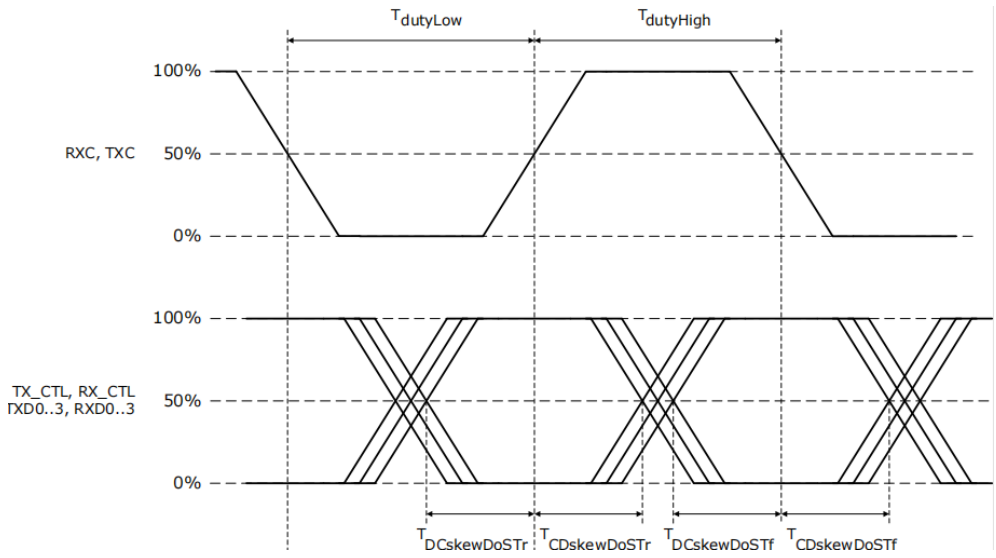


Figure 25 Signal Timing Parameters at Signal Destination in DoS Mode

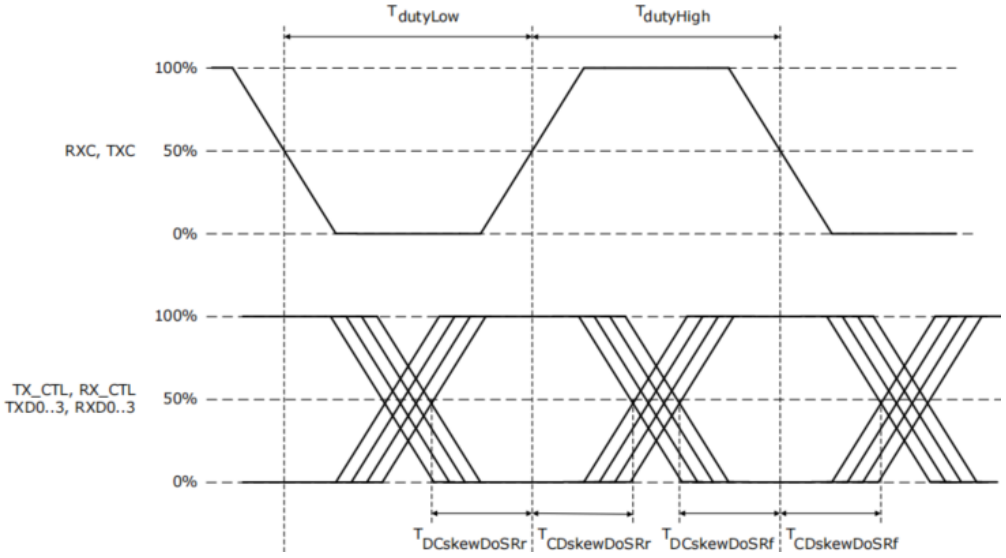


Table 23 Skews at Signal Source in DoS Mode

Symbol	Description	Min	Typ	Max	Unit
$T_{DCskewDoSTr}$	Data to Clock skew in Delay on Source mode at signal Source rising edge.	1.2	-	-	ns
$T_{CDskewDoSTr}$	Clock to Data skew in Delay on Source mode at signal Source rising edge.	1.2	-	-	ns
$T_{DCskewDoSTf}$	Data to Clock skew in Delay on Source mode at signal Source falling edge.	1.2	-	-	ns
$T_{CDskewDoSTf}$	Clock to Data skew in Delay on Source mode at signal Source falling edge.	1.2	-	-	ns

Table 24 Skews at Signal Destination in DoS Mode

Symbol	Description	Min	Typ	Max	Unit
$T_{DCskewDoSRr}$	Data to Clock skew in Delay on Source mode at signal Destination rising edge.	1.05	-	-	ns
$T_{CDskewDoSRr}$	Clock to Data skew in Delay on Source mode at signal Destination rising edge.	1.05	-	-	ns
$T_{DCskewDoSRf}$	Data to Clock skew in Delay on Source mode at signal Destination falling edge.	1.05	-	-	ns
$T_{CDskewDoSRf}$	Clock to Data skew in Delay on Source mode at signal Destination falling edge.	1.05	-	-	ns

Note: Delay could be adjusted by registers according to actual application. The rise/fall time condition is valid for test purposes for a load of 5pF at the signal source. The distributed output load of the transmitter has to be considered by PCB design.

5.2.5 SMI (MDC/MDIO) Interface Characteristics

Figure 26 SMI (MDC/MDIO) Timing

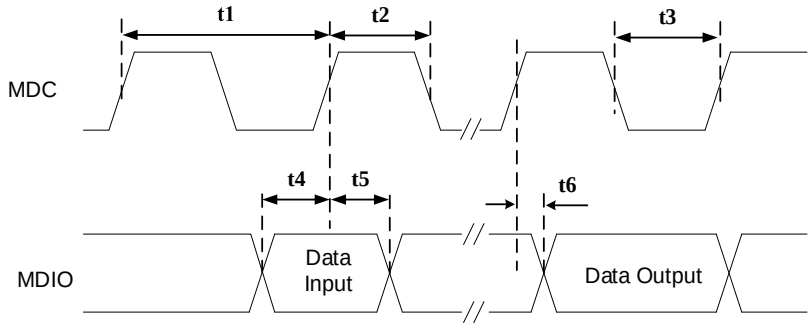


Table 25 MI (MDC/MDIO) Interface Characteristics

Symbol	Description	Min	Typ	Max	Unit
t1	MDC Clock Period	80	-	-	ns
t2	MDC High Time	32	-	-	ns
t3	MDC Low Time	32	-	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC rising edge (Data Output)	0	-	20	ns

5.3 Over Temperature Protection

Table 26 Over Temperature Protection

Symbol	Description	Min	Typ	Max	Unit
T_{otp_det}	Over temperature protection detection junction temperature	143	145	147	°C
T_{otp_rec}	Over temperature protection recovery junction temperature	133	135	137	°C
T_{otp_hys}	Over temperature protection hysteresis temperature	-	10	-	°C

Note: The over temperature protection is based on the ambient temperature, which may be related to the system's operating status. Accuracy can be adjusted by register configuration for different systems.

5.4 ESD

Table 27 ESD information

Feature Description	Value	Comment
HBM-ALL pins	±4KV for VDD33_AUX, ± 6KV for other pins	-
CDM-ALL pins	±750V	-

Feature Description	Value	Comment
Open Alliance Un-powered/Powered ESD	±8KV	● The test method is referred to Open Alliance EMC test. (IEEE 1000BASE-T1 EMC Test Specification for Transceivers ver.2.1). ● The test equipment set-up is referred to IEC61000-4-2.
Latch Up	Power: 1.5*VDD; I: 100mA	-

5.5 Crystal Requirement

Table 28 Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Frequency	Parallel Resonant Crystal Reference Frequency	-	25	-	MHz
Frequency Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-100	-	100	ppm
Frequency Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	100	ohm
Jitter	RMS Jitter	-	-	1	ps
DL	Drive Level	-	-	0.5	mW
V_{IH}	Crystal output high level	1.4	-	-	V
V_{IL}	Crystal output low level	-	-	0.4	V

5.6 Oscillator/External Clock Requirement

Table 29 Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency	-	25	-	MHz
Frequency Tolerance	-100	-	100	PPM
Duty Cycle	40	-	60	%
RMS Jitter	-	-	1	ps
V_{IH}	1.4	-	AVDD33+0.3	V
V_{IL}	-	-	0.4	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns
Operating Temperature Range	-40	-	125	°C

6 Power Requirements

6.1 Absolute Maximum Ratings

Table 30 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VBAT (YT8011A)	Supply voltage 12V	-0.3	30	V
VDD33_AUX (YT8011AN/AR)	Supply voltage 3.3V	-0.3	3.63	V
VDD_REG (YT8011A/AN)	Supply voltage 3.3V	-0.3	3.63	V
AVDDH	Supply voltage 3.3V	-0.3	3.63	V
DVDDL, AVDDL, SVDDL	Supply voltage 0.9V	-0.3	1.1	V
VDDIO (3.3/2.5/1.8V)	Voltage on digital output pins (3.3V IO)	-0.3	3.63	V
	Voltage on digital output pins (2.5V IO)	-0.3	2.8	V
	Voltage on digital output pins (1.8V IO)	-0.3	2.3	V
MDIP, MDIN	Voltage on MDIP, MDIN	-0.3	3.63	V
INH (YT8011A)	Voltage on INH	-0.3	VBAT+0.3	V
WAKE (YT8011A)	Voltage on WAKE	-0.3	VBAT+0.3	V
INH (YT8011AN/AR)	Voltage on INH	-0.3	VDD33_AUX+0.3	V
WAKE (YT8011AN/AR)	Voltage on WAKE	-0.3	VDD33_AUX+0.3	V
XTAL_IN, XTAL_OUT	Voltage on XTAL_IN, XTAL_OUT	-0.3	3.63	V
Other Pins	Voltage on other pins	-0.3	3.63	V
TSTG	Storage temperature	-55	150	℃

6.2 Recommended Operating Conditions

Table 31 Recommended Operating Conditions

Description	Pins	Min	Typ	Max	Unit
Supply Voltage 12V	VBAT(YT8011A)	3.135	12.0[Note1]	30	V
High power supply	AVDDH, VDD33_AUX, VDD_REG	3.135	3.30[Note2]	3.465	V
Low power supply	DVDDL, AVDDL, SVDDL	0.855	0.9[Note2]	0.945	V
Input IO Voltage	VDDIO = 1.8V	1.71	1.8	1.89	V
	VDDIO = 2.5V	2.375	2.5	2.625	V
	VDDIO = 3.3V	3.135	3.3	3.465	V
Ambient Operation Temperature, TAMB		-40	-	125	°C
Maximum Junction Temperature[Note3]		-	-	150	°C

Note1: YT8011A supports 12V power input on VBAT pin. YT8011AN/AR only supports 3.3V input on the VDD33_AUX pin.

Note2: The max ripple (peak to peak) of 3.3V should be under 50mV, and the ripple (peak to peak) of 0.9 should be under 30mV, except that the ripple (peak to peak) for DVDDIO should be under 100mV.

Note3: Actual Tj is calculated by thermal information and power consumption. Besides, the operating time should be taken into consideration.

6.3 Power Sequence

Figure 27 Power Sequence

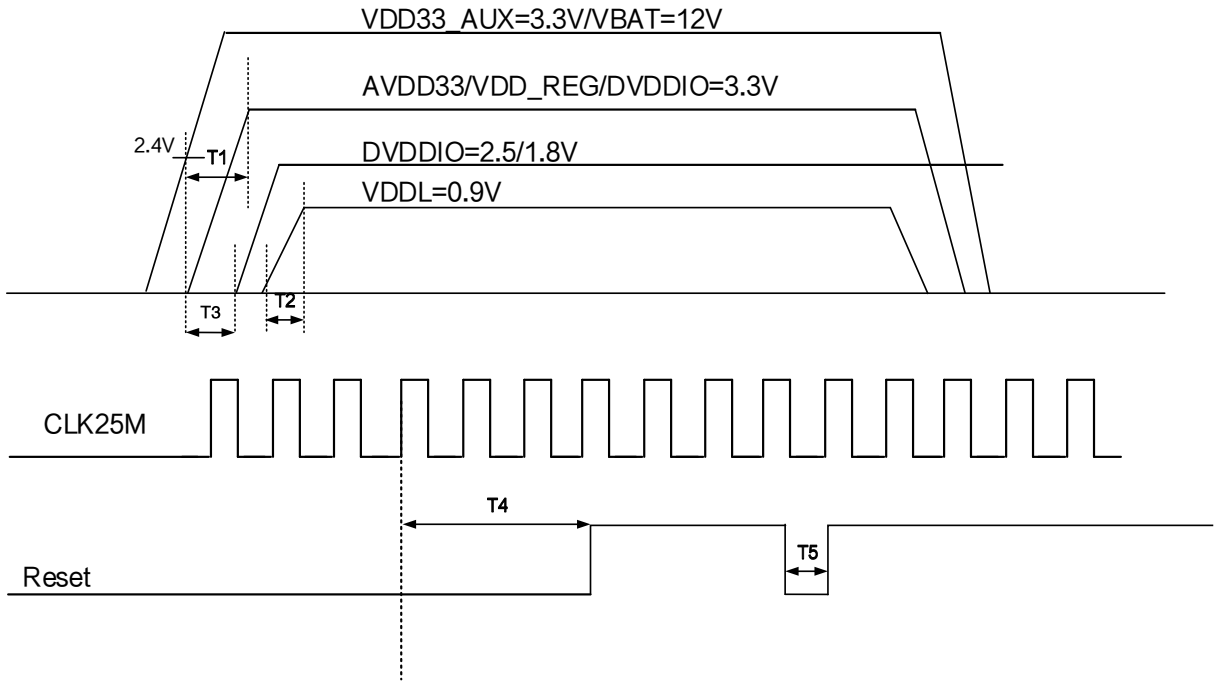


Table 32 Power Sequence

Symbol	Description	Min	Typ	Max	Unit
T1	AVDD33 power rising time.	0.1	-	30	ms
T2	External VDDL power rising time.	0.1	-	5	ms
T3	DVDDIO2.5/1.8 delay time after AVDD33	-	Note1	-	ms
T4	PHY Reset delay time after CLK Stable	10	-	-	ms
T5	PHY Reset active time	160	-	-	us

Note1: For reliable power on strapping, DVDDIO2.5/1.8 needs to be given in the T3 interval. That is external power shall be rose after AVDD33 rose and before VDDL rose. No certain value of T3 is defined.

Note2: VDD33_Aux/VBAT must be supplied first in all situations, AVDD33 should start to ramp up after VDD33_Aux reaches at least 2.4V. When using VDD33_Aux, and the same power source as AVDD33, VDD33_Aux can be supplied at the same time as AVDD33, but not later than AVDD33. If use a separate 3.3V power source, the AVDD33 should ramp up after VDD33_Aux reaches at least 2.4V.

Note3: The order for Powering-off is VDDL>AVDD33/VDD_REG>VBAT/VDD33_AUX. During Power on and off, the voltage of the power domain 3.3V shall exceed the power domain 0.9V. VDD_AUX/VBAT should exceed the power domain 3.3V and 0.9V. There is no restriction on the power-off sequence of DVDD.

6.4 Power Consumption

Table 33 YT8011AN RGMII Power Consumption-Without Internal SWR

Condition	AVDDH (mA)	VDD33_AUX (μA)	VDDIO (mA)	VDDL (mA)	Power (mW)
Traffic@1000Mbps	80.9	113	36.4	169.6	539.7
Traffic@100Mbps	59.7	113	9.4	37.6	262.2
Standby Mode	33.9	113	5.5	19.4	147.5
Reset Mode	8.3	102	3.5	15.8	53.2
Sleep Mode	0	8	0	0	0.03

Table 34 YT8011AN SGMII Power Consumption-Without Internal SWR

Condition	AVDDH (mA)	VDD33_AUX (μA)	VDDIO (mA)	VDDL (mA)	Power (mW)
Traffic@1000Mbps	80.5	113	2.1	191.7	445.1
Traffic@100Mbps	59.8	113	2.1	61.7	260.2
Standby Mode	33.7	113	3.2	45	162.3
Reset Mode	8.3	102	3.6	15.7	53.4
Sleep Mode	0	8	0	0	0.03

Note: Test by TT IC at room temperature. AVDDH/VDD33_AUX/VDDIO = 3.3V, AVDDL/DVDDL/SVDDL = 0.9V(external power supply).

The power consumption of YT8011AR can refer to the YT8011AN RGMII Mode.

6.5 Maximum Power Consumption

Table 35 YT8011AN RGMII Max Power Consumption-Without Internal SWR

Condition	AVDDH (mA)	VDD33_AUX (μA)	VDDIO (mA)	VDDL (mA)	Power (mW)
Traffic@1000Mbps	93	150	44	570	965.6

Table 36 YT8011AN SGMII Max Power Consumption-Without Internal SWR

Condition	AVDDH (mA)	VDD33_AUX (μA)	VDDIO (mA)	VDDL (mA)	Power (mW)
Traffic@1000Mbps	93	150	4	610	869.6

Note: Maximum power consumption is tested by corner FF IC at 125°C. VDD33_AUX max current is related to the external power circuit, maximum current may reach more than 2mA. AVDDH/VDD33_AUX/VDDIO=3.3V, AVDDL/DVDDL/SVDDL=0.9V (external power supply).

Power consumption test by TT IC at 125°C, +5% voltage: RGMII Mode=763.7mW, SGMII Mode=681.4mW.

7 Package Information

7.1 RoHS-Compliant Packaging

Motorcomm offers a RoHS package that is compliant with RoHS.

Table 37 RoHS-Compliant Packaging

Part Number	Status	Package	Operation Temp (°C)	Note
YT8011A	Active	QFN 48 7x7mm	-40 to 125	
YT8011AN	Active	QFN 48 7x7mm	-40 to 125	
YT8011AR	Active	QFN 40 6x6mm	-40 to 125	

7.2 Thermal Resistance

Table 38 Thermal Resistance (QFN48)

Symbol	Parameter	Condition	Typ	Unit
θ_{JA}	Thermal resistance - junction to ambient $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no airflow T_A=25°C	28.02	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with no airflow T_A=125°C	24.28	°C/W
θ_{JC}	Thermal resistance - junction to case $\theta_{JC} = (T_J - T_C)/ Ptop$ Ptop = Power dissipation from the top of the package	JEDEC with no airflow	11.54	°C/W
θ_{JB}	Thermal resistance - junction to board $\theta_{JB} = (T_J - T_B)/ Pbottom$ Pbottom = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no airflow	9.32	°C/W

8 Mechanical and Thermal

8.1 Mechanical Information

8.1.1 YT8011A/AN Mechanical Information

Figure 28 YT8011A/AN Mechanical Dimensions

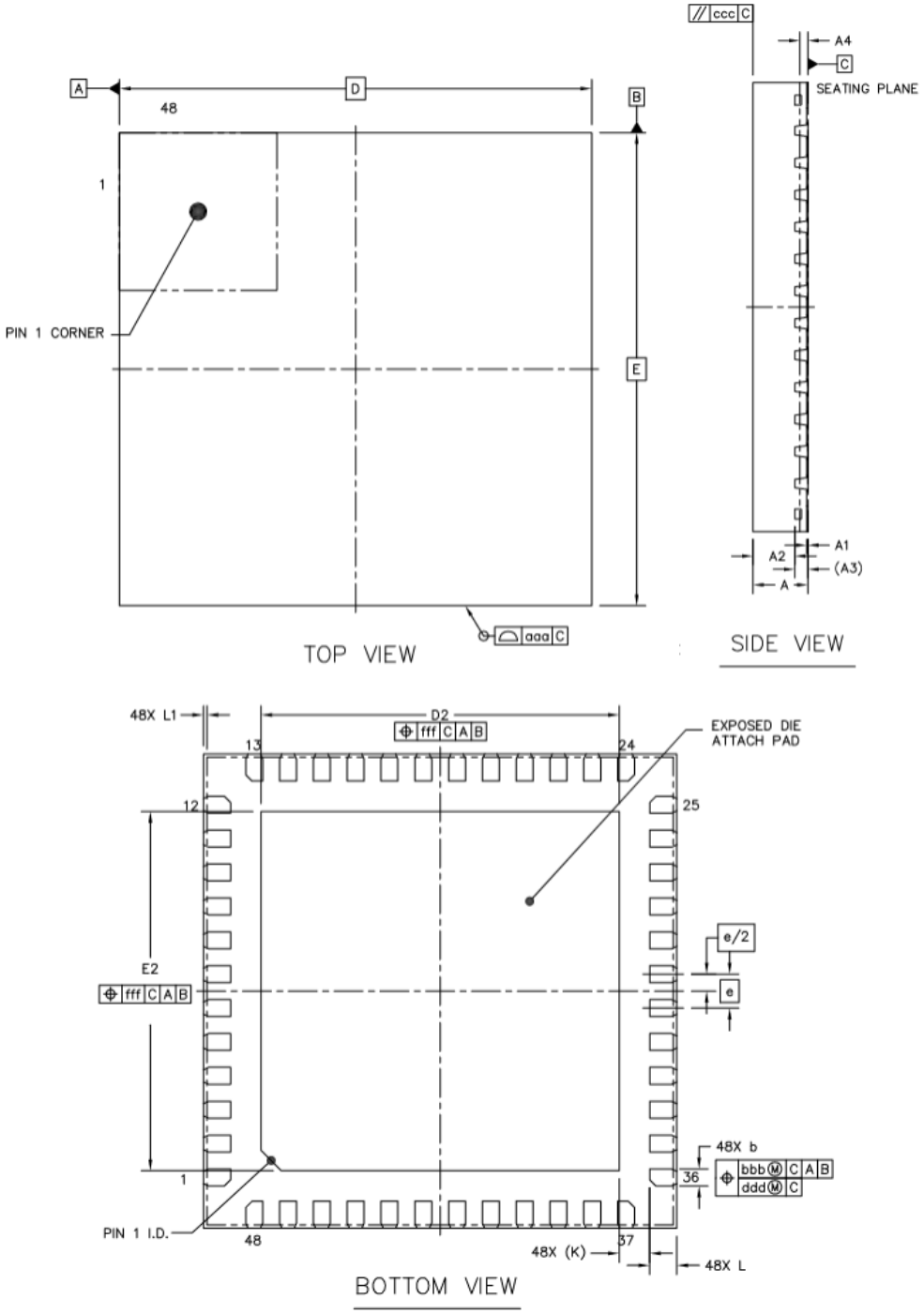
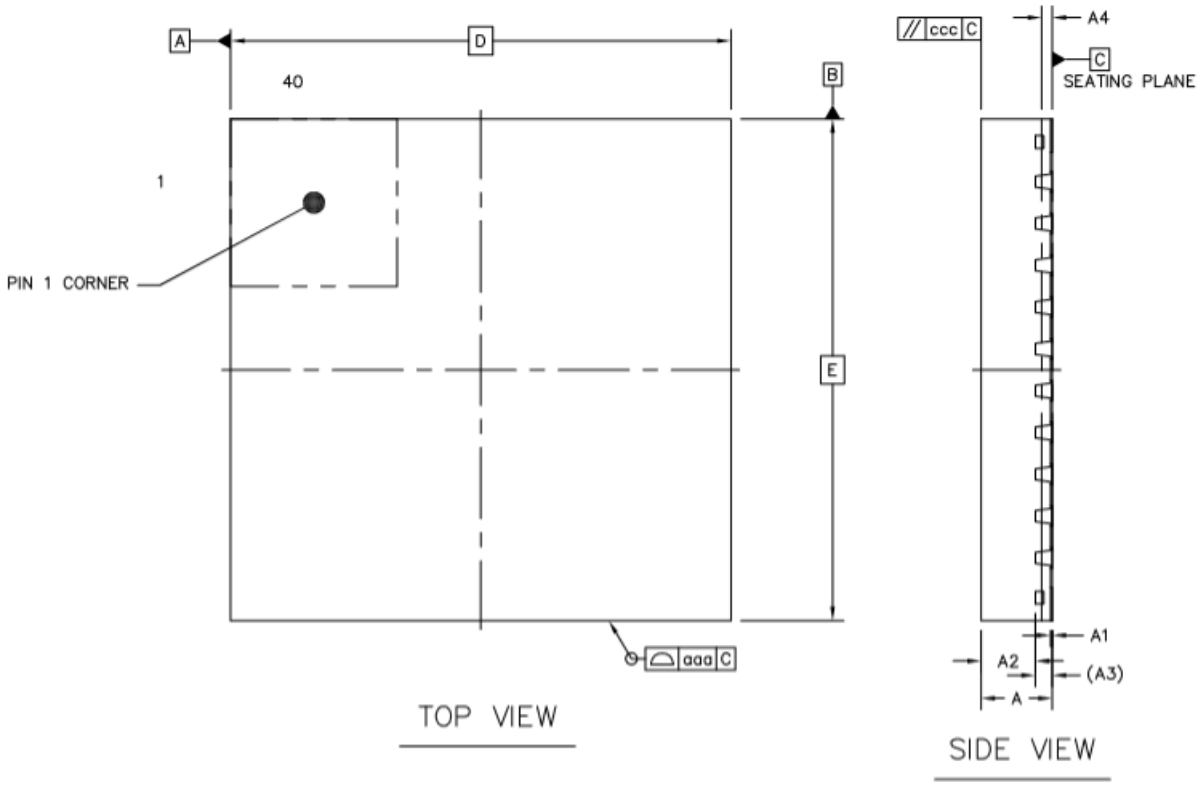


Table 39 YT8011A/AN Mechanical Dimensions in mm

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	5.2	5.3	5.4
	Y	E2	5.2	5.3	5.4
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.45 REF	

8.1.2 YT8011AR Mechanical Information

Figure 29 YT8011AR Mechanical Dimensions



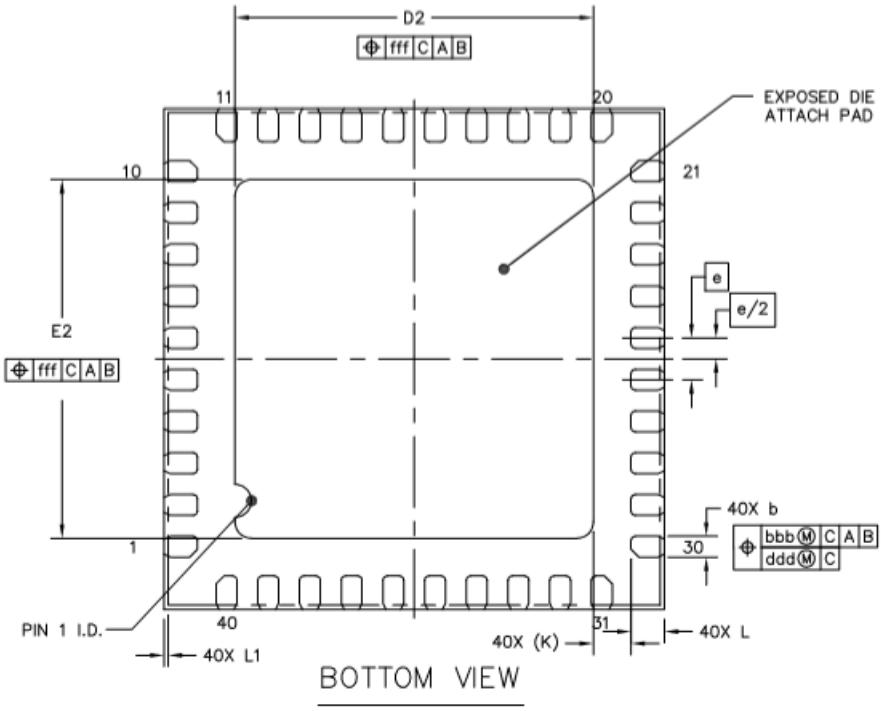


Table 40 YT8011AR Mechanical Dimensions in mm

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
SIDE WETTABLE DEPTH		A4	0.075	---	0.18
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	4.2	4.3	4.4
	Y	E2	4.2	4.3	4.4
LEAD LENGTH		L	0.3	0.4	0.5
SIDE WETTABLE WIDTH		L1	0.01	---	0.09
LEAD TIP TO EXPOSED PAD EDGE		K		0.45 REF	

9 Ordering Information

Motorcomm offers an RoHS package that is compliant with RoHS.

Part Number	Grade	Package	Pack	Status	Operation Temp
YT8011A	Automotive application AECQ-100 Grade 1	QFN-48 E-PAD	2500EA	MP	-40°C ~ 125°C
YT8011AN	Automotive application AECQ-100 Grade 1	QFN-48 E-PAD	2500EA	MP	-40°C ~ 125°C
YT8011AR	Automotive application AECQ-100 Grade 1	QFN-40 E-PAD	3000EA	MP	-40°C ~ 125°C
MSL (Moisture Sensitivity Level)				Level 3	