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Motorcomm

Motorcomm
YT9218MB Datasheet

LAYER 2 MANAGED 8+2 PORT 10/100/1000 SWITCH CONTROLLER

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General Description

YT9218MB is a LQFP176 E-PAD, high-performance 8+2-port Gigabit Ethernet switch. It integrates eight PHY ports support 1000Base-T/100Base-TX/10Base-Te,two extra MAC ports for specific applications which supports 2500BX/SGMII/1000Base-X/100Base-FX/RGMII/MII/RMII. YT9218MB is also embedded with a RISC-V microprocessor.

The integrated Giga-PHY complies with 10Base-Te, 100Base-TX, and 1000Base-T IEEE standard 802.3 and also support Motorcomm proprietary LRE100-4 feature, which makes the device can auto-negotiate and link up with LRE100-4 compliant link partners, in extended cable length applications up to 400 meters at 100Mbps over CAT5E cable.

The Extension GMAC1 and Extension GMAC2 of the YT9218MB supports xMII or SerDes connecting with an external PHY, MAC, external CPU or RISC in specific applications. The xMII refer to Reduced Gigabit Media Independent Interface (RGMII), Media Independent Interface (MII), and Reduced Media Independent Interface (RMII). The SerDes supports IEEE 100Base-FX, IEEE 1000Base-X and IEEE 2500Base-X.

YT9218MB integrates a 4K look-up table with an efficient hashing algorithm for address searching and learning, each entry also can be configured as a static entry.

YT9218MB supports IEEE 802.1Q VLAN and has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol -based, VLAN translation, Flow-based capability，and MAC-based, IP-subnet-based VLAN can be supported by configuration It also supports IVL, SVL, and IVL/SVL for flexible network topology architecture.

The YT9218MB supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources. The YT9218MB supports storm control.

In order to support flexible traffic classification, the YT9218MB supports 383-hardware entry ACL rules check and multiple actions options. The 383 entries are composed of 48 rows, each row has 8 entries. To support long rule, rule extension is supported by any combinations of the 8 entries for each row. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. The ACL action can be configured as Drop/Permit/Redirect/ Mirror, change priority/DSCP value in 802.1q, and rate policing when an ACL rule matches.

Key Features

- High performance, nonblocking, 10 ports Ethernet Switch integrating:
  - Eight 1000Base-T/100Base-TX/10Base-Te PHY
  - Two SerDes interfaces for 2500Base-X/SGMII/1000Base-X/100Base-FX
  - Two RGMII/MII/RMII interfaces
- PHY Transceiver
  - Each PHY supports 10/100/1000M full duplex mode (half duplex only supports in 10/100M mode)
  - Full duplex operation with IEEE 802.3x flow control and half duplex operation with backpressure
  - Each PHY supports Advanced Cable Status Diagnostic (CSD)
  - Each PHY supports Motorcomm proprietary LRE100-4 feature
- Advanced Features
  - Supports parallel LED or serial LED outputs
  - Supports SPI/SMI/I2C Slave interface for external CPU
  - Supports SMI/I2C Master interface
  - Supports 1 interrupt output to external CPU for notification
  - Supports 64K-byte EEPROM space for configuration
  - Link On Cable Length Power Saving
  - Link Down Power Saving
  - Supports 9K byte jumbo frames
- Supports 2 IEEE 802.3ad Link aggregation groups
- Security Filtering
  - Supports Disable learning for each port
  - Supports Disable learning-table aging for each port
  - Supports Unknown DA filter mask
  - Supports Port Isolation
  - Supports Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
  - Supports DOS attack prevent

- Control, Management and Statistics
  - Supports RFC MIB Counters
    - MIB-II (RFC 1213)
    - Ethernet-Like MIB (RFC 3635)
    - Interface Group MIB (RFC 2863)
    - RMON (RFC 2819)
    - Bridge MIB (RFC 1493)
    - Bridge MIB Extension (RFC 2674)
  - Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol)
  - Supports Loop Detection
- Packet Process Engine
  - Supports 4k 802.1Q VLANs
  - Supports VLAN policing and VLAN forwarding decision
  - Supports Port based, Tag based, and Protocol based VLAN
  - Supports per port egress VLAN tagging and untagging
  - Supports IEEE 802.1D/s/w Spanning Tree Protocols
  - Supports Multicast VLAN (MVR)
  - Supports IVL, SVL, and IVL/SVL
  - Supports IEEE 802.1ad Stacking VLAN
  - Supports VLAN translation (1:1/2:1/2:2/ N:1/1:N)
  - Supports IEEE 802.1x Access Control Protocol
    - Port-Based Access Control
    - MAC-Based Access Control
    - Guest VLAN
  - Supports ACL Rules
  - Supports Hardware/Software IGMP/ MLD Snooping
    - Supports Fast Leave
    - Supports IGMP v1/v2
    - Static/Dynamic Router port

- Mirror
  - Port based mirror
  - Flow based mirror
- Supports reserved multicast control
- Supports WOL

- Quality of Service (QoS)
  - Supports Queue based DWRR/SP, packet/byte modes are both supported for DWRR
  - Supports min-max queue based shaping, packet/byte modes are both supported
  - Supports single token bucket for port based shaping, packet/byte modes are both supported
  - Supports per port Input Bandwidth Control, packet/byte modes are both supported
  - trTCM color aware/blind packet/byte modes
  - Traffic classification based on multiple source types
  - Supports 8 unicast queues and 4 multicast queues for each port
  - Tail drop is supported for UQ/MQ, WRED is supported for UQ
- Microprocessor
  - Integrated RISC-V microprocessor
  - Supports Flash Interface (Dual mode/Single mode)
  - Supports code execution (XIP) directly from SPI Flash
- 25MHz crystal or 3.3V OSC input
- LQFP 176-pin E-PAD package

Block Diagram

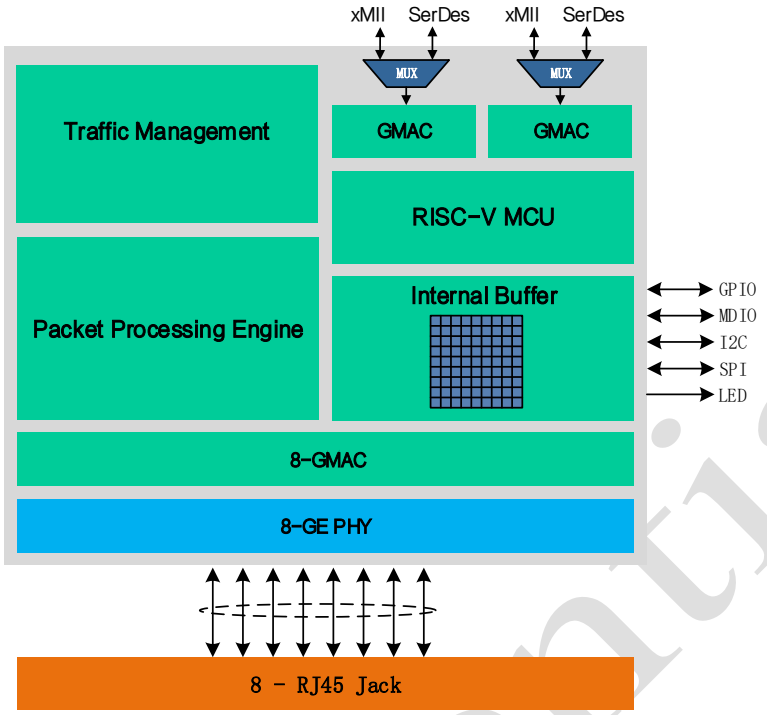

Figure 1. Block Diagram

System Applications

- 8-Port 1000Base-T+2-Port 2500Base-X Switch
- 8-Port 1000Base-T+1-Port RGMII + 1-Port 2500Base-X Switch
- 8-Port 1000Base-T+2-Port 1000Base-X/100Base-FX Switch
- 8-Port 1000Base-T Router with Dual MII/RGMII
- 8-Port 1000Base-T Router with Dual SGMII
- 8-Port 1000Base-T NVR
- 8-Port 1000Base-T ONU

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Revision History

Revision	Release Date	Summary
V1.00	2024/5/21	First version.

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1.1. Pin Assignment

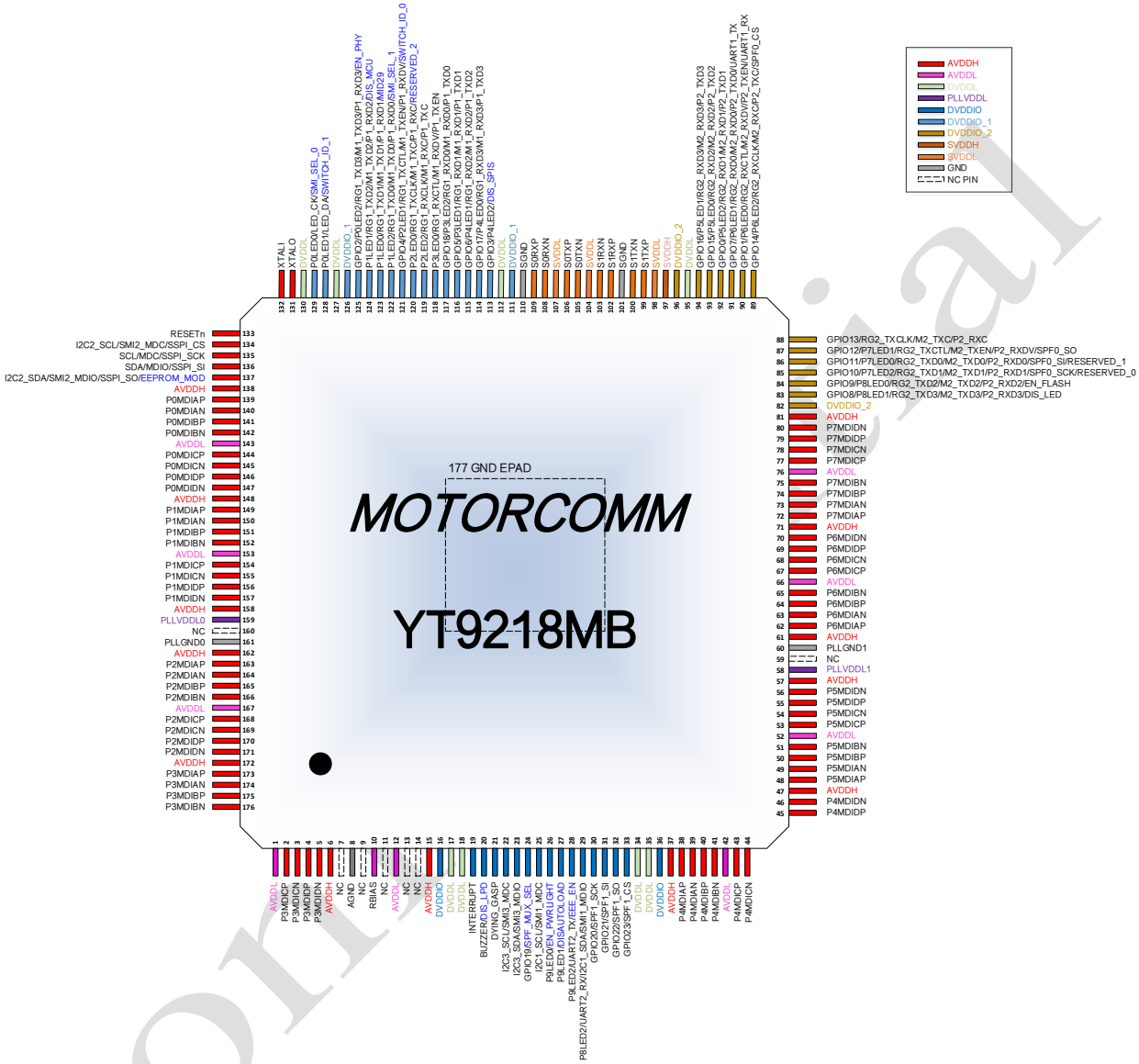

Figure 2. Pin Assignment

1.2. Pin Assignment Table

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Digital Power Pin
- G: Digital Ground pin
- PU: Internal pull up
- LI: Latched Input During Power UP
- OD: Open Drain
- AI: Analog Input
- AO: Analog Output
- AIO: Analog Bidirectional Input and Output
- AP: Analog Power pin
- AG: Analog Ground pin
- PD: Internal pull down
- XT: Crystal Related

Table 1. Pin Assignment

No.	Pin Name	Type
1	AVDDL	AP
2	P3MDICP	AIO
3	P3MDICN	AIO
4	P3MDIDP	AIO
5	P3MDIDN	AIO
6	AVDDH	AP
7	NC	–
8	AGND	AG
9	NC	–
10	RBIAS	AO
11	NC	–
12	AVDDL	AP
13	NC	–
14	NC	–
15	AVDDH	AP
16	DVDDIO	P
17	DVDDL	P
18	DVDDL	P
19	INTERRUPT	O/PU
20	BUZZER/DIS_LPD	IO/LI/PU

No.	Pin Name	Type
21	DYING_GASP	AI
22	I2C3_SCL/SMI3_MDC	IO/OD/PU
23	I2C3_SDA/SMI3_MDIO	IO/OD/PU
24	GPIO19/SPF_MUX_SEL	IO/LI/PU
25	I2C1_SCL/SMI1_MDC	IO/OD/PU
26	P9LED0/EN_PWRLIGHT	IO/LI/PU
27	P9LED1/DISAUTOLOAD	IO/LI/PU
28	P9LED2/UART2_TX/EEE_EN	IO/LI/PU
29	P8LED2/UART2_RX/I2C1_SDA/SMI1_MDIO	IO/OD/PU
30	GPIO20/SPF1_SCK	IO/PU
31	GPIO21/SPF1_SI	IO/PU
32	GPIO22/SPF1_SO	IO/PU
33	GPIO23/SPF1_CS	IO/PU
34	DVDDL	P

No.	Pin Name	Type
35	DVDDL	P
36	DVDDIO	P
37	AVDDH	AP
38	P4MDIAP	AIO
39	P4MDIAN	AIO
40	P4MDIBP	AIO
41	P4MDIBN	AIO
42	AVDDL	AP
43	P4MDICP	AIO
44	P4MDICN	AIO
45	P4MDIDP	AIO
46	P4MDIDN	AIO
47	AVDDH	AP
48	P5MDIAP	AIO
49	P5MDIAN	AIO
50	P5MDIBP	AIO
51	P5MDIBN	AIO
52	AVDDL	AP
53	P5MDICP	AIO
54	P5MDICN	AIO
55	P5MDIDP	AIO
56	P5MDIDN	AIO
57	AVDDH	AP
58	PLLVDDL1	AP
59	NC	–
60	PLLGND1	AG
61	AVDDH	AP
62	P6MDIAP	AIO
63	P6MDIAN	AIO
64	P6MDIBP	AIO
65	P6MDIBN	AIO
66	AVDDL	AP
67	P6MDICP	AIO
68	P6MDICN	AIO
69	P6MDIDP	AIO

No.	Pin Name	Type
70	P6MDIDN	AIO
71	AVDDH	AP
72	P7MDIAP	AIO
73	P7MDIAN	AIO
74	P7MDIBP	AIO
75	P7MDIBN	AIO
76	AVDDL	AP
77	P7MDICP	AIO
78	P7MDICN	AIO
79	P7MDIDP	AIO
80	P7MDIDN	AIO
81	AVDDH	AP
82	DVDDIO_2	P
83	GPIO8/P8LED1/RG2_TXD3/M2_TXD3/P2_RXD3/DIS_LED	IO/LI/PU
84	GPIO9/P8LED0/RG2_TXD2/M2_TXD2/P2_RXD2/EN_FLASH	IO/LI/PU
85	GPIO10/P7LED2/RG2_TXD1/M2_TXD1/P2_RXD1/SPF0_SCK/RESERVED_0	IO/LI/PU
86	GPIO11/P7LED0/RG2_TXD0/M2_TXD0/P2_RXD0/SPF0_SI/RESERVED_1	IO/LI/PU
87	GPIO12/P7LED1/RG2_TXCTL/M2_TXEN/P2_RXDV/SPF0_SO	IO/PU
88	GPIO13/RG2_TXCLK/M2_TXC/P2_RXC	IO/PD
89	GPIO14/P6LED2/RG2_RXCLK/M2_RXC/P2_TXC/SPF0_CS	IO/PU
90	GPIO1/P6LED0/RG2_RXCTL/M2_RXDV/P2_TXEN/UART1_RX	IO/PU
91	GPIO7/P6LED1/RG2_RXD0/M2_RXD0/P2_TXD0/UART1_TX	IO/PU
92	GPIO0/P5LED2/RG2_RXD1/M2_RXD1/P2_TXD1	IO/PU
93	GPIO15/P5LED0/RG2_RXD2/M2_RXD2/P2_TXD2	IO/PU

No.	Pin Name	Type
94	GPIO16/P5LED1/RG2_RXD3/M2_RXD3/P2_TXD3	IO/PU
95	DVDDL	P
96	DVDDIO_2	P
97	SVDDH	AP
98	SVDDL	AP
99	S1TXP	AO
100	S1TXN	AO
101	SGND	AG
102	S1RXP	AI
103	S1RXN	AI
104	SVDDL	AP
105	S0TXN	AO
106	S0TXP	AO
107	SVDDL	AP
108	S0RXN	AI
109	S0RXP	AI
110	SGND	AG
111	DVDDIO_1	P
112	DVDDL	P
113	GPIO3/P4LED2/DIS_SPIS	IO/LI/PU
114	GPIO17/P4LED0/RG1_RXD3/M1_RXD3/P1_TXD3	IO/PU
115	GPIO6/P4LED1/RG1_RXD2/M1_RXD2/P1_TXD2	IO/PU
116	GPIO5/P3LED1/RG1_RXD1/M1_RXD1/P1_TXD1	IO/PU
117	GPIO18/P3LED2/RG1_RXD0/M1_RXD0/P1_TXD0	IO/PU
118	P3LED0/RG1_RXCTL/M1_RXDV/P1_TXEN	IO/PU
119	P2LED2/RG1_RXCLK/M1_RXC/P1_TXC	IO/PU
120	P2LED0/RG1_TXCLK/M1_TXC/P1_RXC/RESERVED_2	IO/LI/PU
121	GPIO4/P2LED1/RG1_TXCTL/M1_TXEN/P1_RXDV/SWITCH_ID_0	IO/LI/PU

No.	Pin Name	Type
122	P1LED2/RG1_TXD0/M1_TXD0/P1_RXD0/SMI_SEL_1	IO/LI/PU
123	P1LED0/RG1_TXD1/M1_TXD1/P1_RXD1/MID29	IO/LI/PU
124	P1LED1/RG1_TXD2/M1_TXD2/P1_RXD2/DIS_MCU	IO/LI/PU
125	GPIO2/P0LED2/RG1_TXD3/M1_TXD3/P1_RXD3/EN_PHY	IO/LI/PU
126	DVDDIO_1	P
127	DVDDL	P
128	P0LED1/LED_DA/SWITCH_ID_1	IO/LI/PU
129	P0LED0/LED_CK/SMI_SEL_0	IO/LI/PU
130	DVDDL	P
131	XTALO	XT
132	XTALI	XT
133	RESETn	AI
134	I2C2_SCL/SMI2_MDC/SSPI_CS	IO/OD/PU
135	SCL/MDC/SSPI_SCK	IO/OD/PU
136	SDA/MDIO/SSPI_SI	IO/OD/PU
137	I2C2_SDA/SMI2_MDIO/SSPI_SO/EEPROM_MOD	IO/OD/LI/PU
138	AVDDH	AP
139	P0MDIAP	AIO
140	P0MDIAN	AIO
141	P0MDIBP	AIO
142	P0MDIBN	AIO
143	AVDDL	AP
144	P0MDICP	AIO
145	P0MDICN	AIO
146	P0MDIDP	AIO
147	P0MDIDN	AIO
148	AVDDH	AP
149	P1MDIAP	AIO
150	P1MDIAN	AIO

No.	Pin Name	Type
151	P1MDIBP	AIO
152	P1MDIBN	AIO
153	AVDDL	AP
154	P1MDICP	AIO
155	P1MDICN	AIO
156	P1MDIDP	AIO
157	P1MDIDN	AIO
158	AVDDH	AP
159	PLLVDDL0	AP
160	NC	–
161	PLLGND0	AG
162	AVDDH	AP
163	P2MDIAP	AIO
164	P2MDIAN	AIO

No.	Pin Name	Type
165	P2MDIBP	AIO
166	P2MDIBN	AIO
167	AVDDL	AP
168	P2MDICP	AIO
169	P2MDICN	AIO
170	P2MDIDP	AIO
171	P2MDIDN	AIO
172	AVDDH	AP
173	P3MDIAP	AIO
174	P3MDIAN	AIO
175	P3MDIBP	AIO
176	P3MDIBN	AIO
177	GND EPAD	G

2. Pin Description

2.1. MDI Interface Pins

Table 2. Transceiver Interface

No.	Pin Name	Type	Description
139	P0MDIAP	AIO	Port 0 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
140	P0MDIAN	AIO	
141	P0MDIBP	AIO	Port 0 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
142	P0MDIBN	AIO	
144	P0MDICP	AIO	Port 0 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
145	P0MDICN	AIO	
146	P0MDIDP	AIO	Port 0 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
147	P0MDIDN	AIO	
149	P1MDIAP	AIO	Port 1 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
150	P1MDIAN	AIO	
151	P1MDIBP	AIO	Port 1 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
152	P1MDIBN	AIO	
154	P1MDICP	AIO	Port 1 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
155	P1MDICN	AIO	
156	P1MDIDP	AIO	Port 1 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
157	P1MDIDN	AIO	
163	P2MDIAP	AIO	Port 2 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
164	P2MDIAN	AIO	
165	P2MDIBP	AIO	Port 2 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
166	P2MDIBN	AIO	
168	P2MDICP	AIO	Port 2 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
169	P2MDICN	AIO	
170	P2MDIDP	AIO	Port 2 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
171	P2MDIDN	AIO	
173	P3MDIAP	AIO	Port 3 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
174	P3MDIAN	AIO	
175	P3MDIBP	AIO	Port 3 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
176	P3MDIBN	AIO	
2	P3MDICP	AIO	Port 3 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
3	P3MDICN	AIO	
4	P3MDIDP	AIO	Port 3 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
5	P3MDIDN	AIO	

38	P4MDIAP	AIO	Port 4 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
39	P4MDIAN	AIO	
40	P4MDIBP	AIO	Port 4 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
41	P4MDIBN	AIO	
43	P4MDICP	AIO	Port 4 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
44	P4MDICN	AIO	
45	P4MDIDP	AIO	Port 4 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
46	P4MDIDN	AIO	
48	P5MDIAP	AIO	Port 5 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
49	P5MDIAN	AIO	
50	P5MDIBP	AIO	Port 5 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
51	P5MDIBN	AIO	
53	P5MDICP	AIO	Port 5 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
54	P5MDICN	AIO	
55	P5MDIDP	AIO	Port 5 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
56	P5MDIDN	AIO	
62	P6MDIAP	AIO	Port 6 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
63	P6MDIAN	AIO	
64	P6MDIBP	AIO	Port 6 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
65	P6MDIBN	AIO	
67	P6MDICP	AIO	Port 6 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
68	P6MDICN	AIO	
69	P6MDIDP	AIO	Port 6 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
70	P6MDIDN	AIO	
72	P7MDIAP	AIO	Port 7 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
73	P7MDIAN	AIO	
74	P7MDIBP	AIO	Port 7 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
75	P7MDIBN	AIO	
77	P7MDICP	AIO	Port 7 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
78	P7MDICN	AIO	
79	P7MDIDP	AIO	Port 7 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
80	P7MDIDN	AIO	

2.2. RGMII Interface Pins

Table 3. RGMII 1 Interface Pins

No.	Pin Name	Type	Description
120	RG1_TXCLK	O/PU	RGMII 1 transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100Mbps operation, the clocks will operate at 2.5MHz or 25MHz respectively. TXCLK is an output pin in RGMII mode.
121	RG1_TXCTL	O/PU	RGMII 1 Transmit Control Signal from the MAC. TXCTL is an output pin in RGMII mode.
125	RG1_TXD3	O/PU	RGMII 1 transmit Data. Data is transmitted from MAC to PHY via TXD[3:0] . TXD[3:0] are output pins in RGMII mode.
124	RG1_TXD2	O/PU	
123	RG1_TXD1	O/PU	
122	RG1_TXD0	O/PU	
119	RG1_RXCLK	I/PU	RGMII 1 continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. RXCLK is an input pin in RGMII mode.
118	RG1_RXCTL	I/PU	RGMII 1 receive Control Signal to the MAC. RXCTL is an input pin in RGMII mode.
114	RG1_RXD3	I/PU	RGMII 1 receive Data. Data is transmitted from PHY to MAC via RXD[3:0]. RXD[3:0] are input pins in RGMII mode.
115	RG1_RXD2	I/PU	
116	RG1_RXD1	I/PU	
117	RG1_RXD0	I/PU	

Table 4. RGMII 2 Interface Pins

No.	Pin Name	Type	Description
88	RG2_TXCLK	O/LI/PD	RGMII 2 transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed. For Gigabit operation, the clocks will operate at 125MHz, and for 10/100Mbps operation, the clocks will operate at 2.5MHz or 25MHz respectively. TXCLK is an output pin in RGMII mode.
87	RG2_TXCTL	O/PU	RGMII 2 Transmit Control Signal from the MAC. TXCTL is an output pin in RGMII mode.
83	RG2_TXD3	O/LI/PU	RGMII 2 transmit Data. Data is transmitted from MAC to PHY via TXD[3:0]. TXD[3:0] are output pins in RGMII mode.
84	RG2_TXD2	O/PU	
85	RG2_TXD1	O/PU	

86	RG2_TXD0	O/LI/PU	
89	RG2_RXCLK	I/PU	RGMII 2 continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. RXCLK is an input pin in RGMII mode.
90	RG2_RXCTL	I/PU	RGMII 2 receive Control Signal to the MAC. RXCTL is an input pin in RGMII mode.
94	RG2_RXD3	I/PU	RGMII 2 receive Data. Data is transmitted from PHY to MAC via RXD[3:0]. RXD[3:0] are input pins in RGMII mode.
93	RG2_RXD2	I/PU	
92	RG2_RXD1	I/PU	
91	RG2_RXD0	I/PU	

2.3. MII Interface Pins

Table 5. MII1 Interface Pins

No.	Pin Name	Type	Description
120	M1_TXCLK/ P1_RXCLK	IO/PU	1. M_TXCLK Pin in MII1 MAC Mode. MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. 2. P_RXCLK Pin in MII1 PHY Mode. MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te. M_TXCLK is an input pin in MII MAC mode. P_RXCLK is an output pin in MII PHY mode.
121	M1_TXEN/ P1_RXDV	O/PU	1. M_TXEN Pin in MII1 MAC Mode. MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXCLK. 2. P_RXDV Pin in MII1 PHY Mode. MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXCLK. M_TXEN/P_RXDV is an output pin in both MII MAC mode and MII PHY mode.
125	M1_TXD3/ P1_RXD3	O/PU	1. M_TXD[3:0] Pin in MII1 MAC Mode. MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXCLK. 2. P_RXD[3:0] Pin in MII1 PHY Mode.
124	M1_TXD2/ P1_RXD2	O/PU	

123	M1_TXD1/ P1_RXD1	O/PU	MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXCLK. M_TXD[3:0]/P_RXD[3:0] are output pins in both MII MAC mode and MII PHY mode.
122	M1_TXD0/ P1_RXD0	O/PU	
119	M1_RXCLK/ P1_TXCLK	IO/PU	1. M_RXCLK Pin in MII1 MAC Mode. MII Receive Clock(input). Used to synchronize M_RXD[3:0], and M_RXDV. 2. P_TXCLK Pin in MII1 PHY Mode. MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te. M_RXCLK is an input pin in MII MAC mode. P_TXCLK is an output pin in MII PHY mode.
118	M1_RXDV/ P1_TXEN	I/PU	1. M_RXDV Pin in MII1 MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on M_RXD bus. M_RXDV is synchronous to M_RXCLK. 2. P_TXEN Pin in MII1 PHY Mode. MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXCLK. M_RXDV/P_TXEN is an input pin in both MII MAC mode and MII PHY mode.
114	M1_RXD3/ P1_TXD3	I/PU	1. M_RXD[3:0] Pin in MII1 MAC Mode. MII Receive Data Bus. M_RXD[3:0] is synchronous to M_RXCLK. 2. P_TXD[3:0] Pin in MII1 PHY Mode. MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXCLK . M_RXD[3:0]/P_TXD[3:0] are input pins in both MII MAC mode and MII PHY mode.
115	M1_RXD2/ P1_TXD2	I/PU	
116	M1_RXD1/ P1_TXD1	I/PU	
117	M1_RXD0/ P1_TXD0	I/PU	

Table 6. MII2 Interface Pins

No.	Pin Name	Type	Description
88	M2_TXCLK/ P2_RXCLK	IO/LI/PD	1. M_TXCLK Pin in MII2 MAC Mode. MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. 2. P_RXCLK Pin in MII2 PHY Mode. MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV.

			The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te. M_TXCLK is an input pin in MII MAC mode. P_RXCLK is an output pin in MII PHY mode.
87	M2_TXEN/ P2_RXDV	O/PU	1. M_TXEN Pin in MII2 MAC Mode. MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXCLK. 2. P_RXDV Pin in MII2 PHY Mode. MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXCLK. M_TXEN/P_RXDV is an output pin in both MII MAC mode and MII PHY mode.
83	M2_TXD3/ P2_RXD3	O/LI/PU	1. M_TXD[3:0] Pin in MII2 MAC Mode. MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXCLK. 2. P_RXD[3:0] Pin in MII2 PHY Mode. MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXCLK. M_TXD[3:0]/P_RXD[3:0] are output pins in both MII MAC mode and MII PHY mode.
84	M2_TXD2/ P2_RXD2	O/PU	
85	M2_TXD1/ P2_RXD1	O/PU	
86	M2_TXD0/ P2_RXD0	O/LI/PU	
89	M2_RXCLK/ P2_TXCLK	IO/PU	1. M_RXCLK Pin in MII2 MAC Mode. MII Receive Clock(input). Used to synchronize M_RXD[3:0], and M_RXDV. 2. P_TXCLK Pin in MII2 PHY Mode. MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te. M_RXCLK is an input pin in MII MAC mode. P_TXCLK is an output pin in MII PHY mode.
90	M2_RXDV/ P2_TXEN	I/PU	1. M_RXDV Pin in MII2 MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on M_RXD bus. M_RXDV is synchronous to M_RXCLK. 2. P_TXEN Pin in MII2 PHY Mode. MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXCLK. M_RXDV/P_TXEN is an input pin in both MII MAC mode and MII PHY mode.

94	M2_RXD3/ P2_TXD3	I/PU	1. M_RXD[3:0] Pin in MII2 MAC Mode. MII Receive Data Bus. M_RXD[3:0] is synchronous to M_RXCLK. 2. P_TXD[3:0] Pin in MII2 PHY Mode. MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXCLK . M_RXD[3:0]/P_TXD[3:0] are input pins in both MII MAC mode and MII PHY mode.
93	M2_RXD2/ P2_TXD2	I/PU	
92	M2_RXD1/ P2_TXD1	I/PU	
91	M2_RXD0/ P2_TXD0	I/PU	

2.4. RMII Interface Pins

Table 7. RMII1 Interface Pins

No.	Pin Name	Type	Description
120	M1_TXC/ P1_RXC	IO/PU	REFCLK pin in RMII Mode. 1. In RMII1 MAC Mode, REFCLK is an input pin. 2. In RMII1 PHY Mode, REFCLK is an output pin. REF_CLK is a 50MHz clock that provides the timing reference for RXDV, RXD[1:0], TXEN, TXD[1:0].
121	M1_TXEN/ P1_RXDV	O/PU	1. TXEN Pin in RMII1 MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. 2. RXDV Pin in RMII1 PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK. M_TXEN/P_RXDV is an output pin in both MII MAC mode and MII PHY mode.
123	M1_TXD1 / P1_RXD1	O/PU	1. TXD[1:0] Pin in RMII1 MAC Mode, synchronous to REFCLK. 2. RXD[1:0] Pin in RMII1 PHY Mode, synchronous to REFCLK. M_TXD[1:0]/P_RXD[1:0] are output pins in both MII MAC mode and MII PHY mode.
122	M1_TXD0 / P1_RXD0	O/PU	
118	M1_RXDV/ P1_TXEN	I/PU	1. RXDV Pin in RMII1 MAC Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK. 2. TXEN Pin in RMII1 PHY Mode. The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. M_RXDV/P_TXEN is an input pin in both MII MAC mode and MII PHY mode.

116	M1_RXD1/ P1P_TXD1	I/PU	1. RXD[1:0] Pin in RMII1 MAC Mode, is synchronous to RXC. 2. TXD[1:0] Pin in RMII1 PHY Mode, is synchronous to TXC . M_RXD[1:0]/P_TXD[1:0] are input pins in both MII MAC mode and MII PHY mode.
117	M1_RXD0/ P1_TXD0	I/PU	

Table 8. RMII2 Interface Pins

No.	Pin Name	Type	Description
88	M2_TXC/ P2_RXC	IO/LI/PD	REFCLK pin in RMII Mode. 1. In RMII2 MAC Mode, REFCLK is an input pin. 2. In RMII2 PHY Mode, REFCLK is a output pin. REF_CLK is a 50MHz clock that provides the timing reference for RXDV, RXD[1:0], TXEN, TXD[1:0].
87	M2_TXEN/ P2_RXDV	O/PU	1. TXEN Pin in RMII2 MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. 2. RXDV Pin in RMII2 PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK. M_TXEN/P_RXDV is an output pin in both MII MAC mode and MII PHY mode.
85	M2_TXD1/ P2_RXD1	O/PU	1. TXD[1:0] Pin in RMII2 MAC Mode, synchronous to REFCLK. 2. RXD[1:0] Pin in RMII2 PHY Mode, synchronous to REFCLK. M_TXD[1:0]/P_RXD[1:0] are output pins in both MII MAC mode and MII PHY mode.
86	M2_TXD0/ P2_RXD0	O/PU	
90	M2_RXDV/ P2_TXEN	I/PU	1. RXDV Pin in RMII2 MAC Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK. 2. TXEN Pin in RMII2 PHY Mode. The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. M_RXDV/P_TXEN is an input pin in both MII MAC mode and MII PHY mode.
92	M2_RXD1/ P2_TXD1	I/PU	1. RXD[1:0] Pin in RMII2 MAC Mode, is synchronous to RXC.
91	M2_RXD0/	I/PU	

	P2_TXD0		2. TXD[1:0] Pin in RMII2 PHY Mode, is synchronous to TXC . M_RXD[1:0]/P_TXD[1:0] are input pins in both MII MAC mode and MII PHY mode.

2.5. SerDes Interface Pins

Table 9. SerDes Interface Pins

No.	Pin Name	Type	Description
109	S0RXP	AI	1000Base-X/100FX/SGMII/2500Base-X SerDes 0 Interface Receive Data Differential Input Pair.
108	S0RXN	AI	
106	S0TXP	AO	1000Base-X/100FX/SGMII/2500Base-X SerDes 0 Interface Transmit Data Differential Output Pair.
105	S0TXN	AO	
103	S1RXN	AI	1000Base-X/100FX/SGMII/2500Base-X SerDes 1 Interface Receive Data Differential Input Pair.
102	S1RXP	AI	
100	S1TXN	AO	1000Base-X/100FX/SGMII/2500Base-X SerDes 1 Interface Transmit Data Differential Output Pair.
99	S1TXP	AO	

2.6. Parallel LED Pins

Table 10. Parallel LED Pins

No.	Pin Name	Type	Description
28	P9LED2	IO/LI/PU	Default port 9 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
27	P9LED1	IO/LI/PU	Default port 9 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
26	P9LED0	IO/LI/PU	Default port 9 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
29	P8LED2	IO/PU	Default port 8 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
83	P8LED	IO/LI/PU	Default port 8 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
84	P8LED0	IO/LI/PU	Default port 8 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
85	P7LED2	O/PU	Default port 7 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
87	P7LED1	O/PU	Default port 7 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM

86	P7LED0	O/LI/PU	Default port 7 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
89	P6LED2	O/PU	Default port 6 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
91	P6LED1	O/PU	Default port 6 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
90	P6LED0	O/PU	Default port 6 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
92	P5LED2	O/PU	Default port 5 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
94	P5LED1	O/PU	Default port 5 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
93	P5LED0	O/PU	Default port 5 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
113	P4LED2	IO/LI/PU	Default port 4 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
115	P4LED1	O/PU	Default port 4 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
114	P4LED0	O/PU	Default port 4 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
117	P3LED2	O/PU	Default port 3 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
116	P3LED1	O/PU	Default port 3 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
118	P3LED0	O/PU	Default port 3 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
119	P2LED2	O/PU	Default port 2 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
121	P2LED1	O/PU	Default port 2 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
120	P2LED0	O/LI/PU	Default port 2 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
122	P1LED2	IO/LI/PU	Default port 1 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
124	P1LED1	IO/LI/PU	Default port 1 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
123	P1LED0	IO/LI/PU	Default port 1 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
125	P0LED2	IO/LI/PU	Default port 0 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM

128	P0LED1	O/PU	Default port 0 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
129	P0LED0	IO/LI/PU	Default port 0 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM

2.7. Serial LED Pins

Table 11. Serial LED Pins

No.	Pin Name	Type	Description
129	LED_CK	O/LI/PU	Serial Mode LED Clock Signal.
128	LED_DA	IO/PU	Serial Mode LED Data Signal.

2.8. SPI FLASH Pins

Table 12. SPI FLASH 0 Interface Pins

No.	Pin Name	Type	Description
89	SPF0_CS	IO/PU	SPI FLASH0 chip select signal.
87	SPF0_SO	IO/PU	In Serial I/O Mode, SPI Serial FLASH0 Serial Data Output (YT9218MB input pin) In Dual I/O Mode, SPI FLASH0 bi-directional pin (this is MSB)
86	SPF0_SI	IO/LI/PU	In Serial I/O Mode SPI Serial FLASH0 Serial Data Input (YT9218MB output pin) In Dual I/O Mode SPI FLASH0 bi-directional pin (this is LSB)
85	SPF0_SCK	IO/PU	SPI FLASH0 Clock.

Table 13. SPI FLASH 1 Interface Pins

No.	Pin Name	Type	Description
33	SPF1_CS	O/PU	SPI FLASH1 chip select signal.
32	SPF1_SO	IO/PU	In Serial I/O Mode, SPI Serial FLASH1 Serial Data Output (YT9218MB input pin) In Dual I/O Mode, SPI FLASH1 bi-directional pin (this is MSB)
31	SPF1_SI	IO/PU	In Serial I/O Mode SPI Serial FLASH1 Serial Data Input (YT9218MB output pin) In Dual I/O Mode

			SPI FLASH1 bi-directional pin (this is LSB)
30	SPF1_SCK	IO/LI/PU	SPI FLASH1 Clock.

2.9. UART Interface Pins

Table 14. UART 0 Interface Pins

No.	Pin Name	Type	Description
90	UART0_RX	IO/LI/PU	UART0 RX pin.
91	UART0_TX	IO/LI/PU	UART0 TX pin.

Table 15. UART 1 Interface Pins

No.	Pin Name	Type	Description
29	UART1_RX	IO/LI/PU	UART1 RX pin.
28	UART1_TX	IO/LI/PU	UART1 TX pin.

2.10. Master I2C Interface Pins

Table 16. Master I2C 1 Interface Pins

No.	Pin Name	Type	Description
25	I2C1_SCL	IO/OD/PU	SCL pin in Group1 Master I2C.
29	I2C1_SDA	IO/OD/PU	SDA pin in Group1 Master I2C.

Table 17. Master I2C 2 Interface Pins

No.	Pin Name	Type	Description
134	I2C2_SCL	IO/OD/PU	SCL pin in Group2 Master I2C.
137	I2C2_SDA	IO/OD/LI/PU	SDA pin in Group2 Master I2C.

Table 18. Master I2C 3 Interface Pins

No.	Pin Name	Type	Description
22	I2C3_SCL	IO/OD/PU	SCL pin in Group3 Master I2C.
23	I2C3_SDA	IO/OD/PU	SDA pin in Group3 Master I2C.

2.11. Master SMI Interface Pins

Table 19. Master SMI 1 Interface Pins

No.	Pin Name	Type	Description
25	SMI1_MDC	IO/OD/PU	MDC pin in Group1 Master SMI.
29	SMI1_MDIO	IO/OD/PU	MDIO pin in Group1 Master SMI.

Table 20. Master SMI 2 Interface Pins

No.	Pin Name	Type	Description
134	SMI2_MDC	IO/OD/PU	MDC pin in Group2 Master SMI.
137	SMI2_MDIO	IO/OD/LI/PU	MDIO pin in Group2 Master SMI.

Table 21. Master SMI 3 Interface Pins

No.	Pin Name	Type	Description
22	SMI3_MDC	IO/OD/PU	MDC pin in Group3 Master SMI.
23	SMI3_MDIO	IO/OD/PU	MDIO pin in Group3 Master SMI.

2.12. Management Interface Pins

Table 22. Management Interface Pins

No.	Pin Name	Type	Description
134	SSPI_CS	IO/PU	SPI slave Mode Chip Select Input.
135	SCL/ MDC/ SSPI_SCK	IO/OD/PU	1. EEPROM auto-load mode serial clock output 2. I2C slave mode serial clock input 3. MDC/MDIO slave mode serial clock input 4. SPI slave Mode serial clock input
136	SDA/ MDIO/ SSPI_SI	IO/OD/PU	1. EEPROM auto-load mode serial data input 2. I2C slave mode serial data 3. MDC/MDIO slave mode serial data 4. SPI slave Mode serial data input
137	SSPI_SO	IO/PU	SPI slave Mode serial data output

2.13. GPIO Pins

Table 23. GPIO Pins

No.	Pin Name	Type	Description
92	GPIO0	IO/PU	General Purpose Input/Output Interfaces IO0.
90	GPIO1	IO/PU	General Purpose Input/Output Interfaces IO1.
125	GPIO2	IO/LI/PU	General Purpose Input/Output Interfaces IO2.
113	GPIO3	IO/LI/PU	General Purpose Input/Output Interfaces IO3.
121	GPIO4	IO/LI/PU	General Purpose Input/Output Interfaces IO4.
116	GPIO5	IO/PU	General Purpose Input/Output Interfaces IO5.
115	GPIO6	IO/PU	General Purpose Input/Output Interfaces IO6.
91	GPIO7	IO/PU	General Purpose Input/Output Interfaces IO7.
83	GPIO8	IO/LI/PU	General Purpose Input/Output Interfaces IO8

84	GPIO9	IO/LI/PU	General Purpose Input/Output Interfaces IO9.
85	GPIO10	IO/LI/PU	General Purpose Input/Output Interfaces IO10.
86	GPIO11	IO/ LI/PU	General Purpose Input/Output Interfaces IO11.
87	GPIO12	IO/PU	General Purpose Input/Output Interfaces IO12.
88	GPIO13	IO/PD	General Purpose Input/Output Interfaces IO13.
89	GPIO14	IO/PU	General Purpose Input/Output Interfaces IO14.
93	GPIO15	IO/PU	General Purpose Input/Output Interfaces IO15.
94	GPIO16	IO/PU	General Purpose Input/Output Interfaces IO16.
114	GPIO17	IO/PU	General Purpose Input/Output Interfaces IO17.
117	GPIO18	IO/PU	General Purpose Input/Output Interfaces IO18.
24	GPIO19	IO/LI/PU	General Purpose Input/Output Interfaces IO19.
30	GPIO20	IO/PU	General Purpose Input/Output Interfaces IO20
31	GPIO21	IO/LI/PU	General Purpose Input/Output Interfaces IO21.
32	GPIO22	IO/PU	General Purpose Input/Output Interfaces IO22.
33	GPIO23	IO/PU	General Purpose Input/Output Interfaces IO23.

2.14. Configuration Pins

Table 24. Configuration Pins

No.	Pin Name	Type	Description
20	DIS_LPD	LI/PU	Loop detection configuration Pull Up: disable LPD. Pull Down: enable LPD.
24	SPF_MUX_SEL	LI/PU	SPI FLASH Interface Select. Pull Up: Select SPI FLASH 0 Interface. Pull Down: Select SPI FLASH 1 Interface.
26	EN_PWRLIGHT	LI/PU	Disable/Enable LED function When Powered On. Pull Up: Enable LED. Pull Down: Disable LED.
27	DISAUTOLOAD	LI/PU	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload upon power on or reset Pull Down: Enable EEPROM autoload upon power on or reset
28	EEE_EN	LI/PU	Enable 802.3az EEE. Pull Up: Enable 802.3az EEE. Pull Down: Disable 802.3az EEE.
83	DIS_LED	LI/PU	Disable/Enable LED function When Powered On. Pull Down: Enable LED Pull Up: Disable LED.

84	EN_ FLASH	LI/PU	Enable SPI FLASH Interface. Pull Up: Enable FLASH interface Pull Down: Disable FLASH interface
113	DIS_SPIS	LI/PU	Disable Slave SPI Interface for External CPU Access YT9218MB Register Pull Up: Disable SPI Slave Interface and refer [SMI_SEL_1, SMI_SEL_0] Pull Down: Enable SPI Slave Interface
122	SMI_SEL_1	LI/PU	Slave I2C/Slave MII Management Interface Selection [SMI_SEL_1, SMI_SEL_0] 00: LSB I2C 01: MSB I2C 10: MDC/MDIO 11: Simply I2C
129	SMI_SEL_0	LI/PU	
123	MID29	LI/PU	Slave SMI (MDC/MDIO) Device Address. Pull Up: Slave SMI (MDC/MDIO) Device Address is 0x1d Pull Down: Slave SMI (MDC/MDIO) Device Address is 0x0
124	DIS_MCU	LI/PU	Disable Embedded MCU. Pull Up: Disable embedded MCU upon power on or reset Pull Down: Enable embedded MCU upon power on or reset
125	EN_PHY	LI/PU	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY
137	EEPROM_MOD	LI/PU	EEPROM Mode Selection. Pull Up: EEPROM 24Cxx Size greater than or equal to 32Kbits (24C32~). Pull Down: EEPROM 24Cxx Size less than or equal to 16Kbit (24C02~24C16).
128	SWITCH_ID1	LI/PU	Switch_ID[1:0] for slave MDC/MDIO format.
121	SWITCH_ID0	LI/PU	
85	RESERVED_0	LI/PU	Reserved. This pin must be pulled up to DVDDIO via an external 4.7k ohm resistor upon power on.
86	RESERVED_1	LI/PU	Reserved. This pin must be pulled up to DVDDIO via an external 4.7k ohm resistor upon power on.
120	RESERVED_2	LI/PU	Reserved. This pin must be pulled up to DVDDIO via an external 4.7k ohm resistor upon power on.

2.15. Power Related Pins

Table 25. Power Related Pins

No.	Pin Name	Type	Description
16,36	DVDDIO	P	Digital power 3.3V/2.5V/1.8V
111,126	DVDDIO_1	P	Digital power 3.3V/2.5V/1.8V for Extension Port 1
82,96	DVDDIO_2	P	Digital power 3.3V/2.5V/1.8V for Extension Port 2
17,18,34,35,95,112,127,130	DVDDL	P	Digital power 1.1V
6,15,37,47,57,61,71,81,138,148,158,162,172	AVDDH	AP	Analog power 3.3V
1,12,42,52,66,76,143,153,167	AVDDL	AP	Analog power 1.1V
97	SVDDH	AP	SerDes power 3.3V
98,104,107	SVDDL	AP	SerDes power 1.1V
159	PLLVDDL0	AP	PLL0 Power 1.1V.
58	PLLVDDL1	AP	PLL1 Power 1.1V.
8	AGND	AG	Analog GND.
101,110	SGND	AG	SerDes GND.
161	PLLGND0	AG	PLL0 GND.
60	PLLGND1	AG	PLL1 GND.
EPAD	GND	G	GND

2.16. Clock Pins

Table 26. Clock Pins

No.	Pin Name	Type	Description
132	XTAL_I	XT	25MHz Crystal Input pin. If use external oscillator or clock from another device. 1. When connect an external 25MHz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25MHz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.
131	XTAL_O	XT	25MHz Crystal Output pin. If use external oscillator or clock from another device. 1. When connect an external 25MHz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND.

			2. When connect an external 25MHz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.

2.17. Reset Pins

Table 27. Reset Pins

No.	Pin Name	Type	Description
133	RESETn	AI/PU	Hardware reset, active low. Requires an external pull-up resistor

2.18. Miscellaneous Pins

Table 28. Miscellaneous Pin

No.	Pin Name	Type	Description
10	RBIAS	AO	Bias Resistor. An external 2.49 kΩ ± 1% resistor must be connected between the RBIAS pin and GND.
19	INTERRUPT	O/PU	Interrupt Output.
21	DYING_GASP	AI	The reference voltage pin for dying gasp.
7,9,11,13,14, 59, 160	NC	–	Not connect. Must be left floating in normal operation.

3. Integrated PHY Functional Overview

YT9218MB integrates eight 10/100/1000M Giga PHY ports. Each PHY port supports 1000Base-T, 100Base-TX, and 10Base-Te by four signal pairs, namely MDIAP/N, MDIBP/N, MDICP/N and MDIDP/N. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. For 1000Base-T, all four pairs are used in both directions at the same time. For 100Base-TX and 10Base-Te, only pairs MDIAP/N and MDIBP/N are used.

3.1. Transmit Encoder Modes

3.1.1. 1000BASE-T

In 1000BASE-T mode, the PHY port scrambles data bytes to be transmit from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5E UTP cable.

3.1.2. 100BASE-TX

In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

3.1.3. 10BASE-Te

In 10BASE-Te mode, the PHY port transmits Manchester-encoded data.

3.2. Receive Decoder Modes

3.2.1. 1000BASE-T

In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately, and data is output to the MAC interfaces.

3.2.2. 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to MAC interfaces after data stream delimiters have been translated.

3.2.3. 10BASE-Te

In 10BASE-Te mode, the recovered 10BASE-Te signal is decoded from Manchester then aligned.

3.3. Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects back as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in drastic SNR degradation on the receive signal. The PHY port implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

3.4. NEXT Canceller

The 1000BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high frequency crosstalk occurs between adjacent pairs in the bundle. The PHY port uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The PHY port cancels NEXT by subtracting an estimate of these signals from the equalizer output.

3.5. Baseline Wander Canceller

Baseline wander results from Ethernet links that AC-couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000BASE-T environment than in 100BASE-TX due to the DC baseline shift in the transmit and receive signals. The YT9218MB device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

3.6. Digital Adaptive Equalizer

The digital adaptive equalizer removes inter- symbol interference at the receiver. The digital adaptive equalizer takes signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best optimized signal-to-noise (SNR) ratio.

3.7. Auto-Negotiation

The integrated PHY port negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and abilities received from link partner.

Auto negotiation is enabled for YT9218MB by default and can be disabled by software control.

3.8. Auto Crossover and Polarity Correction

The integrated PHY port can detect and correct two types of cable errors: auto crossover of pairs within the UTP cable (between pair 0 and pair 1, and(or) between pair 2 and pair 3) and swapping of polarity within a pair.

4. General Function Description

4.1. Reset

4.1.1. Hardware Reset

YT9218MB have a hardware reset pin (nRESET) which is low active. The reset signal should be active for at least 10ms. Hardware reset should be applied after power on correctly.

After reset is released, the YT9218MB will start the reset initialization procedures by the following steps:

1. All internal logic are reset to a known state, and all registers are resetted to default value.

2. Latch input value on configuration pins which are used as configuration information to provide flexible applications.

3. Complete the memory BIST process and initialize the packet buffer.

4. Autoload from the EEPROM, or boot from Flash or EEPROM by internal CPU if needed.

4.1.2. Software Reset

YT9218MB supports two software resets can be triggered by programming switch global control register: a chip reset (CHIP_RESET, bit 31 of register 0x8_0000) and a software reset (SW_RESET, bit 1 of register 0x8_0000).

4.1.2.1. CHIP_RESET

The CHIP_RESET is set to 1 to take effect and self-clear. The chip will follow the steps below:

1. All the digital and analog circuit will be reset to default.

2. The packet buffer will be reinitialized and all the Lookup and VLAN tables will be cleared.

3. Autoload from the EEPROM, or boot from Flash or EEPROM by internal CPU if needed, and the chip will be configured again.

4. The integrated PHYs will restart auto-negotiation process.

4.1.2.2. SW_RESET

The SW_RESET is also set to 1 to take effect and self-clear, and its function is similar to the CHIP_RESET except the analog circuit of integrated PHYs will not be reset.

4.2. Flexible Applications by Configuration Pins

According to the system application, user can select the most suitable mode by configuration pins DISAUTOLOAD, DIS_MCU, EN_SPIF, DIS_SPI and SMI_SEL, shown in the following table.

Table 29. Flexible Applications

DISAUTOLOAD	DIS_MCU	EN_SPIF	DIS_SPI	SMI_SEL [1:0]	Initial Stage Loading Data*	
					From	To
0	0	1	X	X	XIP	
0	1	0	X	2b’00/ 2b’01/ 2b’11	EEPROM	Register
Others					No Action	

Note*: Initial Stage means power on, hardware reset, or software reset.

4.3. IEEE 802.3x Full Duplex Flow Control

YT9218MB supports IEEE 802.3x flow control in 10/100/1000M full duplex modes. The flow control ability can be decided by the result of Auto-Negotiation or software configuration.

In most cases, MAC ports with integrated PHY get flow control ability by Auto-Negotiation, and two extra MAC ports with MII/RMII/RGMII by software configuration.

4.4. Half Duplex Flow Control

When PHY port works as 10/100M half duplex modes, it will collide with the link partner when transmit and receive data at the same time. Then this will make the buffer overflow and drop packets. YT9218MB supports two methods, jam mode and defer mode, to avoid this.

The maximum retry count limitation is 16 which follows the definition in IEEE 802.3. But for YT9218MB supports configure the retry count limitation is configurable and will not drop packet by default.

4.5. FDB Table

4.5.1. Lookup and Forward

YT9218MB MAC address table consists of a 4K-entry FDB table. On receiving a packet, YT9218MB uses DA, FID to search the 4K-entry FDB table. If there is an entry matched, the received packet will be forwarded to the corresponding destination port. If there is no entry matched, YT9218MB flood the packet according to the VLAN configuration.

4.5.2. MAC Address Learning

When a packet is received, YT9218MB uses the source MAC address and FID to search the 4K-entry FDB table. If there is a match with one of the entries, YT9218MB will update the entry with new information. If there is no matching entry, the packet information is learned into new entry.

4.5.3. MAC Address Aging

The aging mechanism of MAC address is as following: When a packet flow reaches a port, the port learns the MAC address dynamically. If the port keeps receiving this packet flow, the corresponding MAC address is updated continuously and will not be aged. If the packet flow stops, the MAC address is deleted after the aging time. Aging time of YT9218MB is between 5 and 327,675 seconds (typical is 300 seconds).

4.6. IVL SVL and IVL/SVL

YT9218MB supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (Both Independent and Shared VLAN Learning).

4.7. Reserved Multicast Address

YT9218MB supports the ability to drop/forward/copy IEEE 802.3 specified reserved multicast MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting for these reserved multicast MAC addresses is forwarding. Frames with multicast MAC address 01-80-C2-00-00-01 (802.3x Pause) will always be dropped.

4.8. Storm Control

YT9218MB supports storm control for broadcast, multicast and unknown DA, each storm type can be enabled/disabled per-port, default is disabled. If the Rx rate of those types of packets exceeds configured rate, all following storm packets will be dropped. The rate can be configured with packet mode (pps) or byte mode (bps).

4.9. Port Security

YT9218MB supports following security mechanism to prevent malicious attacks:

- Per-port enable/disable SA auto-learning
- Per-port enable/disable FDB aging update
- Per-port enable/disable unknown DA packet drop

4.10. MIB

YT9218MB supports following MIB standards for common management.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

4.11. Port Mirror

YT9218MB supports 1 group of port mirror for all ports. The TX/RX or both direction packets from each mirrored port can be mirrored to the monitor port.

4.12. VLAN Function

YT9218MB supports 4K VLAN table. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs, also support IVC (VLAN Translate) function. Ingress-filtering, egress-filtering and accept-frame-type options provide flexible VLAN configuration:

Ingress Filtering: Packets from an input port that is not in the VLAN member will be dropped.

Egress Filtering: Packets to an output port that is not in the VLAN member will be dropped.

Accept Frame Type: the input port can configured 'Accept All', 'Accept Tagged', 'Accept Untagged' and 'Drop All' .

The packets at the output port can be inserted or removed VLAN tag. For untagged packets YT9218MB can insert VLAN TAG or remove the VLAN TAG from tagged frames.

4.12.1. Port-Based VLAN

The 4K-entry VLAN Table designed into YT9218MB provides full flexibility for users to configure the input ports to associate with different VLAN entries. Each input port can join with more than one VLAN entry.

Port-based VLAN mapping is the simplest and effective mapping rule. It defines VLAN members based on device ports. All the packets received from a given input port will be forwarded to this port's VLAN members.

4.12.2. IEEE 802.1Q Tag-Based VLAN

In 802.1Q VLAN mapping, device uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. YT9218MB compares the VID in the VLAN tag with the 4K VLAN Table to determine the packets forwarding action.

4.12.3. Port VID

YT9218MB supports Port VID (PVID) for each port. When untagged or priority tagged packet forwarded to output port without hit other assign vid rules and the egress tag mode set tagged, device support to insert a PVID in the VLAN tag.

4.13. QoS Function

YT9218MB supports 8 unicast priority queues, 4 multicast priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1Q Tag-based priority, VLAN entry-based priority, MAC SA-based priority, MAC DA-based priority, DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in YT9218MB, the packet's priority will be assigned based on the priority selection table.

Per-queue in each output port can be set as Strict Priority (SP) or Deficit Weighted Round Robin (DWRR) for packet scheduling algorithm.

4.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, if flow control enable, this port will send out a 'pause ON' frame, if flow control disable, will drop the input packet. Per-port input bandwidth control rates can be set from 9Kbps to 2.5Gbps (in 9Kbps steps).

4.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet based on various rules. YT9218MB can recognize the QoS priority information of receiving packets to give a different service priority.

YT9218MB identifies the priority of packets based on seven types of QoS priority information:

- Port-based priority
- 802.1Q-based priority
- DSCP-based priority
- ACL-based priority
- VLAN entry-based priority

• MAC SA-based priority

• MAC DA -based priority

4.13.3. Priority Queue Scheduling

Packet scheduler controls the various traffics (control packets sending sequence of the priority queue), YT9218MB scheduling algorithm is DWRR.

• Deficit Weighted Round Robin (DWRR): supports byte based or packet based

In addition, each queue of each port can select Strict Priority or DWRR packet schedule, and DWRR can co-exist with SP schedule.

4.13.4. IEEE 802.1Q and DSCP Remarking

YT9218MB supports the IEEE 802.1Q and DSCP remarking function. If remarking function enable, when packets egress from one of the 12 queues, the packet's 802.1Q priority and DSCP can be remarked to a configured value. 802.1Q priority & DSCP value can be remarked based on internal priority.

4.14. IGMP & MLD Snooping Function

YT9218MB supports hardware IGMPv1/v2 snooping and MLDv1/v2 snooping. These multicast groups are learned and deleted/aged out automatically. For data packets of a known multicast group, YT9218MB forwards them according to the learned group membership.

YT9218MB supports bypass designated IP multicast address with global control and per ingress port join/leave packets allowed control.

YT9218MB supports IGMP Dynamic Router Port Learning, dynamic router port enable control is based on per-port basis. The aging time can be configured by SW, the router port will be removed when timeout.

YT9218MB supports IGMP/MLD Hardware Fast Leave, when leave, the multicast group will be marked as invalid again.

YT9218MB supports IGMP/MLD Packet Copy/Trap/Flood based on global control.

4.15. IEEE 802.1x Function

YT9218MB supports IEEE 802.1x Port-based.

• Port-Based Access Control for each port

• Authorized Port-Based Access Control for each port

• Port-Based Access Control Direction for each port

• Guest VLAN

4.15.1. Port-Based Access Control

Each port of YT9218MB can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

4.15.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

4.15.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

4.15.4. Guest VLAN

When YT9218MB enables the Port-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, YT9218MB will drop all packets from this port. If configure Guest VLAN, YT9218MB will allow packets from unauthorized ports to be forwarded to a limited VLAN domain.

4.16. Spanning Tree

IEEE 802.1D Spanning Tree allows bridges to prevent and resolve Layer 2 forwarding loops automatically. Switches exchange BPDUs and configuration messages and selectively enable and disable forwarding on specified ports. YT9218MB supports 16 STP instances and four status (Disabled/Blocking/Learning/Forwarding) for each port when CPU implements STP/RSTP/MSTP function.

4.17. Embedded RISC-V

A RISC-V MCU is embedded in YT9218MB to support software management/protocol functions. The RISC-V MCU can transmit to or receive frames from the switch core. The features of the RISC-V MCU are listed below:

• On-chip 64K SRAM

• On-chip 16K boot ROM

- 2K I-Cache
- Up to 8M-Byte serial I/O, dual I/O SPI Flash supported

4.18. Cable Status Diagnostic

Physical layer transceivers of YT9218MB supports Motorcomm Advanced Cable Status Diagnostic (CSD) feature. Some of the possible problems that can be diagnosed in each differential pair. The result of CSD are summarized to normal, open and short.

4.19. LED Indicators

The YT9218MB supports parallel and serial mode LEDs for each port. Each port has three LED indicator pins, LED0, LED1, and LED2. Each LED of each port may have different indicator information defined in Table 30. LED0 default indicate Link/Act, LED1 default indicate 1000M_Link, and LED2 default indicate 100M_Link.

YT9218MB supports power-on-blinking feature by the EN_PWRLIGHT pin and software configuration. The LEDs will blink once after reset.

Table 30. LED Definitions

LED Definition	Description
Full	Full Duplex Indicator. LED on when the corresponding port link at full duplex.
Half	Half Duplex Indicator. LED on when the corresponding port link at half duplex.
Link	Link Indicator. LED on when the corresponding port link up.
1000M_Link	1000Mbps Link Indicator. LED on when the corresponding port link at 1000Mbps.
100M_Link	100Mbps Link Indicator. LED on when the corresponding port link at 100Mbps.
10M_Link	10Mbps Link Indicator. LED on when the corresponding port link at 10Mbps.
Act	Activity Indicator. LED blink when the corresponding port is transmitting or receiving.
1000M_Act	1000Mbps Activity Indicator. LED blink when the corresponding port link at 1000Mbps and is transmitting or receiving.
100M_Act	100Mbps Activity Indicator. LED blink when the corresponding port link at 100Mbps and is transmitting or receiving.
10M_Act	10Mbps Activity Indicator. LED blink when the corresponding port link at 10Mbps and is transmitting or receiving.
TX_Act	TX Activity Indicator. LED blink when the corresponding port is transmitting.
RX_Act	RX Activity Indicator. LED blink when the corresponding port is receiving.
EEE_Act	EEE Mode Indicator. LED blink when the corresponding port enter EEE mode.
Loop_Act	Loop Detection Indicator. LED blink when the corresponding port detect a loop.

4.19.1. Parallel LED Mode

In parallel LED mode, each PHY port has three LED indicator pins.

LED signals are active low by default. The LED pins also support hardware configuration functions, so they are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. When the pin input is pulled high upon reset, the pin output is active low for LED function after reset. When the pin input is pulled down upon reset, the pin output is active high for LED function after reset. Typical values for pull-up/pull-down resistors are 4.7KΩ. Refer to Figure 3 for more information.

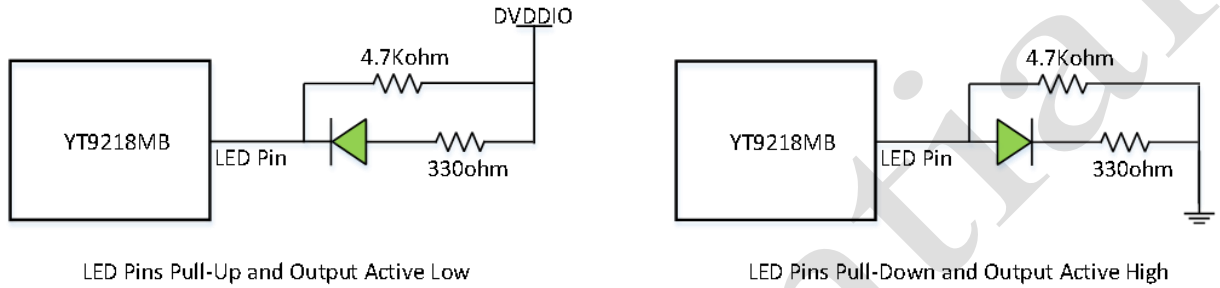

Figure 3. Pull-Up and Pull-Down of LED Pins

The LED Pins can also support Bi-color LED application. Both LED pins connected to the Bi-color LED should be the same polarity active, and the LED definition of both will not appear at the same time.

For example: Refer to Figure 4, PnLED1 and PnLED2 will be Pull-Up or Pull-Down together. The PnLED1 definition is 1000M_link. Nevertheless, the PnLED2 definition is 100M_link. PnLED1 and PnLED2 will not be ON at the same time.

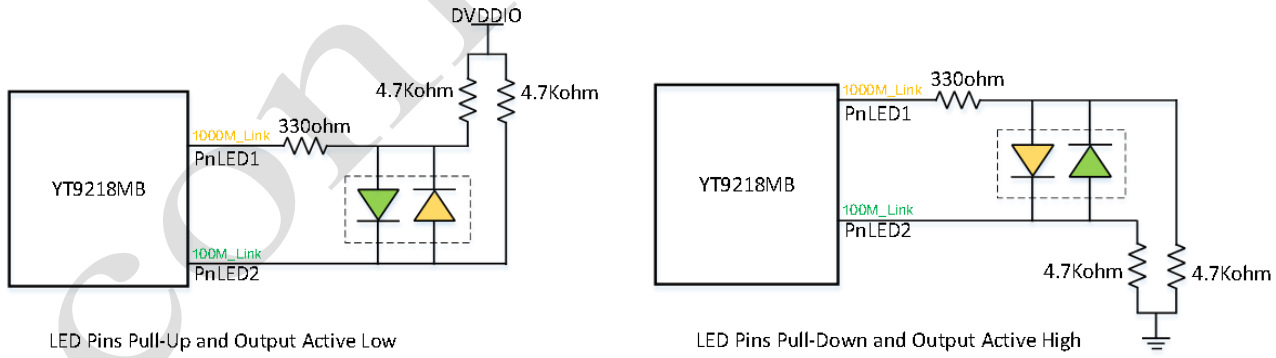

Figure 4. Typical Application for Bi-color LED

4.19.2. Serial LED Mode

Refer to Table 11, LED_CK and LED_DA pins of YT9218MB device are used for the serial LED mode. In this mode, each port supports up to three LED indicator, LED0, LED1, and

LED2. If only two LED indicator needed, LED0 and LED1 will be used. Similarly, LED0 will be used if only one LED indicator needed.

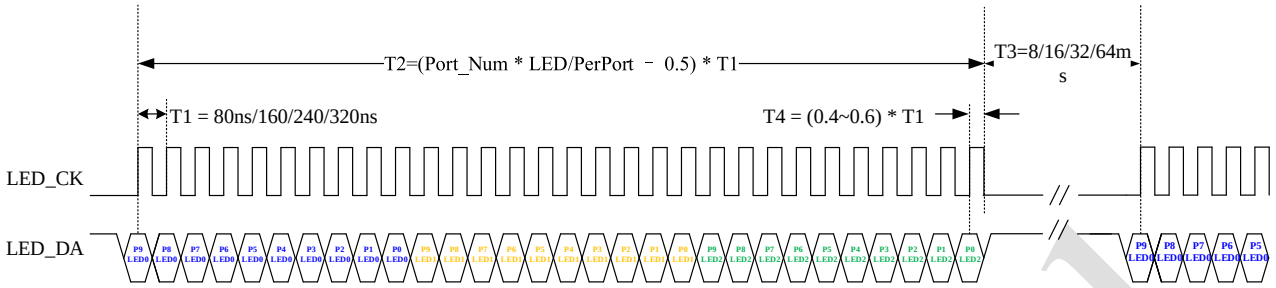

Figure 5. Serial LED Mode

In this mode, a parallel-out serial shift register device, such as 74HC164, converts LED_CK and LED_DA signals to parallel signals to drive LED indicators. Typical usage is shown in the following diagram.

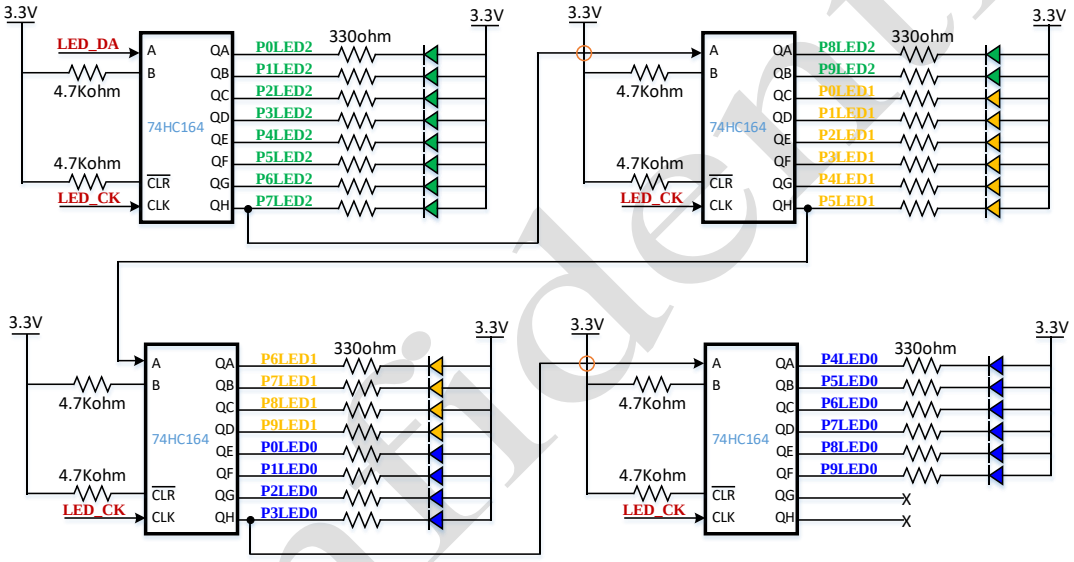

Figure 6. Typical Usage With 74HC164

4.20. Link Down Power Saving (Sleep Mode)

Physical layer transceivers of YT9218MB supports link down power saving, also called sleep mode. When UTP port link down and no signals over UTP cable for 40 seconds, Physical layer transceivers will enter sleep mode. In this mode, some circuits of physical layer transceivers will be disabled, and the power consumption of whole chip will be lower.

Once detecting signals over UTP cable, the physical layer transceiver will exit sleep mode to normal mode.

4.21. Energy Efficient Ethernet (EEE)

YT9218MB supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation.

IEEE 802.3az is an extension of the IEEE 802.3 standard. It defines the PHY transceivers to operate in Low Power Idle (LPI) mode which supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY transceiver's circuitry and save power consumption.

When Low Power Idle mode is enabled by MAC and PHY, the YT9218MB MAC uses Low Power Idle signaling to indicate to the PHY that a period of idle in the data stream is expected. Both local and link partner PHY transceiver may use this information to enter power saving modes.

4.22. Interrupt Pin for External CPU

The YT9218MB provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with mask.

When port link-up or link-down interrupt mask is enabled, the YT9218MB will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

5. Interface Descriptions

5.1. SPI Flash Interface

YT9218MB supports two group SPI flash interfaces. Both support Serial I/O and Dual I/O operation modes, 3-byte address mode access and up to 8Mbyte size flash. The value of the configuration pin SPF_MUX_SEL upon power on or reset will decide which SPI interface to be used. See Table 22 and Table 29 for more details about the spi flash interface.

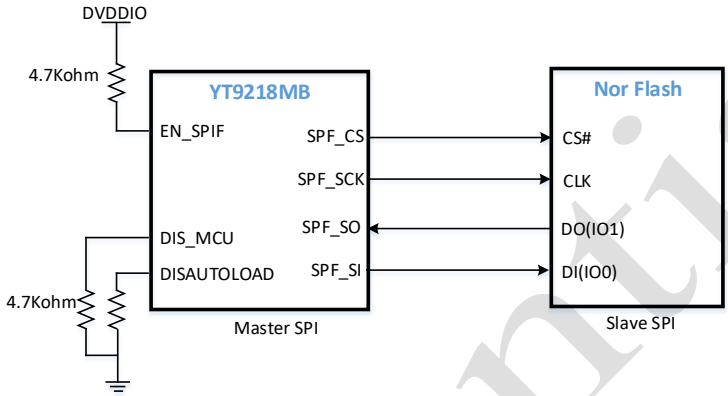

Figure 7. XIP On Flash

5.2. Master I2C Interface

YT9218MB supports two group Master I2C interfaces to access peripheral slave I2C device. Due to the I2C interface pins are shared with other functions, it needs to enable I2C function by software programming. Besides, it should be noted that the type of I2C interface is Open Drain. Pull-Up resistors, for example 4.7Kohm, should be connected to SCL and SDA signals.

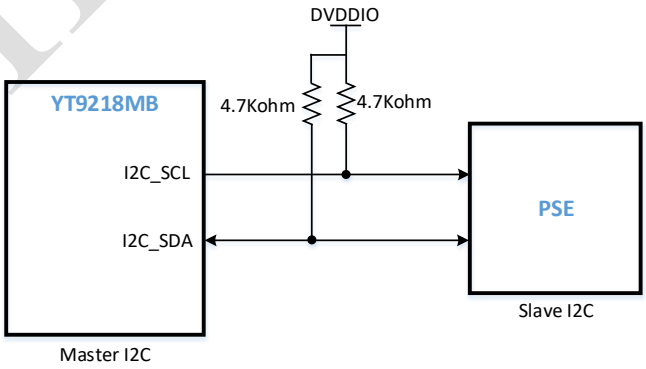

Figure 8. Master I2C Interface Connection Example

5.3. Master SMI Interface

YT9218MB also supports two group Master Serial Management Interfaces (SMI). The SMI interface supports to access external devices, such as PHY transceivers, and is compatible with IEEE 802.3u clause 22 and clause 45. SMI (MDC/MDIO) pins shared with other features, so it should be enabled by register configuration. MDIO pin type is Open Drain, a Pull-Up resistor, for example 1Kohm, must be connected on MDIO signal.

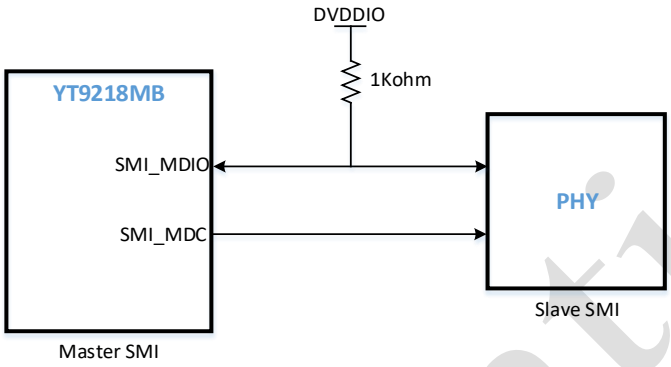

Figure 9. Master SMI (MDC/MDIO) Interface Connection Example

5.4. Master I2C Interface for EEPROM Auto-load

The EEPROM auto-load interface of the YT9218MB uses the serial bus I2C to read the Serial EEPROM. After YT9218MB power on or reset, it drives SCL and SDA to read the data from the EEPROM by configuration pins. See Table 22 and Table 29 for more details about the EEPROM auto-load interface.

As shown in the following figure, Pull-Up resistors, for example 4.7Kohm, should be connected to SCL and SDA signals.

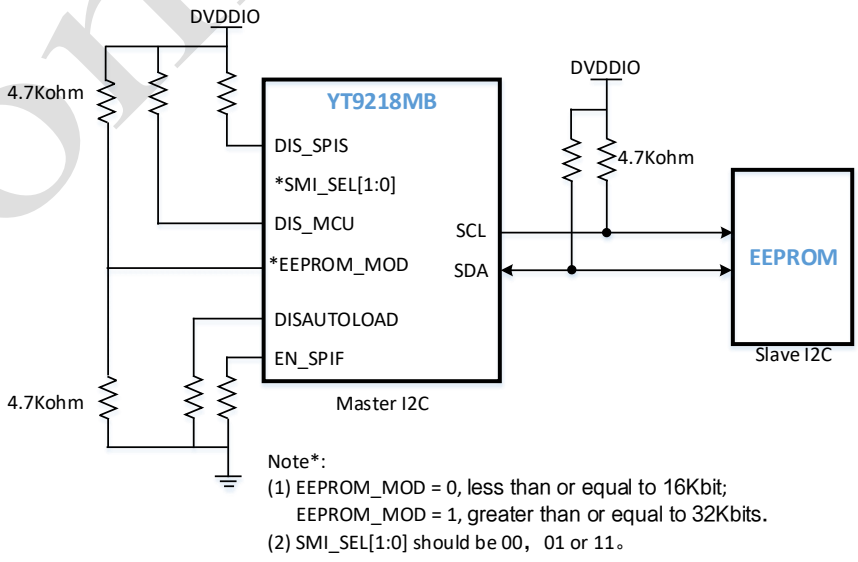

Figure 10. Auto-load From EEPROM To Register

By the size of word address (1 byte or 2 bytes), EEPROM can be divided into two sizes: 2Kbit~16Kbit and 32Kbit~512Kbit. YT9218MB supports the two type EEPROM, and the configuration pin EEPROM_MOD decides which size to be used.

5.5. Management Interfaces

5.5.1. Slave I2C Interface for External CPU

YT9218MB registers can be accessed via slave I2C interface (SCK and SDA) by an external CPU. Three I2C mode could be set through the configuration pins DIS_SPIS and SMI_SEL[1:0].

5.5.1.1. LSB I2C

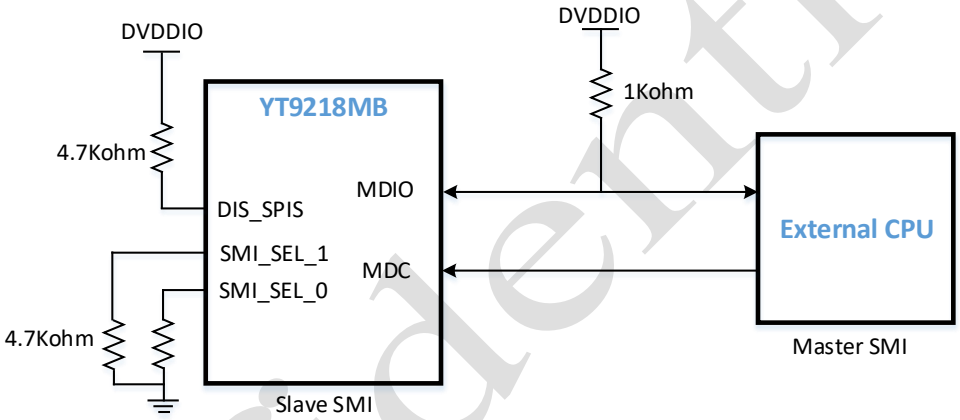

Figure 11. LSB I2C Interface Connection Example

The LSB I2C format is shown in the following diagram, Switch_ID [1:0] comes from the configuration pins SWITCH_ID_1 and SWITCH_ID_0. P stand for the even parity check of ADDR [31:2].

P = 0, if there is an even number of ‘1’ in ADDR [31:2].

P = 1, if there is an odd number of ‘1’ in ADDR [31:2].

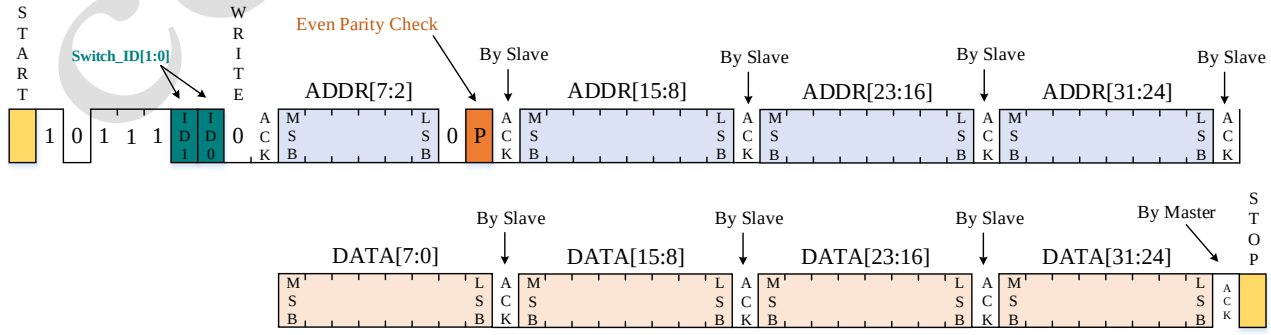

Figure 12. External CPU Write Register into YT9218MB By LSB I2C

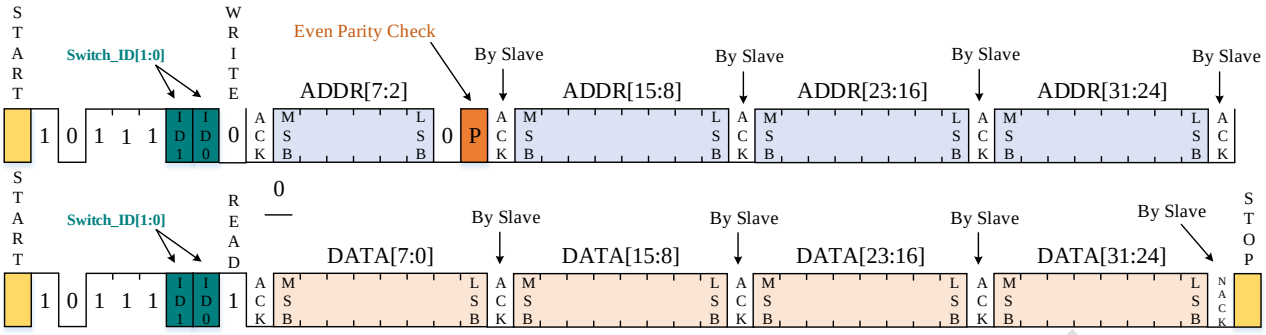

Figure 13. External CPU Read Register from YT9218MB By LSB I2C

5.5.1.2. MSB I2C

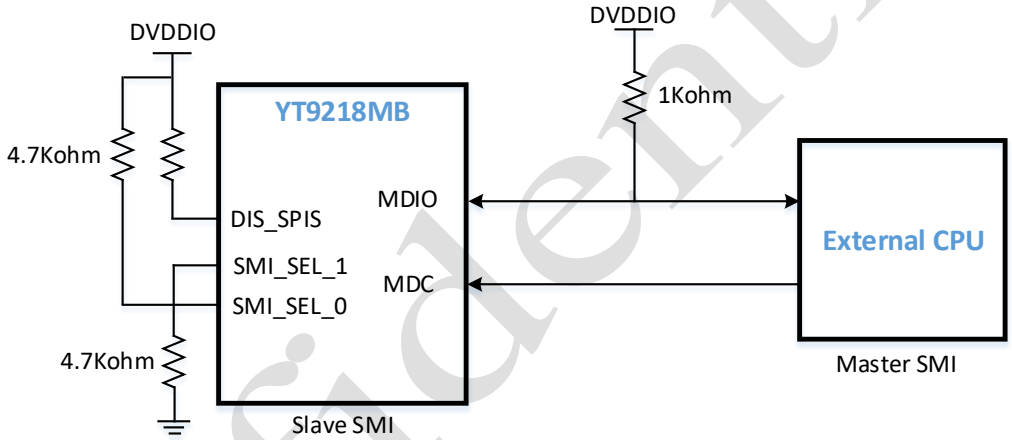

Figure 14. MSB I2C Interface Connection Example

The MSB I2C format is shown in the following diagram.

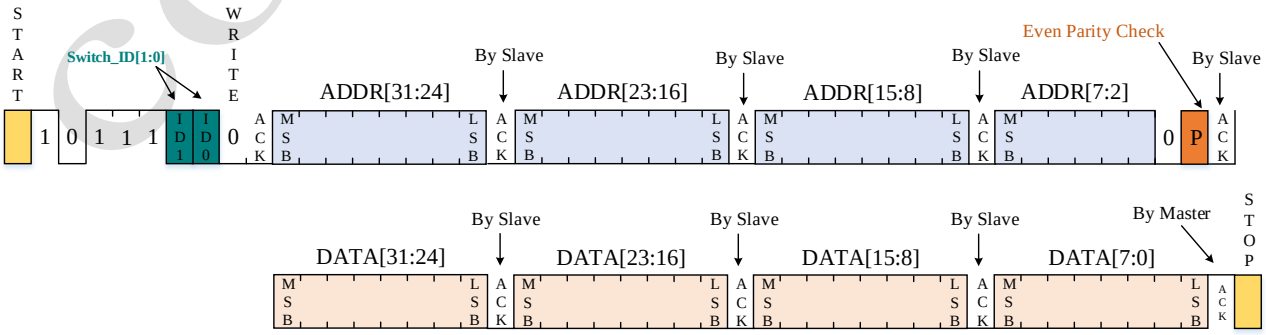

Figure 15. External CPU Write Register into YT9218MB By MSB I2C

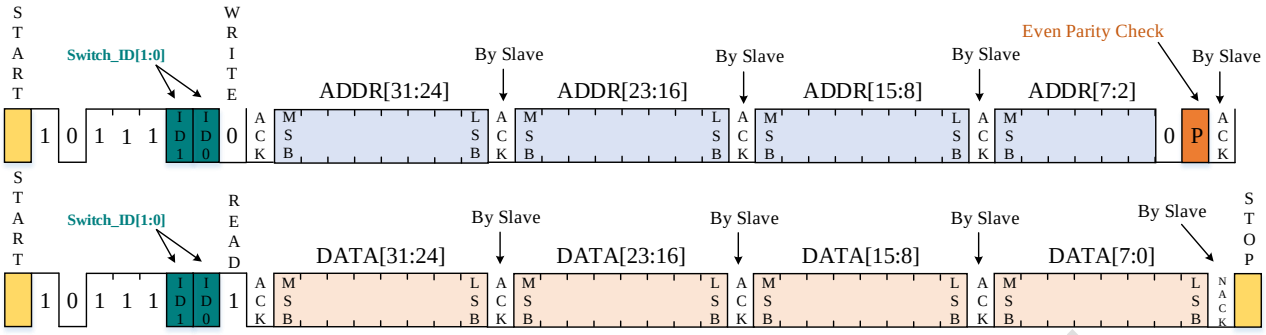

Figure 16. External CPU Read Register from YT9218MB By MSB I2C

5.5.1.3. Simply I2C

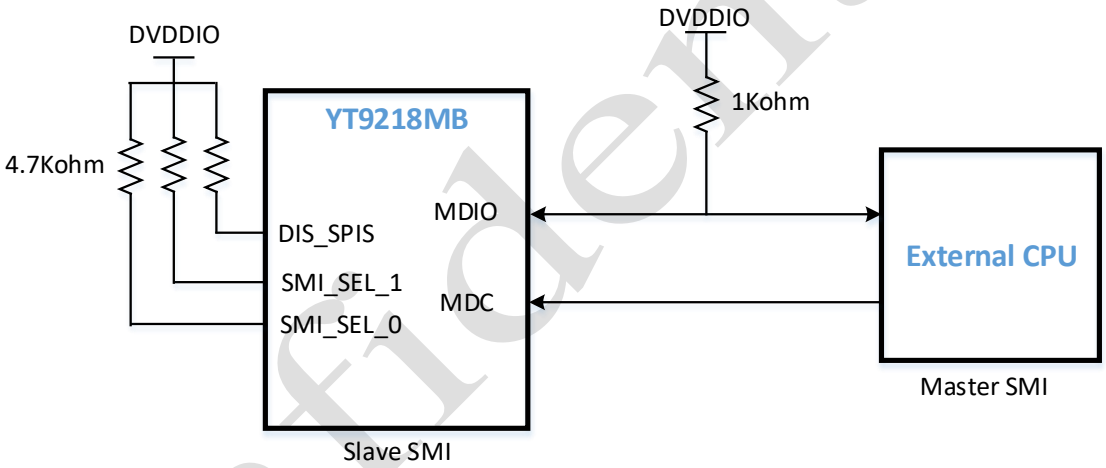

Figure 17. Simply I2C Interface Connection Example

The simply I2C format is shown in the following diagram.

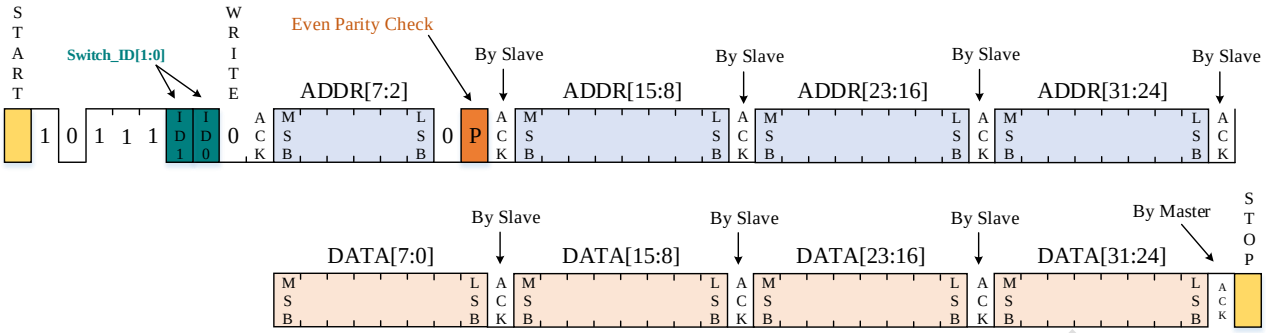

Figure 18. External CPU Write Register into YT9218MB By Simply I2C

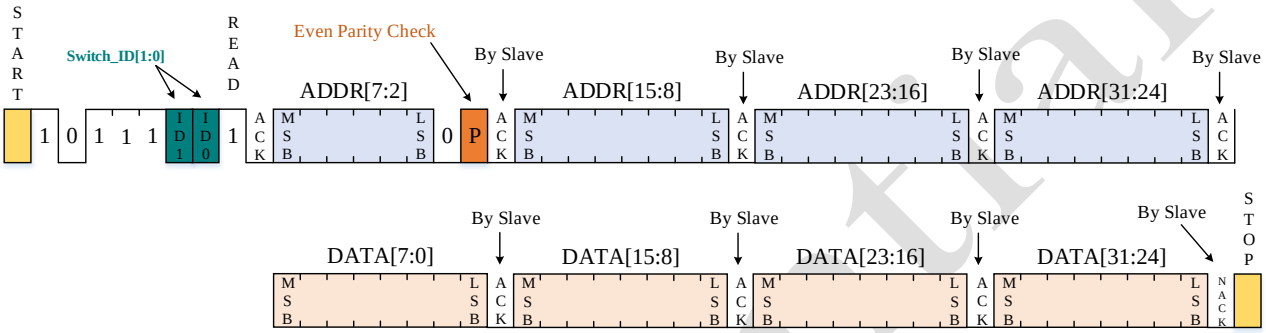

Figure 19. External CPU Read Register from YT9218MB By Simply I2C

5.5.2. Slave SMI Interface for External CPU

If the configuration pin DIS_SPIS should be high and SMI_SEL[1:0] should be 2b’10 upon power on or reset, the slave SMI (MDC/MDIO) is selected to access YT9218MB registers.

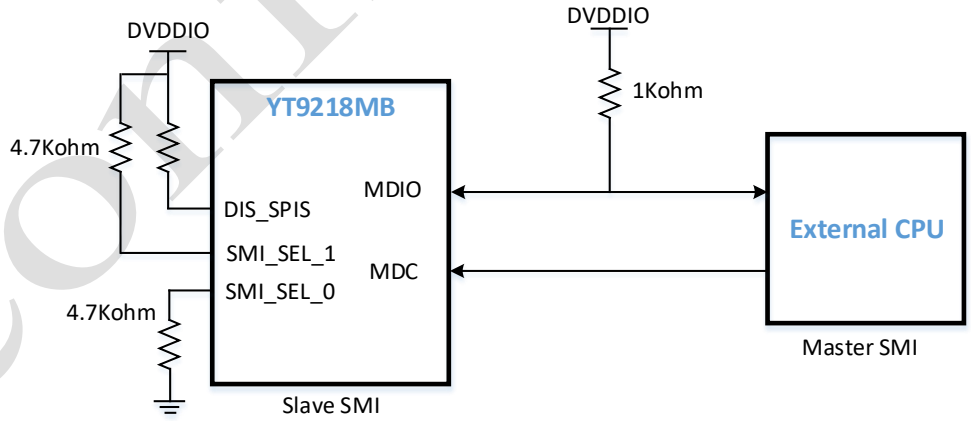

Figure 20. External CPU Read Register from YT9218MB By Slave SMI

5.5.3. Slave SPI Interface for External CPU

An SPI-Slave Management Interface can be enabled via configuration pins to access YT9218MB.

When the CPU writes data to the YT9218MB internal register via the SPI interface, the first 8-bits is OP code, and the write command OP code is 8h’02.

When the CPU reads data from the YT9218MB internal register via the SPI interface, the first 8-bits OP code is 8h’03.

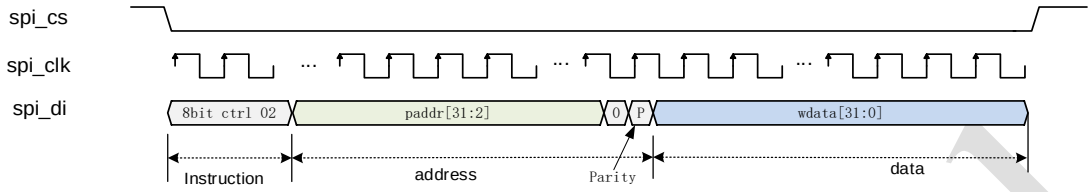

Figure 21. External CPU write command frame format

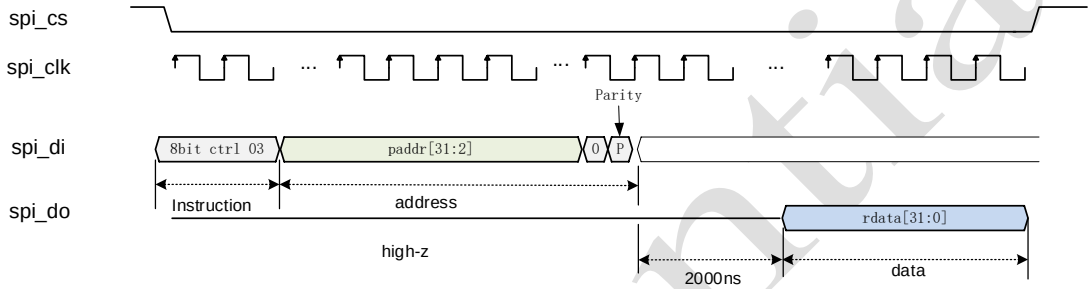

Figure 22. External CPU read command frame format

5.6. General Purpose Interface

The YT9218MB supports two extension interfaces. The two Extension GMAC (GMAC1 and GMAC2) both support SGMII MAC mode, SGMII PHY mode, 1000Base-X mode, 100Base-FX mode, 2500 Base-X mode via register configuration. GMAC2 also support RGMII mode, MII MAC mode, MII PHY mode, RMII MAC mode, or RMII PHY mode via register configuration.

5.6.1. Extension Ports SGMII MAC/PHY Mode (10/100/1000Mbps)

The two Extension GMAC (GMAC1 and GMAC2) both support SGMII MAC/PHY interfaces to an external CPU.

5.6.2. Extension Ports Fiber Mode (100FX/1000BX/2500BX)

The two Extension GMAC (GMAC1 and GMAC2) both support Fiber (100FX/ 1000BX/ 2500BX) interfaces to an external CPU or optical module.

5.6.3. Extension Ports RGMII Mode (10/100/1000Mbps)

The Extension GMAC2 of the YT9218MB support single-port RGMII interfaces to an external CPU.

5.6.4. Extension Ports MII MAC/PHY Mode Interface (10/100Mbps)

The Extension GMAC2 of the YT9218MB supports MII MAC/PHY mode interfaces to an external CPU.

5.6.5. Extension Ports RMII MAC/PHY Mode Interface (10/100Mbps)

The Extension GMAC2 of the YT9218MB supports RMII MAC/PHY mode interfaces to an external CPU.

6. Power Requirements

6.1. Power Sequence

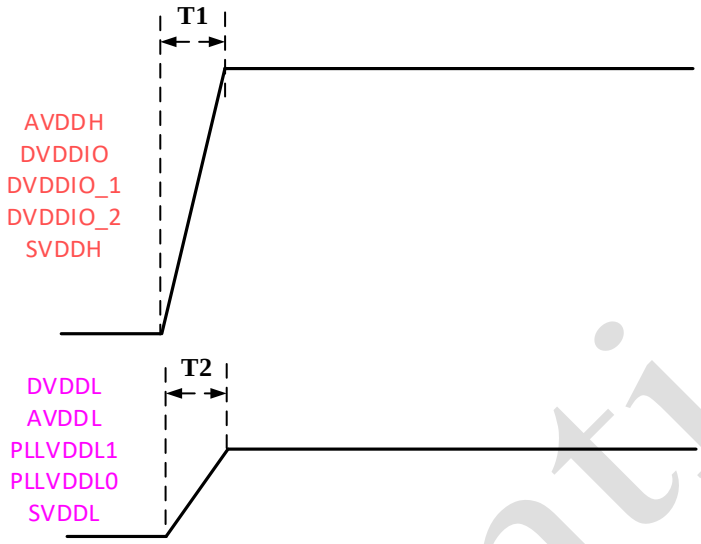

Figure 23. Power Sequence Diagram

Table 31. Power Sequence Timing Parameters

Symbol	Description	Min	Typ	Max	Units
T1	Rising time of AVDDH, DVDDIO, DVDDIO_1, DVDDIO_2, SVDDH.	0.5	-	-	ms
T2	Rising time of DVDDL, AVDDL, PLLVDDL0, PLLVDDL1, SVDDL.	0.5	-	-	ms

6.2. Power Consumption

Table 32. YT9218MB Power Consumption

	DVDDIO_1 (mA)	DVDDIO_2 (mA)	SVDDH (mA)	SVDDL (mA)	DVDDL (mA)	AVDDL (mA)	AVDDH (mA)	Power Consumption (mW)
Reset	0.17	0.41	0.11	0.56	8.67	4.65	31.77	123.08
sleep	0.33	0.42	0.11	0.53	77.04	26.03	37.76	246.59
link down	0.59	0.34	0.1	0.48	107.57	46.68	109.02	541.10
8*1G UTP link up	0.18	0.35	0.1	0.54	697.49	190.81	436.37	2464.26
8*1G UTP link and traffic	0.16	0.34	0.11	0.55	810.12	190.98	436.25	2593.55
8*UTP+2*1G RGMII link up	23.64	6.95	0.11	0.54	706.34	190.95	436.45	2574.11
8*1G UTP+2*1G RGMII link and traffic	31.13	23.16	0.11	0.55	823.73	191.15	428.68	2761.92
8*1G UTP + 2*2.5G SDS link up	0.33	0.34	50.91	89.07	721.69	191.14	436.58	2763.11

8*1G UTP + 2*2.5G SDS link and traffic	0.33	0.22	51.5	89.79	838.31	191.38	428.87	2874.44
8*1G UTP + 2*2.5G SDS link and traffic +led	63.7	60.47	51.81	89.88	838.96	191.64	429.27	3285.87
8*1G UTP + 2*1G SDS link up	0.33	0.44	50.33	76.67	707.57	191.12	436.7	2731.41
8*1G UTP + 2*1G SDS link and traffic	0.33	0.44	50.46	76.89	823.72	191.33	428.51	2838.88

Test Condition: TT IC with SVDDH/AVDDH/DVDDIO_1/DVDDIO_2 = 3.3V and DVDDL/AVDDL/PLLVDDL0/PLLVDDL1/SVDDL = 1.15V at room temperature. Port0~7 work as 1000BT, Port 8/9 work as 1G RGMII or 1G/2.5G SDS mode.

6.3. Power Ripple

The AVDDH/DVDDIO/DVDDIO_1/DVDDIO_2 supply noise should be under 100mV. The DVDDL noise should be under 80mV, and the AVDDL, PLLVDDL0, PLLVDDL1, and SVDDL noise should be under 50mV.

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 33. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	–	+125	℃
Storage Temperature	−45	+125	℃
DVDDIO, DVDDIO_1, DVDDIO_2, AVDDH, SVDDH Supply Referenced to GND and AGND	GND−0.3	+3.70	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1, SVDDL Supply Referenced to GND, AGND, and PLLGND	GND−0.3	+1.40	V
Digital Input Voltage	GND−0.3	VDDIO+0.3	V

7.2. Recommended Operating Range

Table 34. Recommended Operating Range

Parameter		Min	TYP	Max	Units
Ambient Operating Temperature (Ta)		0	–	70	℃
AVDDH, SVDDH Supply Voltage Range		3.135	3.3	3.63	V
DVDDIO Supply Voltage Range	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
DVDDIO_1 Supply Voltage Range (DVDDIO_1: Extension Port 1 Supports 1.8V,2.5V,3.3V)	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
	1.8V	1.62	1.8	1.98	V
DVDDIO_2 Supply Voltage Range (DVDDIO_2: Extension Port 2 Supports 1.8V,2.5V,3.3V)	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
	1.8V	1.62	1.8	1.98	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1, SVDDL Supply Voltage Range		1.045	1.1	1.32	V

7.3. DC Characteristics

Table 35. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
Voh (3.3V)	Minimum High Level Output Voltage	2.4	-	3.63	V
Vol (3.3V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Vih (3.3V)	Minimum High Level Input Voltage	2	-	-	V
Vil (3.3V)	Maximum Low Level Input Voltage	-	-	0.8	V
Voh (2.5V)	Minimum High Level Output Voltage	2	-	2.8	V
Vol (2.5V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Vih (2.5V)	Minimum High Level Input Voltage	1.7	-	-	V
Vil (2.5V)	Maximum Low Level Input Voltage	-	-	0.7	V
Voh (1.8V)	Minimum High Level Output Voltage	1.62	-	2.1	V
Vol (1.8V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Vih (1.8V)	Minimum High Level Input Voltage	1.2	-	-	V
Vil (1.8V)	Maximum Low Level Input Voltage	-	-	0.5	V

7.4. AC Characteristics

7.4.1. Reset Timing

Table 36. Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Units
t1	The duration from all powers steady to nRESET de-asserted, or the nRESET assertion time after power up.	10	-	-	ms

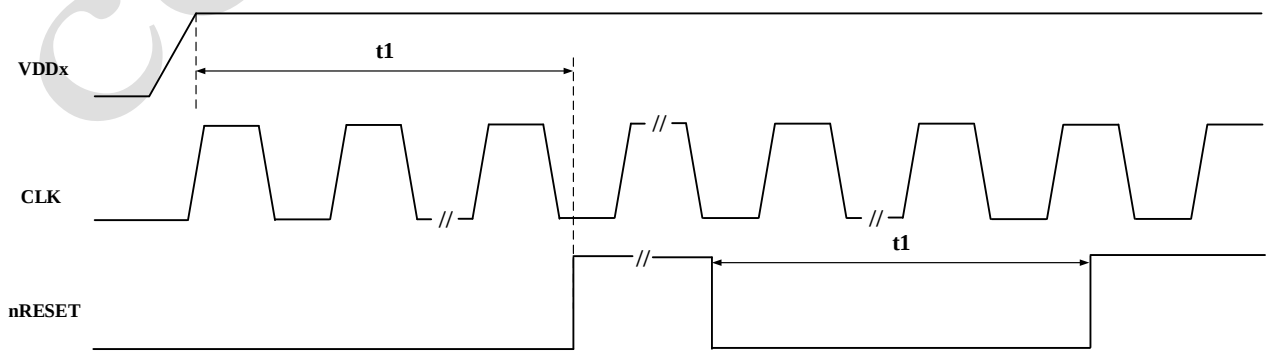

Figure 24. Reset Timing Diagram

7.4.2. SPI Flash Interface Timing Characteristics

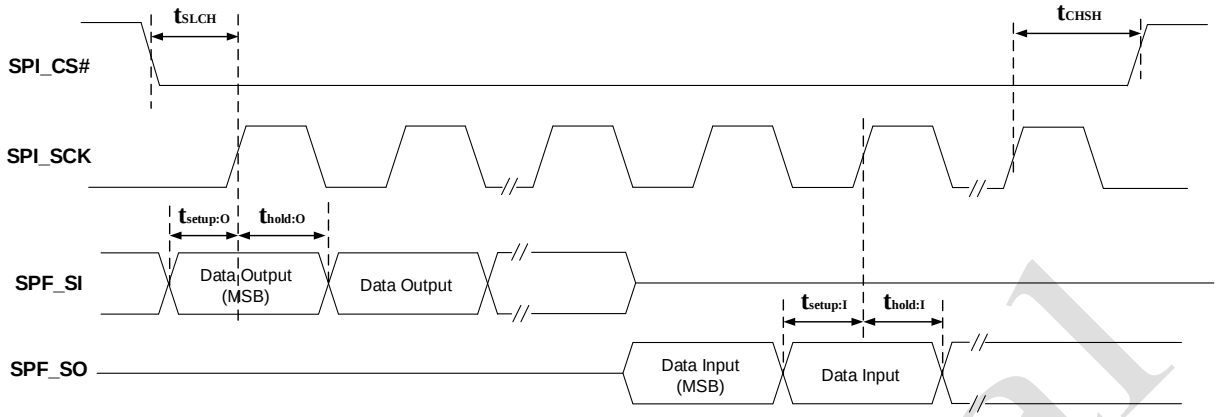

Figure 25. SPI Flash Interface Timing

Table 37. SPI Flash Interface Timing Parameter

Symbol	Description	Type	Min	Typical	Max	Units
fSPI_SCK	Clock Frequency of the SPI_SCK	O	–	31.25		Mhz
Duty	Duty Cycle of the SPI_SCK	O	45	50	55	%
tSLCH	CS#Active Setup Time	O	6	–	–	ns
tCHSH	CS#Active Hold Time	O	6	–	–	ns
tsetupO	Data Output Setup Time	O	5	–	–	ns
tholdO	Data Output Hold Time	O	6	–	–	ns
tsetupI	Data Input Setup Time	I	2	–	–	ns
tholdI	Data Input Hold Time	I	0	–	–	ns

7.4.3. Master I2C Timing Characteristics

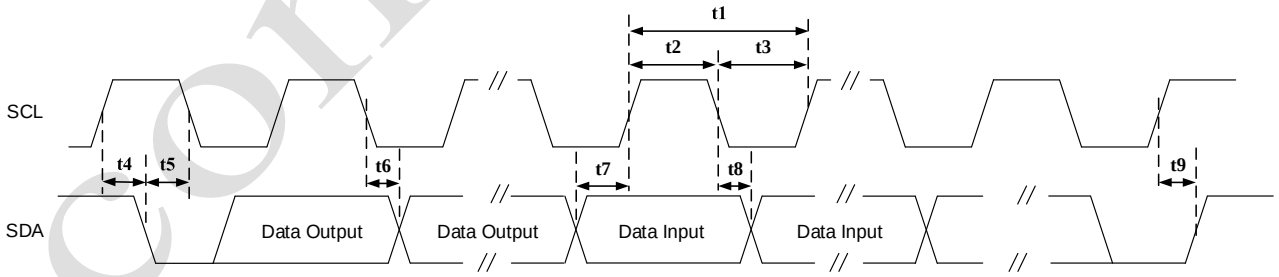

Figure 26. Master I2C Timing

Table 38. Master I2C Timing Parameter

Symbol	Description	Min	Typ	Max	Units
Freq	Clock Frequency of SCL	–	100	800	kHz
t1	SCL Clock Period	1	10	–	us
t2	SCL High Time	0.3*t1	0.5*t1	–	us

t3	SCL Low Time	0.3*t1	0.5*t1	–	us
t4	START Setup Time	0.25*t1	–	–	us
t5	START Hold Time	0.25*t1	–	–	us
t6	SCL Low to Data Output Valid	0.1*t1	–	0.2*t1	us
t7	Data Input Setup Time	0	–	–	ns
t8	Data Input Hold Time	0	–	–	ns
t9	Stop Setup Time	0.3*t1	–	–	us

7.4.4. Master SMI Timing Characteristics

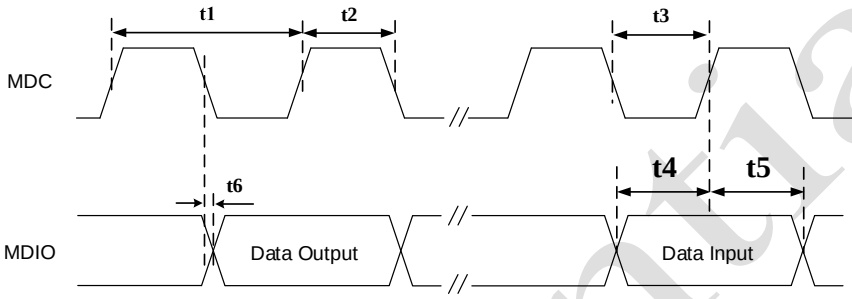

Figure 27. Master SMI Timing

Table 39. Master SMI Timing Parameter

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	100*	–	–	ns
t2	MDC High Time	35	–	–	ns
t3	MDC Low Time	35	–	–	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	–	–	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	–	–	ns
t6	MDIO Valid from MDC rising edge (Data Output)	5	–	50*	ns

Note*: The MDIO pin type is Open Drain when work as Master SMI interface. Therefore, the minimum value of t1 and the maximum value of t6 depend on the value of the pull-up resistor on MDIO signal. Parameters in Table 39 is the result under the condition of pull-up 1Kohm resistor.

7.4.5. Master I2C for EEPROM Auto-load Timing Characteristics

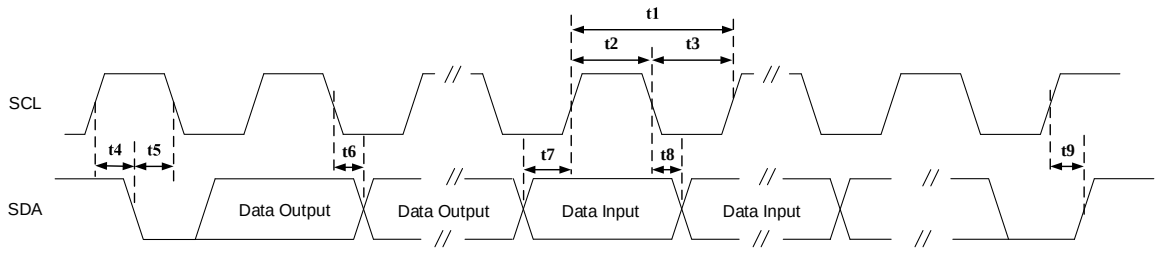

Figure 28. Master I2C for EEPROM Auto-load Timing

Table 40. Master I2C for EEPROM Auto-load Timing Parameter

Symbol	Description	Min	Typ	Max	Units
Tfreq	SCL Clock Frequency	–	100	800	kHz
t1	SCL Clock Period	1.25	10	–	us
t2	SCL High Time	0.3*t1	0.5*t1	–	us
t3	SCL Low Time	0.3*t1	0.5*t1	–	us
t4	START Setup Time	0.25*t1	–	–	us
t5	START Hold Time	0.25*t1	–	–	us
t6	SCL Low to Data Output Valid	0.1*t1	–	0.2*t1	us
t7	Data Input Setup Time	0	–	–	ns
t8	Data Input Hold Time	80	–	–	ns
t9	Stop Setup Time	0.3*t1	–	–	us

7.4.6. Slave I2C Timing Characteristics

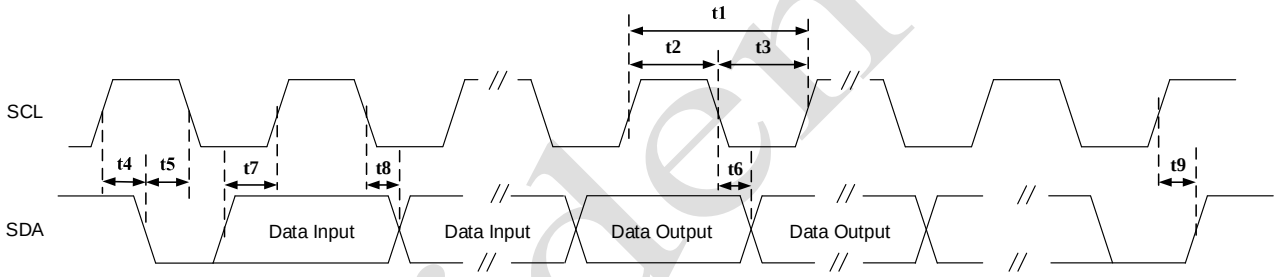

Figure 29. Slave I2C Timing

Table 41. Slave I2C Timing Parameter

Symbol	Description	Min	Typ	Max	Units
Tfreq	SCL Clock Frequency	–	–	400	kHz
t1	SCL Clock Period	2.5	–	–	us
t2	SCL High Time	0.8		–	us
t3	SCL Low Time	0.8		–	us
t4	START Setup Time	0.3	–	–	us
t5	START Hold Time	0.3	–	–	us
t6	SCL Low to Data Output Valid	0.1	–	0.3	us
t7	Data Input Setup Time	0	–	–	ns
t8	Data Input Hold Time	200	–	–	ns
t9	Stop Setup Time	0.3	–	–	us

7.4.7. Slave SMI Timing Characteristics

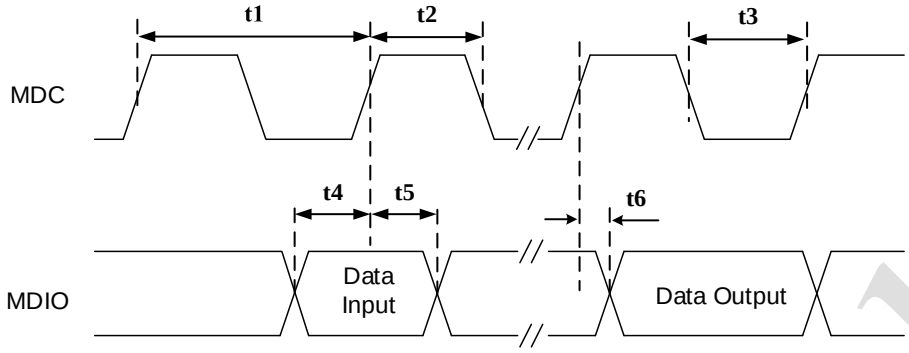

Figure 30. Slave SMI Timing

Table 42. Slave SMI Timing Parameter

Symbol	Description	Min	Typ	Max	Units
t1	MDC Clock Period	100*	–	–	ns
t2	MDC High Time	35	–	–	ns
t3	MDC Low Time	35	–	–	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	–	–	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	–	–	ns
t6	MDIO Valid from MDC rising edge (Data Output)	5	–	40	ns

Note*: The MDIO pin type is Open Drain when work as Master SMI interface. Therefore, the minimum value of t1 and the maximum value of t6 depend on the value of the pull-up resistor on MDIO signal. Parameters in Table 39 is the result under the condition of pull-up 1Kohm resistor.

7.4.8. Slave SPI Timing Characteristics

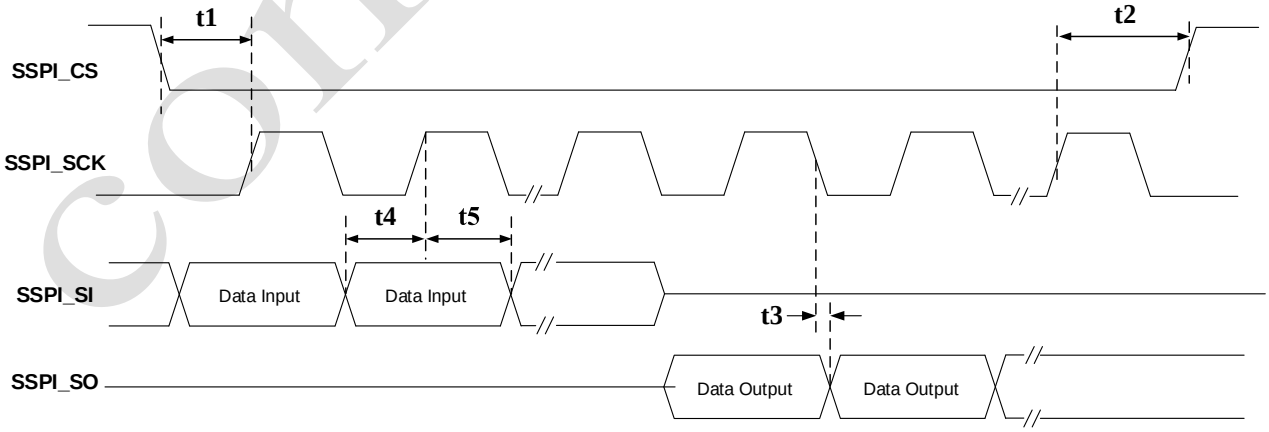

Figure 31. Slave SPI Interface Timing

Table 43. Slave SPI Interface Timing Parameter

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Clock Frequency of SPI_SCK	–	–	6	MHz
t1	SSPI_CS# Active Setup Time relative to SPI_SCK	50			ns
t2	SSPI_CS# Not Active Hold Time relative to SPI_SCK	50			ns
t3	SSPI_SO Output Valid Time	0	–	80	ns
t4	SSPI_SI Input Setup Time	40	–	–	ns
t5	SSPI_SI Input Hold Time	40	–	–	ns

7.4.9. RGMII Timing w/o delay

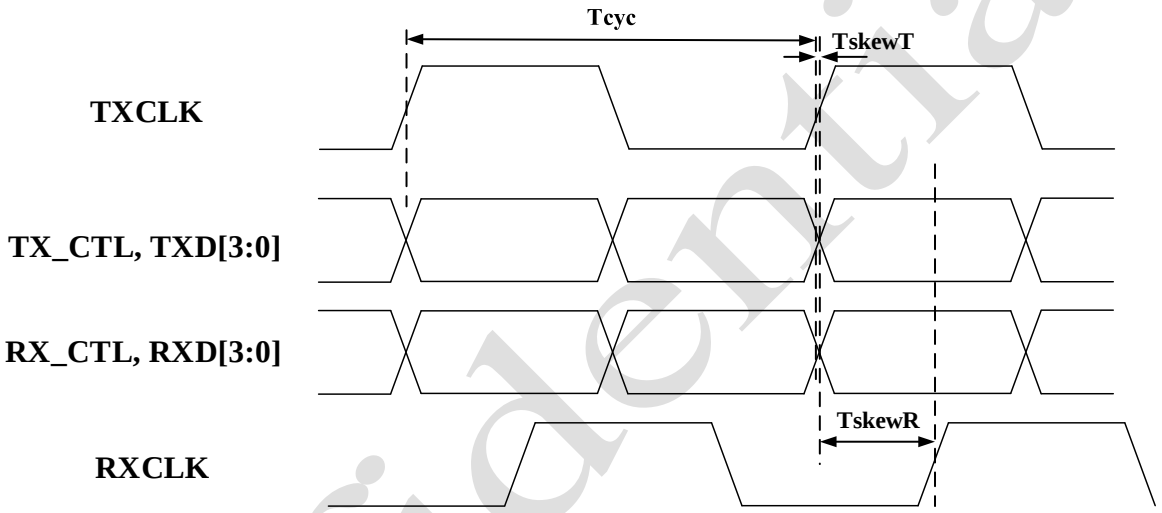

Figure 32. RGMII Timing w/o delay

Table 44. RGMII Timing w/o delay

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to clock output skew (at Transmitter)	−500	0	500	ps
TskewR	Data to clock output skew (at Receiver)	1	1.5	2.0	ns
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100T	40	50	60	%

7.4.10. RGMII Timing with internal delay

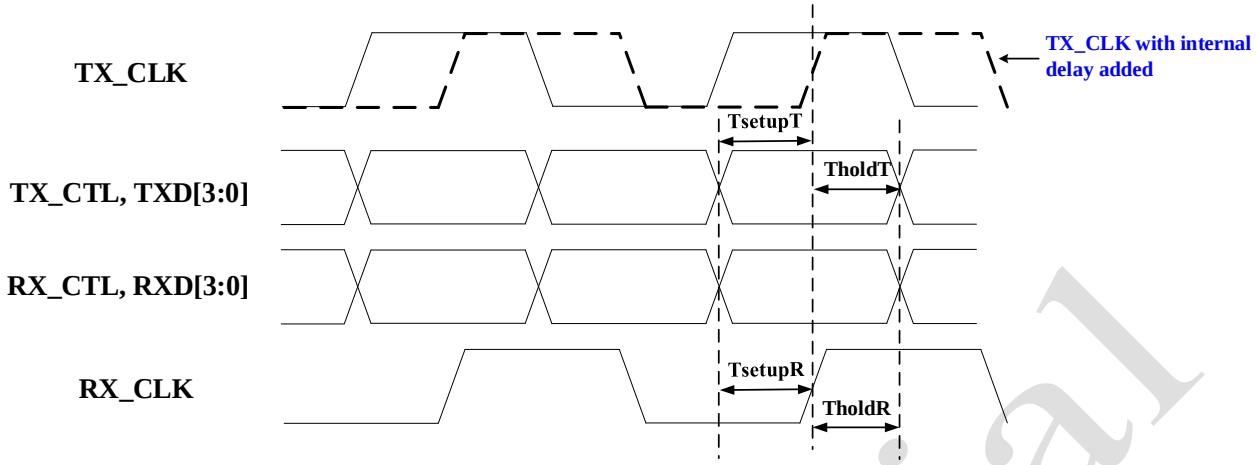

Figure 33. RGMII Timing with internal delay

Table 45. RGMII Timing with internal delay

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock output Setup Time (at Transmitter integrated delay)	1.0	2.0	-	ns
TholdT	Clock to Data output Hold Time (at Transmitter integrated delay)	1.0	2.0	-	ns
TsetupR	Data to Clock input Setup Time (at Receiver integrated delay)	1.0	2.0	-	ns
TholdR	Data to Clock input Hold Time (at Receiver integrated delay)	1.0	2.0	-	ns

7.4.11. 2500Base-X Characteristics

Table 46. 2500Base-X Differential Transmitter Characteristics

Parameter		SYM	Min	Typ	Max	Units	Notes
Unit Interval		UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask		T_X1	–	–	0.2	UI	–
Eye Mask		T_X2	–	–	0.4	UI	–
Eye Mask		T_Y1	150	–	–	mV	–
Eye Mask		T_Y2	–	–	500	mV	–
Output Differential Voltage		$V_{TX-DIFF_{P-P}}$	350	500	900	mV	–
Output Jitter	TJ	$T_{TX-Jitter}$	–	–	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 – $T_{TX-EYE-MIN}$ = 0.30UI
	DJ		–	–	0.165	UI	–
Minimum TX Eye Width		T_{TX-EYE}	0.7	–	–	UI	–
Output Rise Time		$T_{TX-Rise}$	0.125	–	–	UI	20%–80%
Output Fall Time		$T_{TX-Fall}$	0.125	–	–	UI	20%–80%
Output Differential Impendence		R_{TX}	80	100	120	ohm	–
AC Coupling Capacitor		C_{TX}	80	100	200	nF	–
Transmit Length in PCB		L_{TX}	–	–	15(*Note1)	inch	–

Note 1: If multiple SerDes mode is used in system, the shortest trace allowed should be used on board;

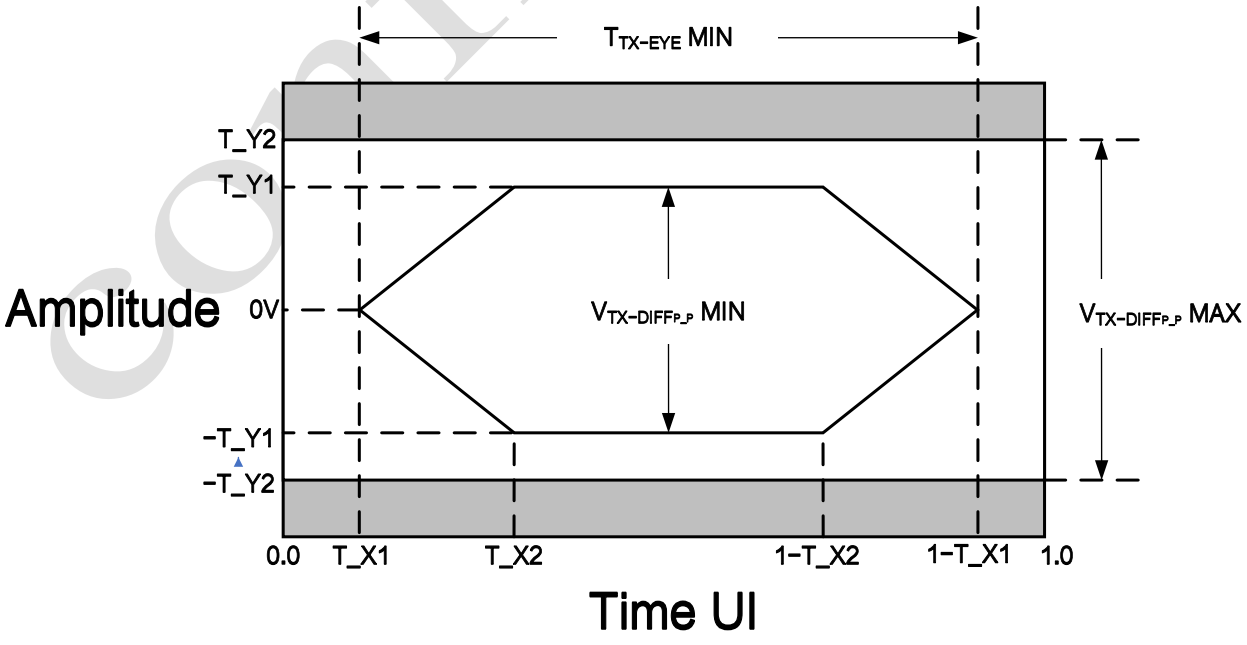

Figure 34. 2500Base-X Differential Transmitter Eye Diagram

Table 47. 2500Base-X Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask	R_X1	–	–	0.275	UI	–
Eye Mask	R_Y1	100	–	–	mV	–
Eye Mask	R_Y2	–	–	550	mV	–
Input Differential Voltage	$V_{RX-DIFF_{P-P}}$	200	–	1100	mV	–
Minimum RX Eye Width	T_{RX-EYE}	0.4	–	–	UI	–
Input Jitter Tolerance	$T_{RX-Jitter}$	–	–	0.6	UI	$T_{RX-JITTER-MAX}$ = 1 – $T_{RX-EYE-MIN}$ = 0.6UI
Input Differential Impendence	R_{RX}	80	100	120	ohm	–

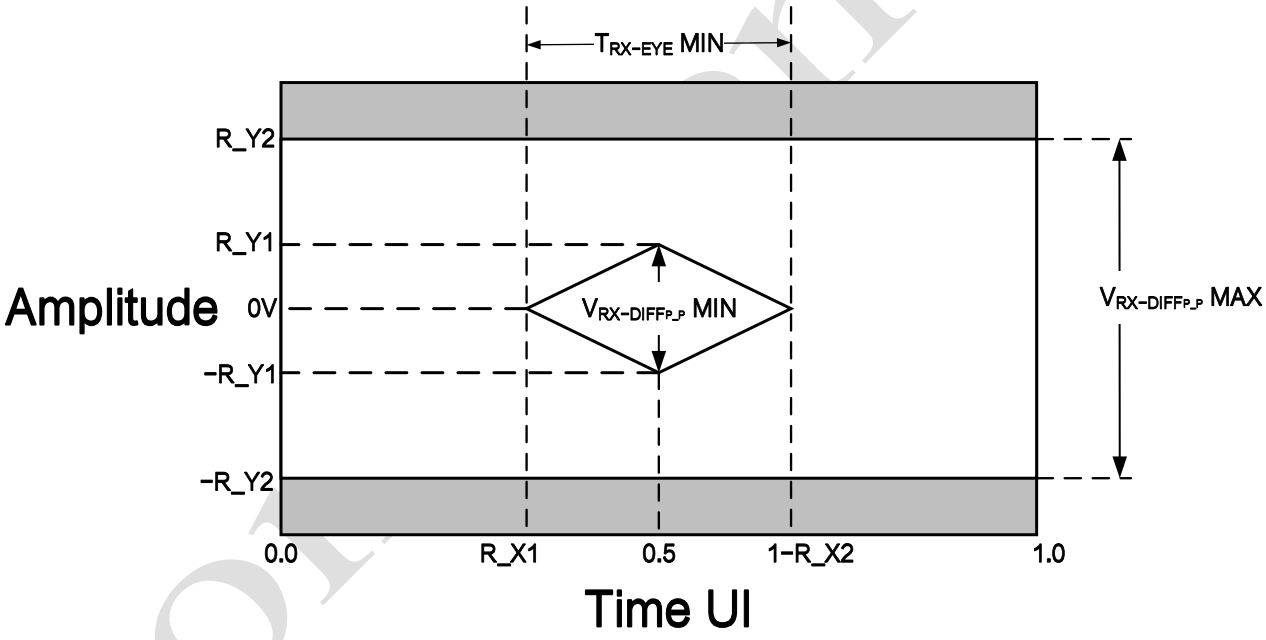

Figure 35. 2500Base-X Differential Receiver Eye Diagram

7.4.12. SGMII Characteristics

Table 48. SGMII Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	T_X1	–	–	0.15	UI	–
Eye Mask	T_X2	–	–	0.4	UI	–
Eye Mask	T_Y1	150	–	–	mv	–
Eye Mask	T_Y2	–	–	500	mv	–
Output Differential Voltage	$V_{TX-DIFF_{P-P}}$	350	500	900	mv	–
Minimum TX Eye Width	T_{TX-EYE}	0.7	–	–	UI	–
Output Jitter	$T_{TX-Jitter}$	–	–	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 – $T_{TX-EYE-MIN}$ = 0.30UI
Data dependent Jitter		–	70	–	ps	–
Output Rise Time	$T_{TX-Rise}$	100	–	200	ps	20%–80%
Output Fall Time	$T_{TX-Fall}$	100	–	200	ps	20%–80%
Output Differential Impendence	R_{TX}	80	100	120	ohm	–
AC Coupling Capacitor	C_{TX}	80	100	200	nF	–
Transmit Length in PCB	L_{TX}	–	–	30(*Note1)	inch	–

Note 1: If multiple SerDes mode is used in system, the shortest trace allowed should be used on board;

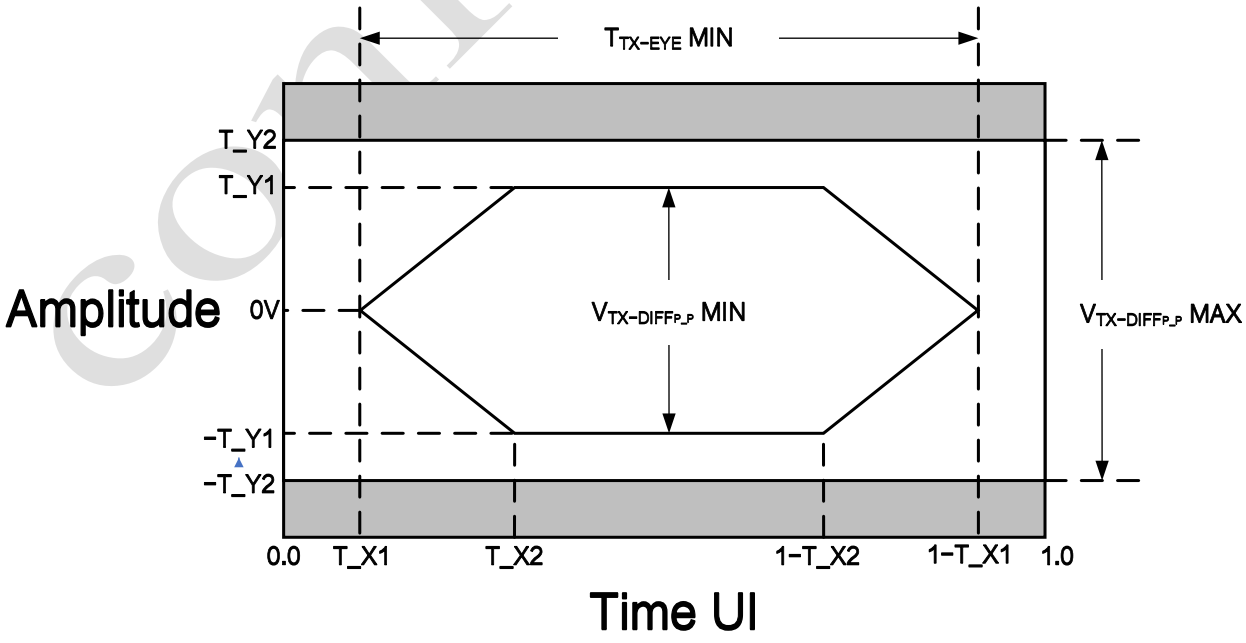

Figure 36. SGMII Differential Transmitter Eye Diagram

Table 49. SGMII Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	R_X1	–	–	0.275	UI	–
Eye Mask	R_Y1	100	–	–	mV	–
Eye Mask	R_Y2	–	–	550	mV	–
Input Differential Voltage	$V_{RX-DIFF_{P-P}}$	200	–	1100	mV	–
Minimum RX Eye Width	T_{RX-EYE}	0.4	–	–	UI	–
Input Jitter Tolerance	$T_{RX-Jitter}$	–	–	0.6	UI	$T_{RX-JITTER-MAX}$ = 1 – $T_{RX-EYE-MIN}$ = 0.6UI
Input Differential Impendence	R_{RX}	80	100	120	ohm	–

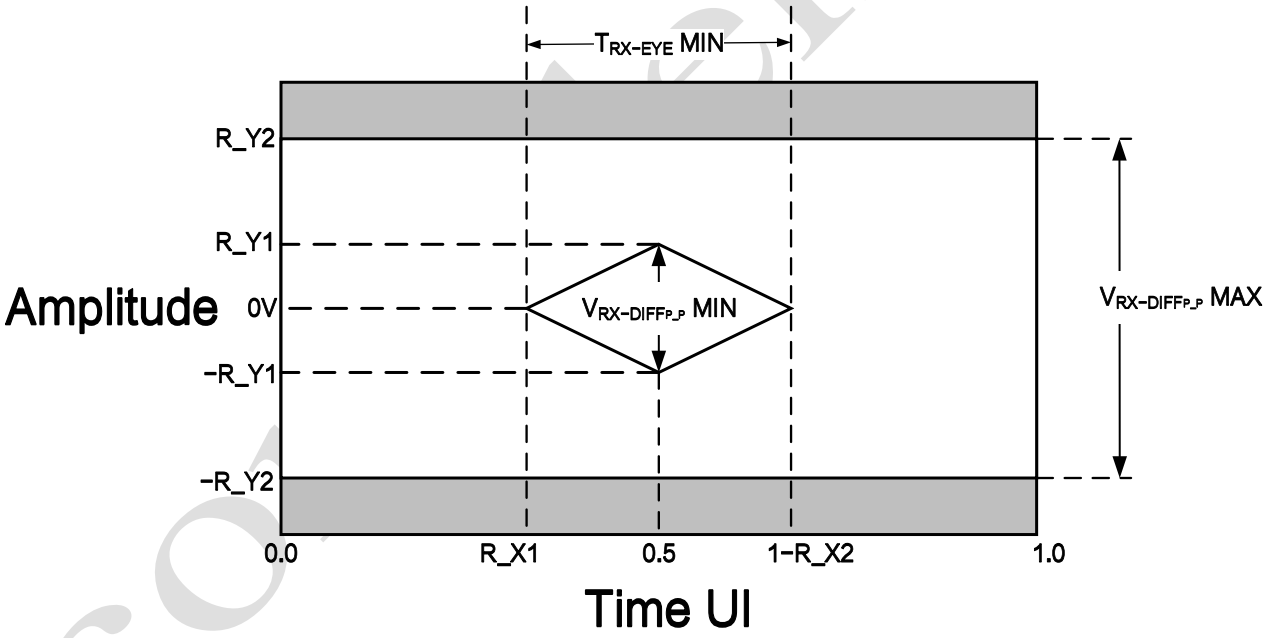

Figure 37. SGMII Differential Receiver Eye Diagram

7.4.13. 1000Base-X Characteristics

Table 50. 1000Base-X Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	T_X1	–	–	0.15	UI	–
Eye Mask	T_X2	–	–	0.4	UI	–
Eye Mask	T_Y1	150	–	–	mv	–
Eye Mask	T_Y2	–	–	500	mv	–
Output Differential Voltage	$V_{TX-DIFF_{P-P}}$	350	500	900	mv	–
Minimum TX Eye Width	T_{TX-EYE}	0.7	–	–	UI	–
Output Jitter	$T_{TX-Jitter}$	–	–	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 – $T_{TX-EYE-MIN}$ = 0.30UI
Output Rise Time	$T_{TX-Rise}$	0.075	–	–	UI	20%–80%
Output Fall Time	$T_{TX-Fall}$	0.075	–	–	UI	20%–80%
Output Impendence	R_{TX}	80	100	120	ohm	–
AC Coupling Capacitor	C_{TX}	80	100	200	nF	–
Transmit Length in PCB	L_{TX}	–	–	30(*Note1)	inch	–

Note 1: If multiple SerDes mode is used in system, the shortest trace allowed should be used on board;

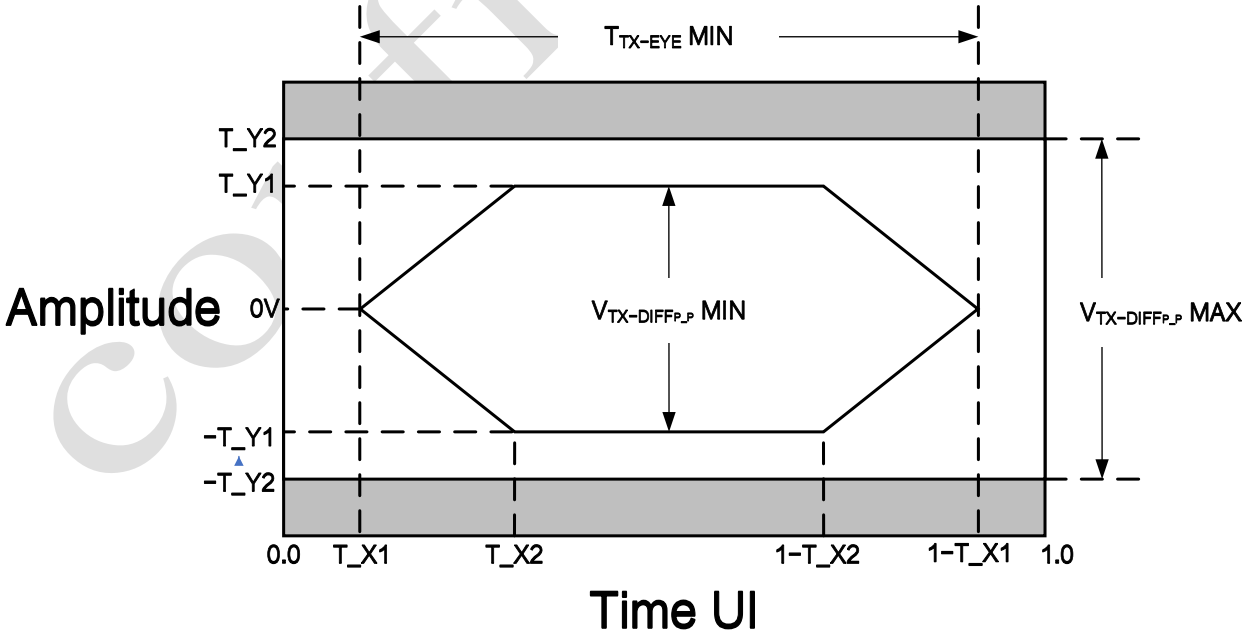

Figure 38. 1000Base-X Differential Transmitter Eye Diagram

Table 51. 1000Base-X Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	R_X1	–	–	0.275	UI	–
Eye Mask	R_Y1	100	–	–	mV	–
Eye Mask	R_Y2	–	–	550	mV	–
Input Differential Voltage	$V_{RX-DIFF_{P-P}}$	200	–	1100	mV	–
Minimum RX Eye Width	T_{RX-EYE}	0.4	–	–	UI	–
Input Jitter Tolerance	$T_{RX-Jitter}$	–	–	0.6	UI	$T_{RX-JITTER-MAX}$ = 1 – $T_{RX-EYE-MIN}$ = 0.6UI
Input Differential Impendence	R_{RX}	80	100	120	ohm	–

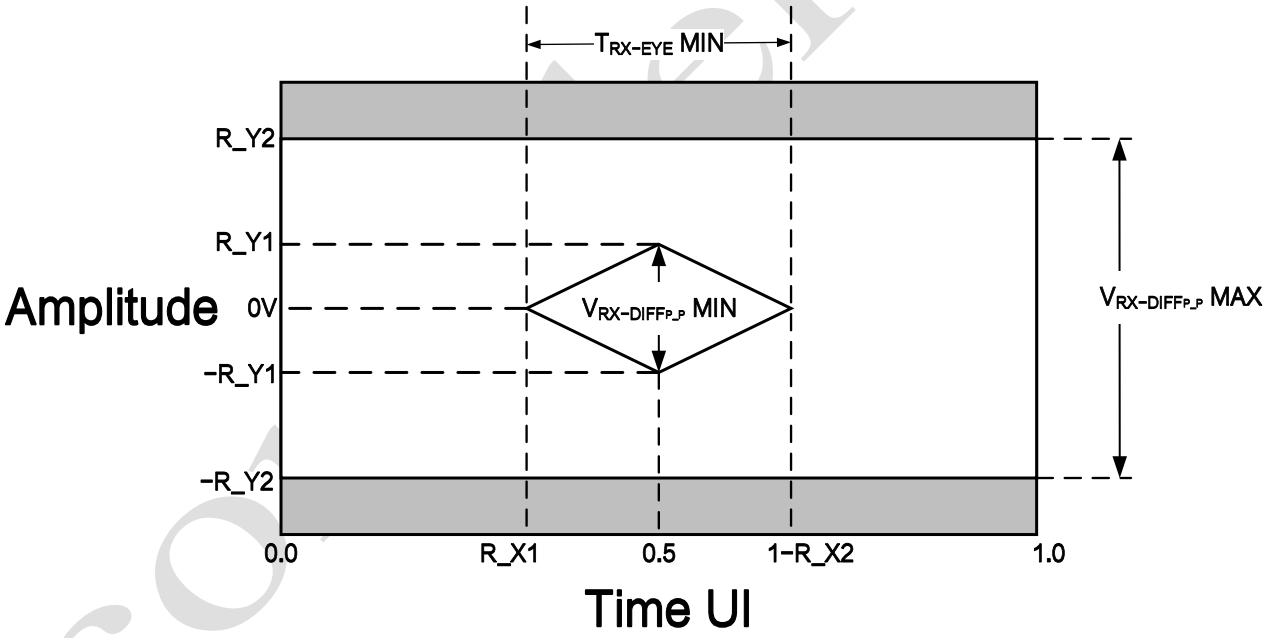

Figure 39. 1000Base-X Differential Receiver Eye Diagram

7.4.14. 100Base-FX Characteristics

Table 52. 100Base-FX Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	7.9976	8	8.0024	ns	8ns ± 300ppm
Eye Mask	T_X1	–	–	0.15	UI	–
Eye Mask	T_X2	–	–	0.4	UI	–
Eye Mask	T_Y1	150	–	–	mv	–
Eye Mask	T_Y2	–	–	500	mv	–
Output Differential Voltage	$V_{TX-DIFF_{P-P}}$	350	500	900	mv	–
Minimum TX Eye Width	T_{TX-EYE}	0.7	–	–	UI	–
Output Jitter	$T_{TX-Jitter}$	–	–	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 – $T_{TX-EYE-MIN}$ = 0.30UI
Output Rise Time	$T_{TX-Rise}$	0.075	–	–	UI	20%–80%
Output Fall Time	$T_{TX-Fall}$	0.075	–	–	UI	20%–80%
Output Impendence	R_{TX}	80	100	120	ohm	–
AC Coupling Capacitor	C_{TX}	80	100	200	nF	–
Transmit Length in PCB	L_{TX}	–	–	30(*Note1)	inch	–

Note 1: If multiple SerDes mode is used in system, the shortest trace allowed should be used on board;

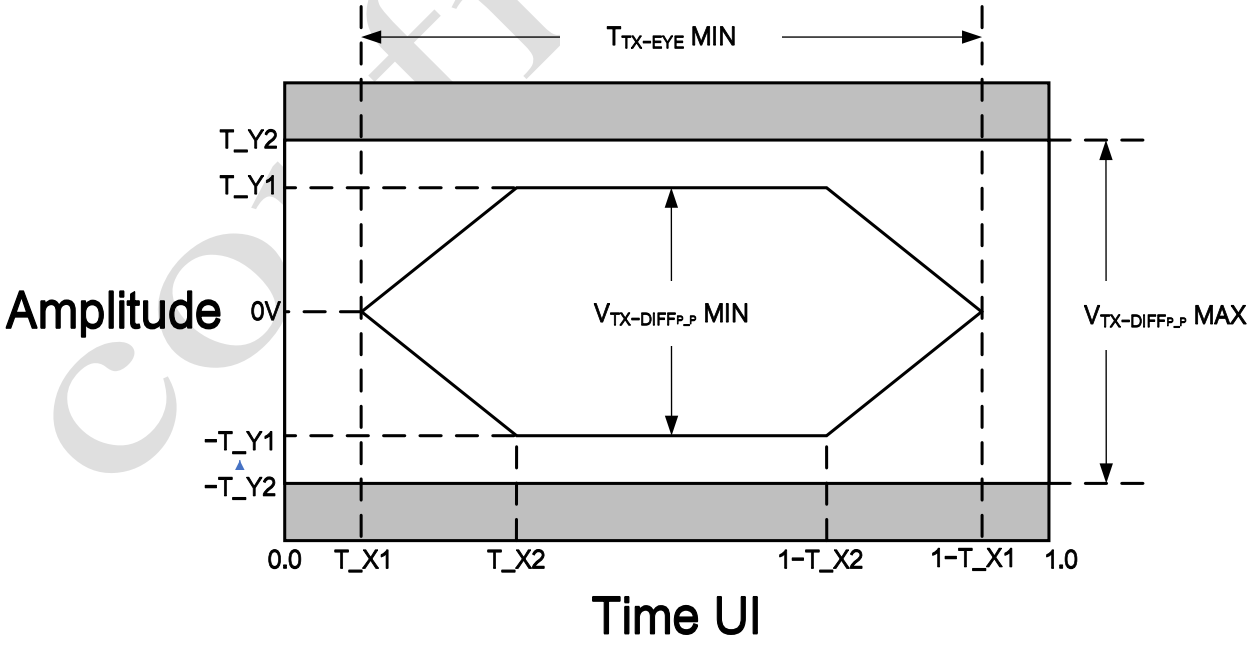

Figure 40. 100Base-FX Differential Transmitter Eye Diagram

Table 53. 100Base-FX Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Units	Notes
Unit Interval	UI	7.9976	8	8.0024	ns	8ns ± 300ppm
Eye Mask	R_X1	–	–	0.275	UI	–
Eye Mask	R_Y1	100	–	–	mV	–
Eye Mask	R_Y2	–	–	550	mV	–
Input Differential Voltage	$V_{RX-DIFF_{P-P}}$	200	–	1100	mV	–
Minimum RX Eye Width	T_{RX-EYE}	0.4	–	–	UI	–
Input Jitter Tolerance	$T_{RX-Jitter}$	–	–	0.6	UI	$T_{RX-JITTER-MAX}$ = 1 – $T_{RX-EYE-MIN}$ = 0.6UI
Input Differential Impendence	R_{RX}	80	100	120	ohm	–

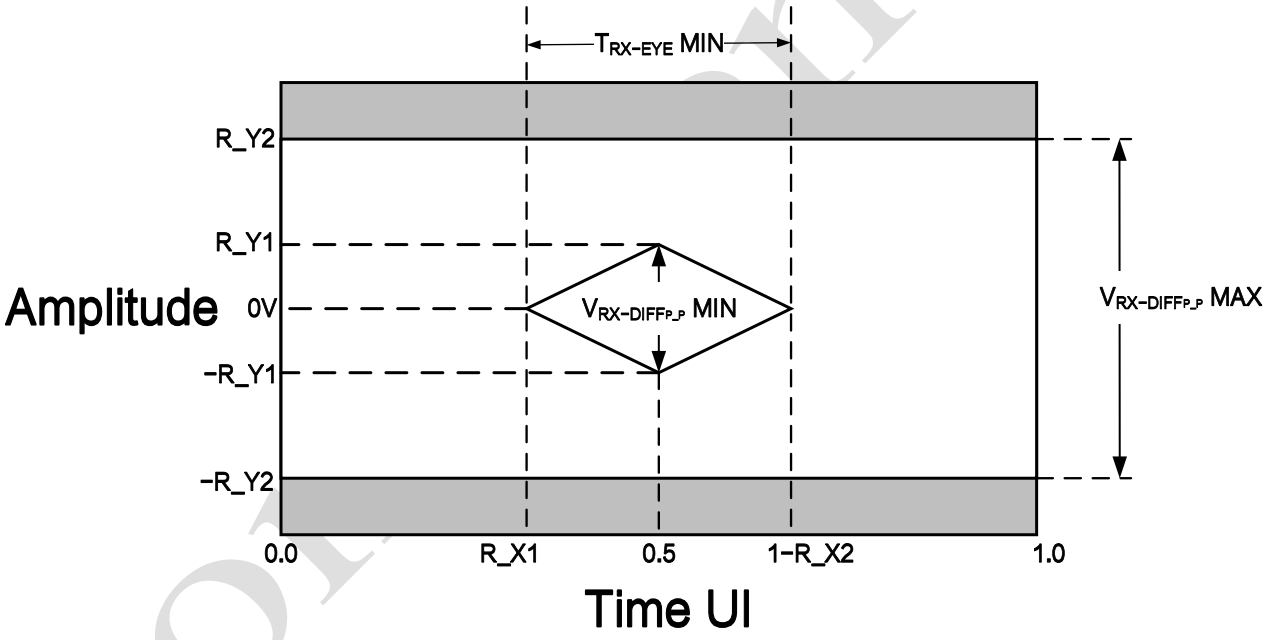

Figure 41. 100Base-FX Differential Receiver Eye Diagram

7.5. Crystal Requirement

Table 54. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Parallel Resonant Crystal Reference Frequency	–	25	–	MHz

Fref Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-50	-	50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.4	-	-	V
Vil	Crystal output low level	-	-	0.7	V

7.6. Oscillator/External Clock Requirement

Table 55. Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency	-	25	-	MHz
Frequency tolerance	-50	-	50	PPM
Duty Cycle	40	-	60	%
Vih	1.4	-	AVDDH+0.3	V
Vil	-	-	0.7	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns

8. Thermal Resistance

Table 56. Thermal Resistance

Symbol	Parameter	Condition	Typ	Units
θJA	Thermal resistance-junction to ambient **θJA=(TJ-TA)/P** P=Total power dissipation	JEDEC 3 in.x 4.5 in.4-layer PCB with no air flow TA=25℃	20.41	°C/W
		JEDEC 3 in.X 4.5 in.4-layer PCB with no air flow TA=85℃	18.39	°C/W
θJB	Thermal resistance-junction to board **θJB=(TJ-TB)/P** P=Total power dissipation	JEDEC with no air flow	9.31	°C/W
θJC	Thermal resistance-junction to case **θjc =(Tj-TC)/P** P=Total power dissipation	JEDEC with no air flow	8.74	°C/W
ψJt	Thermal resistance-junction to case-TOP **ψJt= (TJ-TT) /P** P = Total power dissipation	JEDEC with no air flow	0.29	°C/W
ψJb	Thermal resistance-junction to board **ψJb= (TJ-TB) /P** P = Total power dissipation	JEDEC with no air flow	9.88	°C/W

9. Mechanical Information

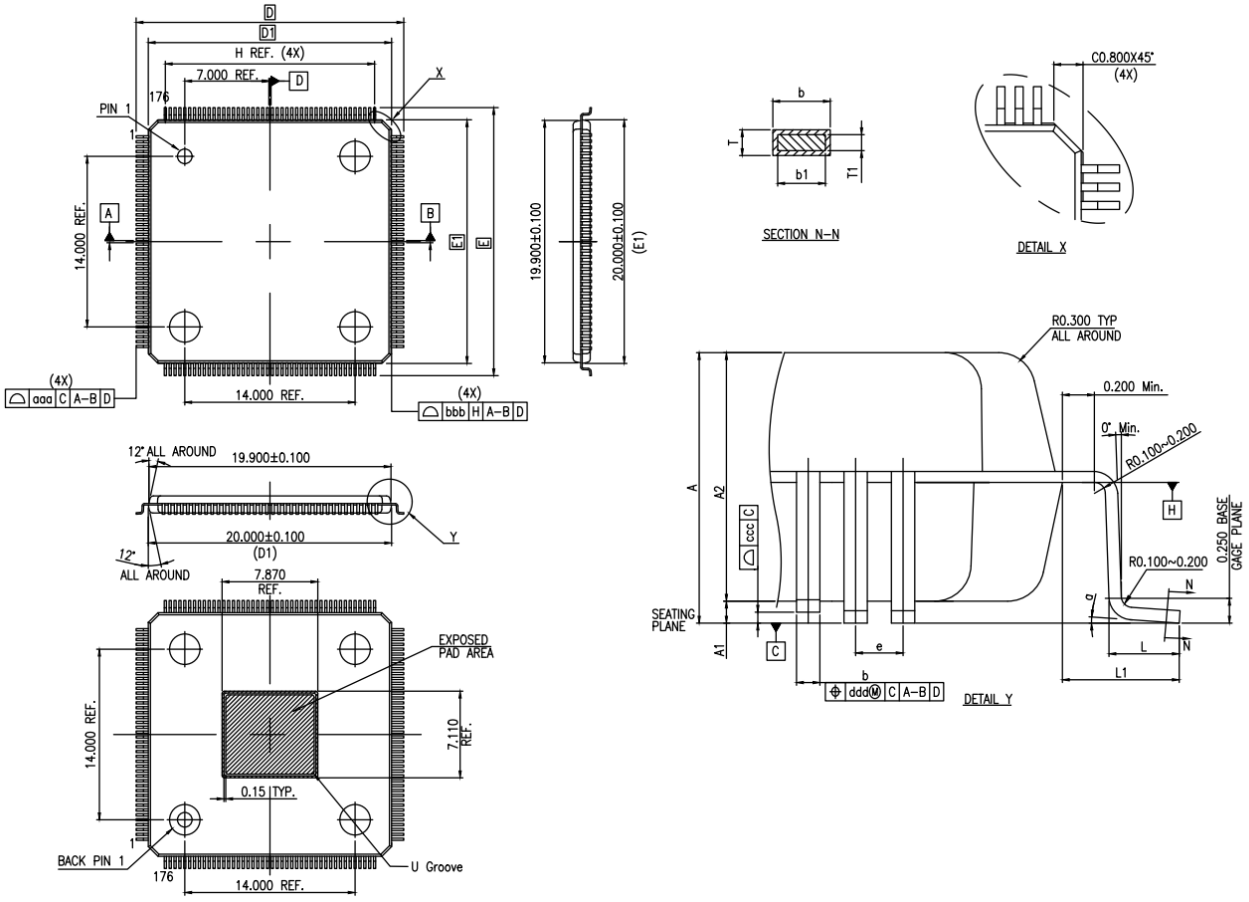

Table 57. Mechanical Dimensions in mm

DIMENSION LIST (FOOTPRINT: 2.00)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A1	$0.100^{+0.027}_{-0.050}$	STANDOFF
3	A2	1.400±0.050	PKG THICKNESS
4	D	22.000±0.200	LEAD TIP TO TIP
5	D1	20.000±0.100	PKG LENGTH
6	E	22.000±0.200	LEAD TIP TO TIP
7	E1	20.000±0.100	PKG WIDTH
8	L	0.600±0.150	FOOT LENGTH
9	L1	1.000 REF.	LEAD LENGTH
10	T	$0.150^{+0.050}_{-0.060}$	LEAD THICKNESS
11	T1	0.127±0.030	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.180±0.050	LEAD WIDTH
14	b1	0.160±0.030	LEAD BASE METAL WIDTH
15	e	0.400 BASE	LEAD PITCH
16	H (REF.)	(17.200)	CUM. LEAD PITCH
17	aaa	0.200	PROFILE OF LEAD TIPS
18	bbb	0.200	PROFILE OF MOLD SURFACE
19	ccc	0.080	FOOT COPLANARITY
20	ddd	0.080	FOOT POSITION

NOTES :

S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXCEPT EJECTION AND PIN 1 MARKING.		Ra0.8~2.0um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

10. Ordering Information

Motorcomm offers a RoHS package that is compliant with RoHS.

Table 58. Ordering Information

Part Number	Grade	Package	Pack	Status	Operation Temp
YT9218MB	Consumer	LQFP176-E	Tray 600EA	Mass Production	0 ~70 ° C