Product Specification

产品规格手册

QN24C02

2-K bits I²C-compatible Serial EEPROM

2080位I²C串行电擦除可编程只读存储器

Description

The QN24C02 is 2048 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. The QN24C02 is an I²C-compatible serial EEPROM device. The device is designed to operate in a supply voltage range of 1.7V ~ 5.5V, with a maximum of 1MHz transfer rate, over an operating temperature range of -40°C ~ +105°C. The device incorporates a Write Protection pin used for hardware Write Protection on the whole memory array. The device also offers a Software Write Protection feature for users to write protect the whole memory array.

The memory array is organized as 16 pages of 16 bytes each, totaling 256*8 bits. The device offers an additional 16-byte Identification Page for users to store sensitive application parameters. This page can be permanently locked in Read-only mode after the data is written into the Identification Page. The device also offers a separate memory block (in Read-only mode) containing a factory programmed 128-bit Unique ID and can be accessed to by sending a specific Read command.

The QN24C02 is delivered in lead-free green packages: DIP-8,SOP-8, MSOP-8, DFN-8 and SOT23-5.

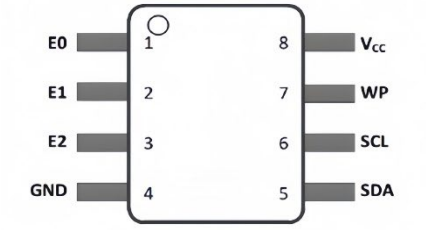
Features

- Supply Voltage Range: 1.7V ~ 5.5V
- 2-wire Serial Interface I²C Compatible
  - 400 kHz and High Speed 1MHz Transfer Rate Compatibility
- Byte and Page (up to 16 Bytes) Write Mode
  - Partial Page Write Allowed
- Self-timed Write Cycle (3ms Maximum)
- Additional 16-byte Write Lockable Page and 128-bit Unique ID
- Hardware and Software Write Protection on the Whole Memory Array
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High Reliability
  - Endurance: 2,000,000 Write Cycles
  - Data Retention: 200 Years

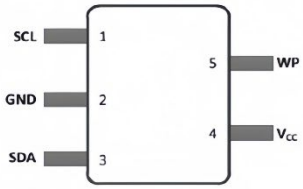
- ESD Protection (Human Body Model): 5000V

- Low Operating Current
  - Write Current: 0.5mA (Maximum)
  - Read Current: 0.5mA (Maximum)
  - Standby Current: 1μA (Maximum)
- Operating Temperature Range: -40°C ~ +105°C
- Green Packaging Options (RoHS Compliant, Pb/Halogen-free)
  - DIP-8/SOP-8/MSOP-8/TSSOP-8/DFN-8/SOT23-5

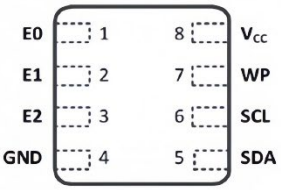
Pin Configuration



DIP-8/SOP-8/MSOP-8/TSSOP-8



SOT23-5



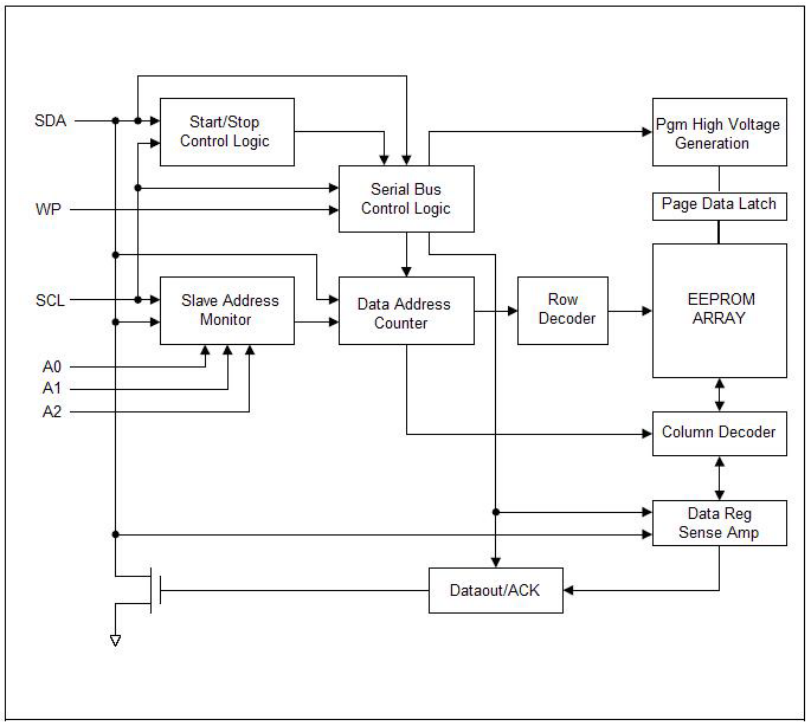
DFN-8 3*3

Pin Descriptions

Symbol	Type	Name and function
E0 E1 E2	Input	**Device Address Inputs**: The E0, E1, and E2 pins are device address inputs for compatibility with other 2-wire serial EEPROM devices. These pins can be directly connected to VCC or GND in any combination, allowing up to eight devices on a single bus system. If these pins are left floating, the E0, E1, and E2 pins will be internally pulled down to GND.
SDA	Input/Output	**Serial Data**: The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device.
SCL	Input	**Serial Clock**: The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL.
VCC	Power	**Device Power Supply**: The VCC pin is used to supply the source voltage to the device.Operations at invalid VCC voltages may produce spurious results and should not be attempted.

GND	Power	**Ground**: The ground reference for the power supply. GND should be connected to the system ground.
WP	Input	**Write Protection**: The WP pin is used to write protect the entire contents of the memory. When the WP pin is connected to Power Supply, the entire memory array becomes Write-protected, that is, the device becomes Read-only. When the WP pin is connected to GND, Write operations are enabled. If the pin is left floating, the WP pin will be internally pulled down to GND. When the WP pin is driven high, the device address byte and the word address bytes are acknowledged, data bytes are not acknowledged.

Block Diagram



PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B) SERIAL DATA LINE (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired-OR with other open-drain output devices.

(C) DEVICE / CHIP SELECT ADDRESSES (A2, A1, A0)

These are the chip select input signals for the serial EEPROM devices. Typically, these signals are hardwired to either VIH or VIL. If left unconnected, they are internally recognized as VIL. However, due to capacitive coupling that may appear in customer applications, FMD recommends always connecting the address pins to a known state. When using a pull-up or pull-down resistor, FMD recommends using 10kΩ or less.

(D) WRITE PROTECT (WP)

The QN24C02 devices have a WP pin to protect the whole EEPROM array from programming. Programming operations are allowed if WP pin is left un-connected or input to VIL. Conversely all programming functions are disabled if WP pin is connected to VIH or VCC. Read operations is not affected by the WP pin's input level. If left unconnected, it is internally recognized as VIL. However, due to capacitive coupling that may appear in customer applications, FMD recommends always connecting the WP pin to a known state. When using a pull-up or pulldown resistor, FMD recommends using 10kΩ or less.

MEMORY ORGANIZATION

The QN24C02 devices have 16 pages. Since each page has 16 bytes, random word addressing to QN24C02 will require 8 bits data word addresses.

DEVICE OPERATION

(A) SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when Serial clock SCL is at VIL. Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B) START CONDITION

With SCL ≥ VIH, a SDA transition from high to low is interpreted as a START condition. All valid commands must begin with a START condition.

(C) STOP CONDITION

With SCL ≥ VIH, a SDA transition from low to high is interpreted as a STOP condition. All valid read or write commands end with a STOP condition. The device goes into the STANDBY mode if it is after a read command. A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the selftimed internal

programming finish.

(D) ACKNOWLEDGE

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledges the data or address by outputting a "0" after receiving each word. The ACKNOWLEDGE signal occurs on the 9th serial clock after each word.

(E) STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up, after receiving a STOP bit in read mode, or after completing a self-time internal programming operation.

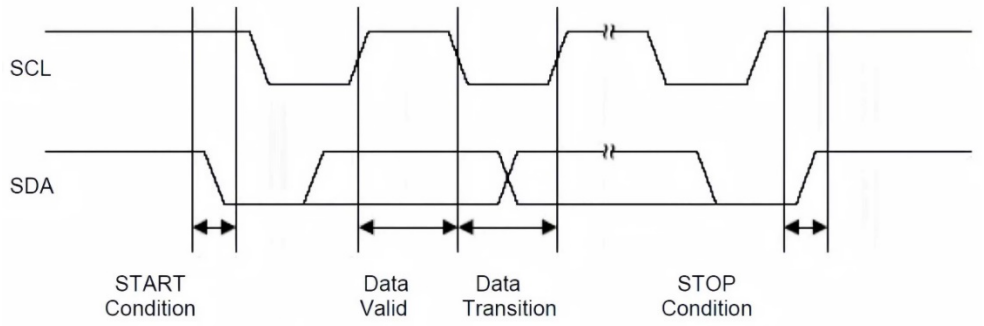
(F) SOFT RESET

After an interruption in protocol power loss or system reset, any two-wire part can be reset by following these steps:

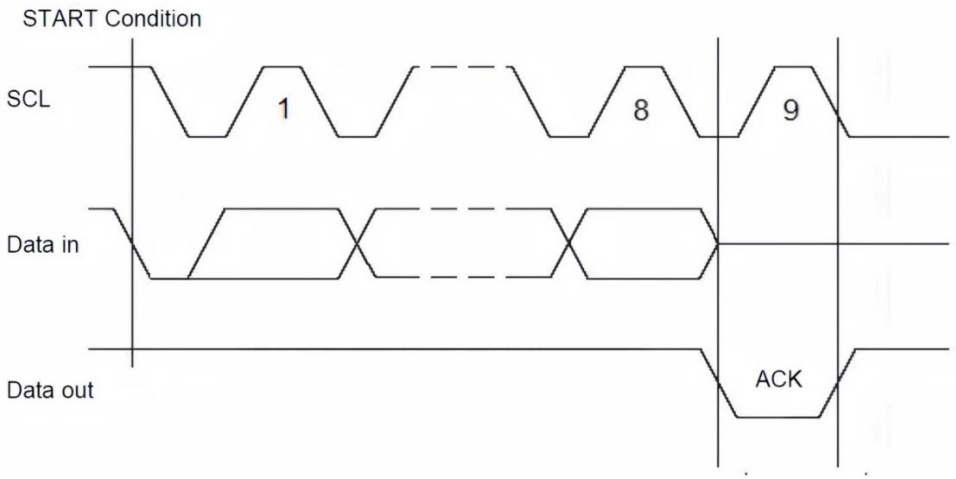
1. Creat a START condition,

2. Clock eighteen data bits “1”,

3. Creat a start condition as SDA is high.



Timing diaram for START and STOP conditions



Timing diagram for output ACKNOWLEDGE

DEVICE ADDRESSING

The 2-wire serial bus protocol mandates an 8 bits device address word after a START bit condition to invoke valid read or write command. The first four most significant bits of the device address must be 1010, which is common to all serial EEPROM devices. The next three bits are device address bits. These three device address bits (5th, 6th and 7th) are to match with the external chip select/address pin states. If a match is made, the EEPROM device outputs an ACKNOWLEDGE signal after the 8th read/write bit, otherwise the chip will go into STANDBY mode.

The last or 8th bit is a read/write command bit. If the 8th bit is at VIH then the chip goes into read mode. If a "0" is detected, the device enters programming mode.

WRITE OPERATIONS

(A) BYTE WRITE

A byte write operation starts when a micro-controller sends a START bit condition, follows by a proper EEPROM device address and then a write command. If the device address bits match the chip select address, the EEPROM device will acknowledge at the 9th clock cycle. The micro-controller will then send the rest of the lower 8 bits word address. At the 18th cycle, the EEPROM will acknowledge the 8-bit address word. The microcontroller will then transmit the 8 bit data. Following an ACKNOWLDEGE signal from the EEPROM at the 27th clock cycle, the micro-controller will issue a STOP bit. After receiving the STOP bit, the EEPROM will go into a self-timed programming mode during which all external inputs will be disabled. After a programming time of T_{WC}, the byte programming will finish and the EEPROM device will return to the STANDBY mode.

(B) PAGE WRITE

A page write is similar to a byte write with the exception that one to sixteen bytes can be programmed along the same page or memory row. All QN24C02 are organized to have 16 bytes per memory row or page.

With the same write command as the byte write, the micro-controller does not issue a STOP bit after sending the 1st byte data and receiving the ACKNOWLEDGE signal from the EEPROM on the 27th clock cycle. Instead it sends out a second 8-bit data word, with the

EEPROM acknowledging at the 36th cycle. This data sending and EEPROM acknowledging cycle repeats until the micro-controller sends a STOP bit after the n X 9th clock cycle. After which the EEPROM device will go into a self-timed partial or full page programming mode. After the page programming completes after a time of T_{WC}, the devices will return to the STANDBY mode.

The least significant 4 bits of the word address (column address) increments internally by one after receiving each data word. The rest of the word address bits (row address) do not change internally, but pointing to a specific memory row or page to be programmed. The first page write data word can be of any column address. Up to 16 data words can be loaded into a page. If more then 16 data words are loaded, the 17th data word will be loaded to the 1st data word column address. The 18th data word will be loaded to the 2nd data word column address and so on. In other word, data word address (column address) will "roll" over the previously loaded data.

(C) ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE signal at the 9th clock cycle.

READ OPERATIONS

The read command is similar to the write command except the 8th read/write bit in address word is set to "1".The three read operation modes are described as follows:

(A) CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the micro-controller issues a START bit and a valid device address word with the read/write bit (8th) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the

micro-controller will not issue an ACKNOWLEDGE signal on the 18th clock cycle. The micro-controller issues a valid STOP bit after the 18th clock cycle to terminate the read operation. The device then returns to STANDBY mode.

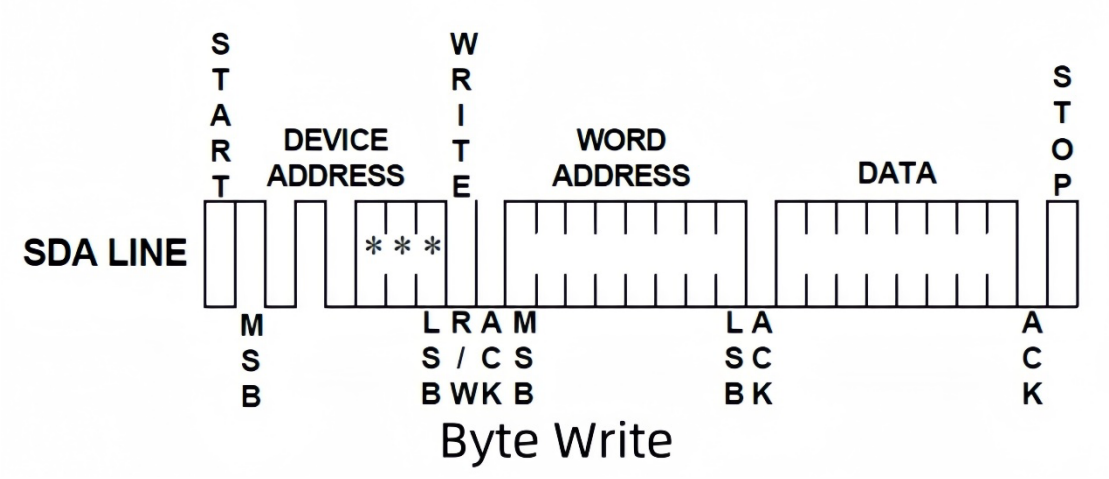
(B) SEQUENTIAL READ

The sequential read is very similar to current address read. The micro-controller issues a START bit and a valid device address word with read/write bit (8th) set to "1". The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one. Unlike current address read, the micro-controller sends an ACKNOWLEDGE signal on the 18th clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs another data, it sends out an ACKNOWLEDGE signal on the 27th clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address. Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a STOP bit afterwards instead.

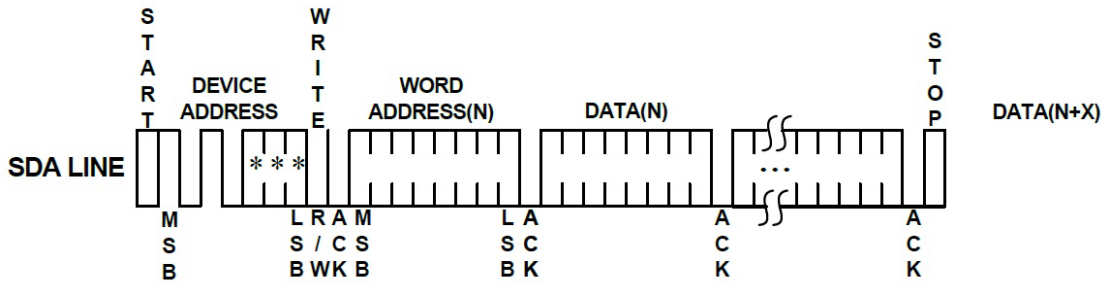
(C) RANDOM READ

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a "dummy write" instruction. The second step is a current address read.

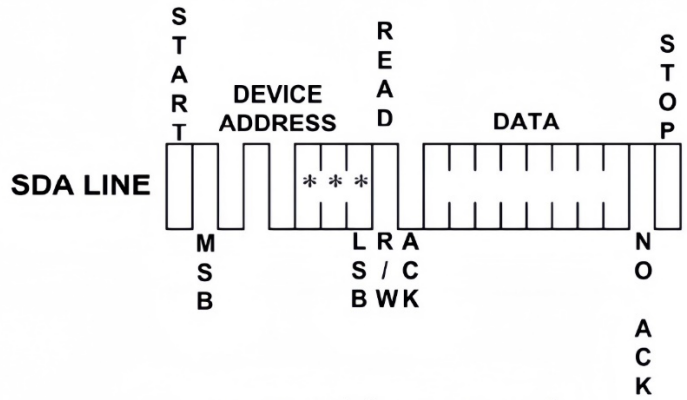
To initialize the internal address counter with a target read address, the micro-controller issues a START bit first, follows by a valid device address with the read/write bit (8th) set to "0". The EEPROM will then acknowledge. The micro-controller will then send the address word. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro-controller performs a current address read instruction to read the data. Note that once a START bit is issued, the EEPROM will reset the internal programming process and continue to execute the new instruction - which is to read the current address.



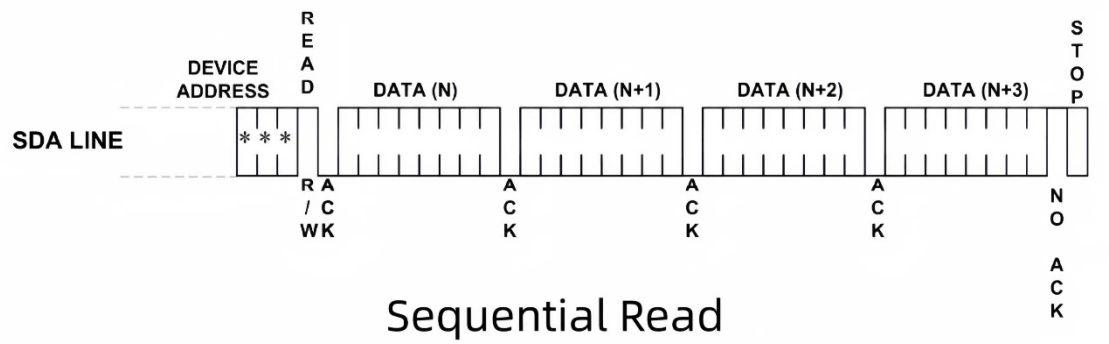
Byte Write



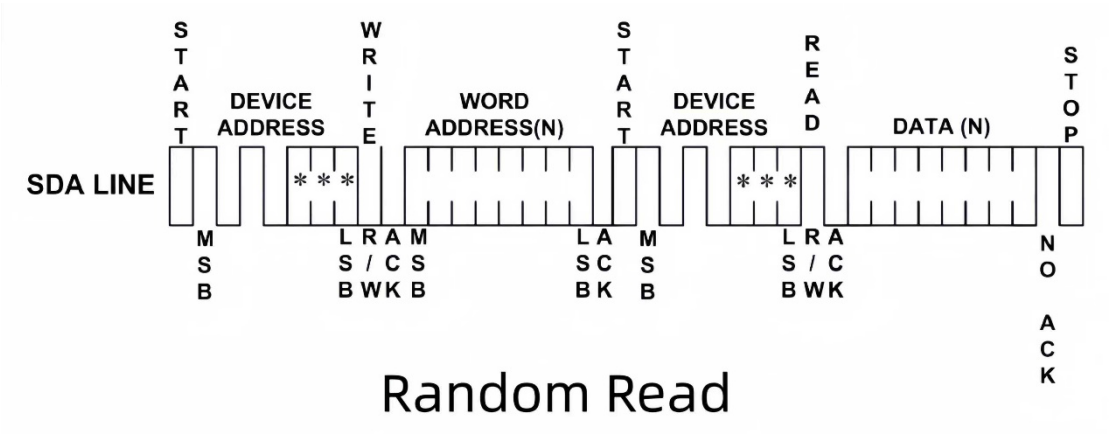
Page Write



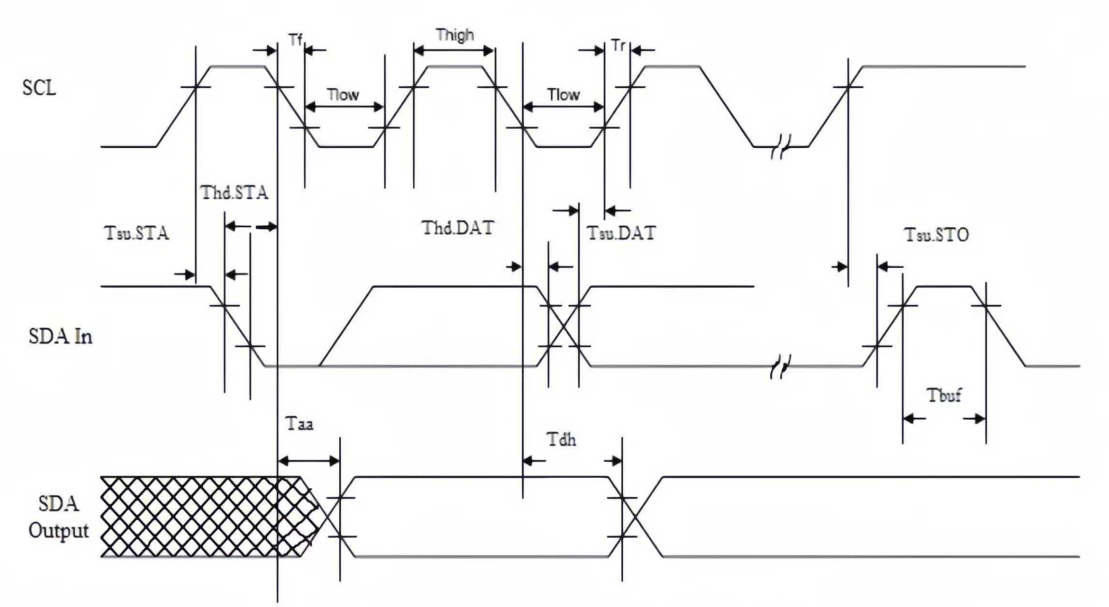
Current Address Read



Sequential Read



Random Read



SCL and SDA Bus Timing

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
	Ambient temperature with power applied	-55 ~ +130	℃
T_{STG}	Storage temperature	-65 ~ +150	℃
V_{CC}	Supply voltage	-0.5 ~ +6.0	V
V_{IN}	Voltage on input Pins	-0.5 ~ +6.0	V
V_{ESD}	Electrostatic pulse (human body model)	5000	V
T_L	Lead Temperature (Soldering, 10 seconds)	260	℃

Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Operating range: TA = -40°C ~ +105°C, VCC = 1.7V ~ 5.5V (unless otherwise noted).

Symbol	Parameter	Test Conditon	Min	Max	Unit
V_{CC}	Supply Voltage		1.7	5.5	V
I_{CC1}	Supply Current (Read)	V_{CC}= 1.7V, Read at 1MHz		0.1	mA
		V_{CC}= 5.5V, Read at 400 kHz		0.4	mA
		V_{CC}= 5.5V, Read at 1MHz		0.5	mA
I_{CC2}	Supply Current (Write)	V_{CC}= 1.7V, Write at 400 kHz		0.2	mA
		V_{CC}= 5.5V, Write at 400 kHz		0.5	mA
I_{SB}	Standby Current	V_{CC} = 1.7V, V_{IN} = V_{CC} or GND		0.5	μA
		V_{CC} = 5.5V, V_{IN} = V_{CC} or GND		1.0	μA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or GND		1.0	μA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or GND		1.0	μA
V_{IL}	Input Low-Level Voltage (SDA, SCL)		-0.5	0.3*V_{CC}	V
V_{IH}	Input High-Level Voltage (SDA, SCL)		0.7*VCC	VCC+0.5	V
V_{OL1}	Low-Level Output Voltage	V_{CC}> 2V, I_{OL}= 3mA		0.4	V
V_{OL2}	Low-Level Output Voltage	V_{CC}≤2V, I_{OL}= 2mA		0.2	V

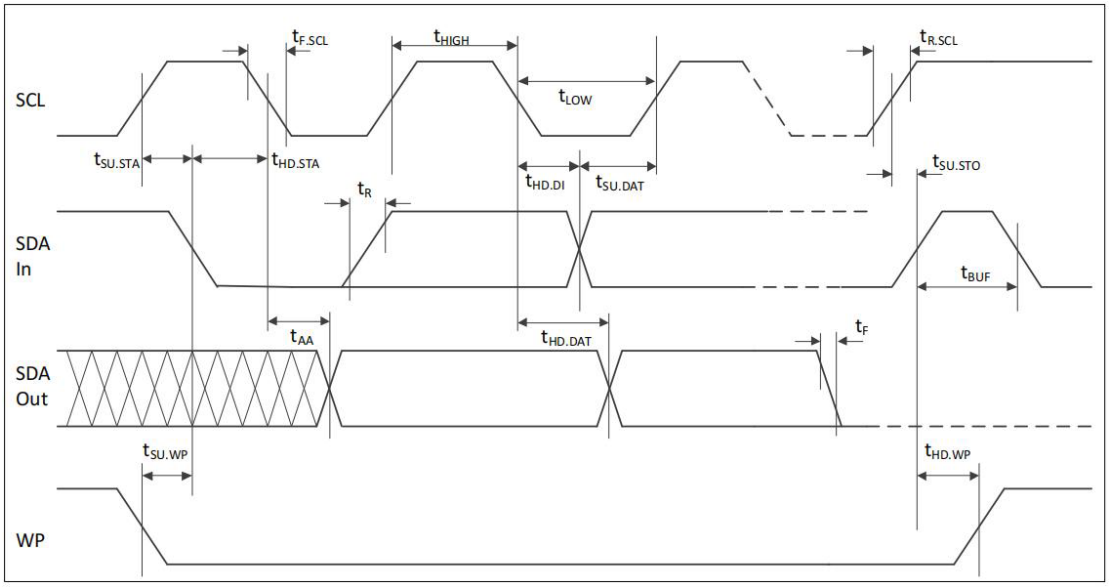
AC Characteristics

Operating range: T_A = -40°C ~ +105°C, V_{CC} = 1.7V ~ 5.5V, C_L = 100pF (unless otherwise noted).
Measurement conditions: Input rise and fall time ≤ 50ns Input pulse voltages: 0.2*V_{CC} ~ 0.8*V_{CC} Input and output timing reference voltages: 0.3*V_{CC} ~ 0.7*V_{CC}

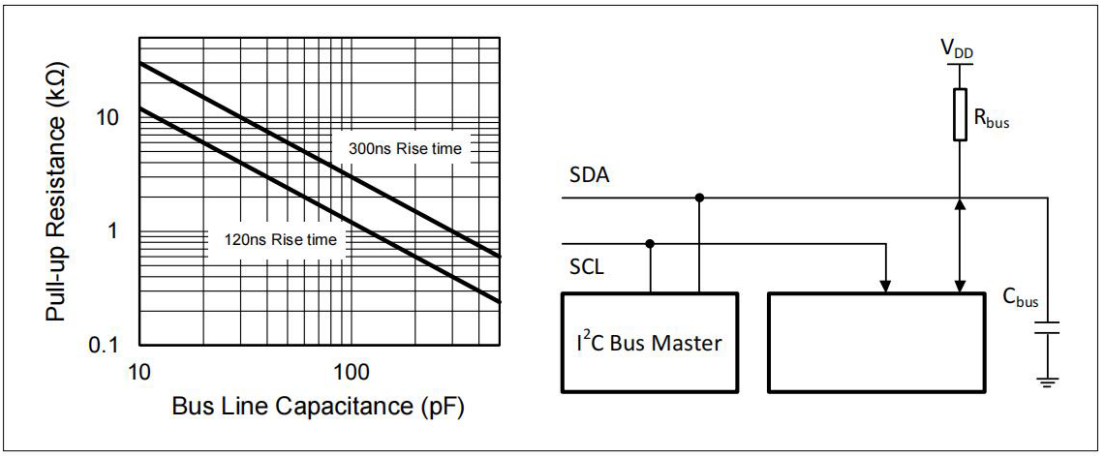
Symbol	Parameter	Fast Mode V_{CC} = 1.7V ~ 5.5V		High Speed Mode V_{CC} = 1.7V ~ 5.5V		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1300		600		ns
t_{HIGH}	Clock Pulse Width High	600		260		ns
t_R[1]	SDA Rise Time		300		300	ns
t_F[1]	SDA(Out) Fall Time		300		100	ns
$t_{HD.STA}$	Start Hold Time	600		250		ns
$t_{SU.STA}$	Start Setup Time	600		250		ns
$t_{SU.STO}$	Stop Setup Time	600		250		ns
t_{BUF}	Bus Free Time between Stop and Next Start	1300		500		ns
$t_{HD.DI}$	Data In Hold Time	0.0		0.0		ns
$t_{SU.DAT}$	Data In Setup Time	100		50		ns
$t_{HD.DAT}$	Data Out Hold Time	50		50		ns

t_{AA}	SCL Low to Data Out Valid	100	900	50	500	ns
$t_{SU.WP}$	WP Pin Setup Time	1200		600		ns
$t_{HD.WP}$	WP Pin Hold Time	1200		600		ns
t_{WR}	Write Cycle Time		5		5	ms
t_I	Noise Suppression Time		50		50	ns

Bus Timing



Maximum Pull-up Resistance vs. Bus Parasitic Capacitance



Pin Capacitance

Operating range for pin capacitance: TA = +25°C, fC = 1MHz, VCC = 1.7V ~ 5.5V.

Symbol	Parameter	Max	Unit	Test Condition
$C_{I/O}$	Input/output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (other Pins)	6	pF	$V_{I/O}$ = 0V

These parameters are ensured by characterization only.

Reliability Characteristics

Symbol	Parameter	Min	Unit	Test Condition
NW	Write Cycle Endurance	$2x10^6$	cycle	TA = +25°C, Page Mode
D_R	Data Retention	200	year	TA = +25°C

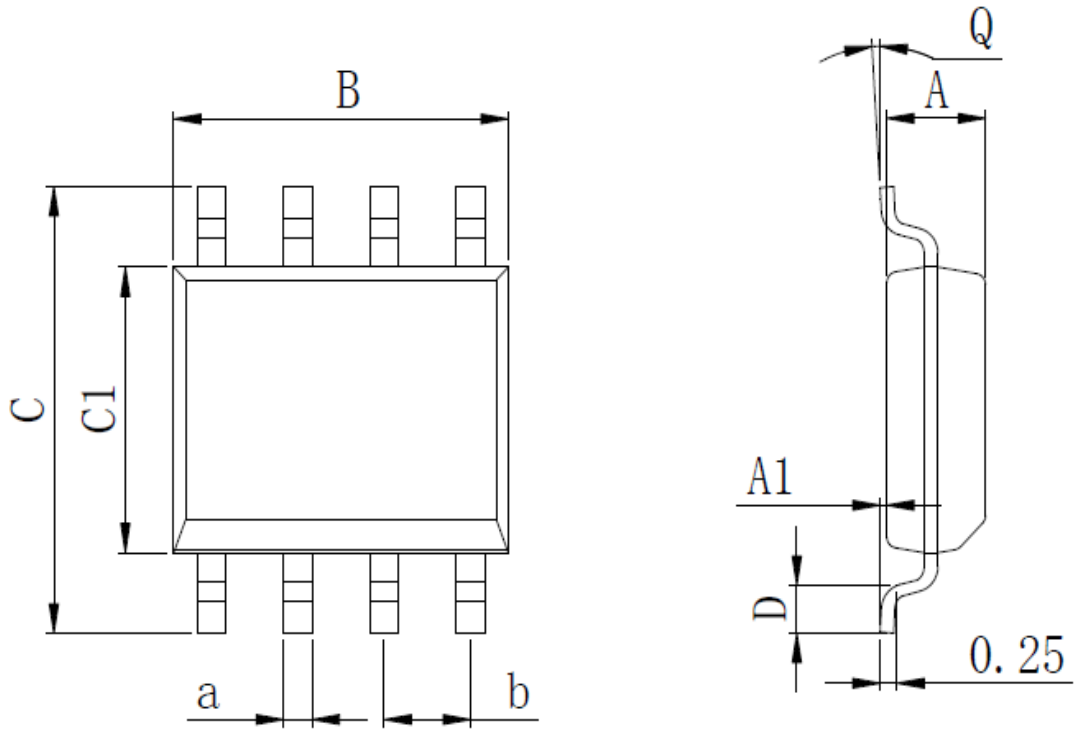
Initial Delivery State

The QN24C02 serial EEPROM is delivered as follows:

- All bits in the memory array are set to '1' (each byte contains FFh).
- All bits in the Identification Page are set to '1' (each byte contains FFh).
- The Software Write Protection bit is set to '0'.

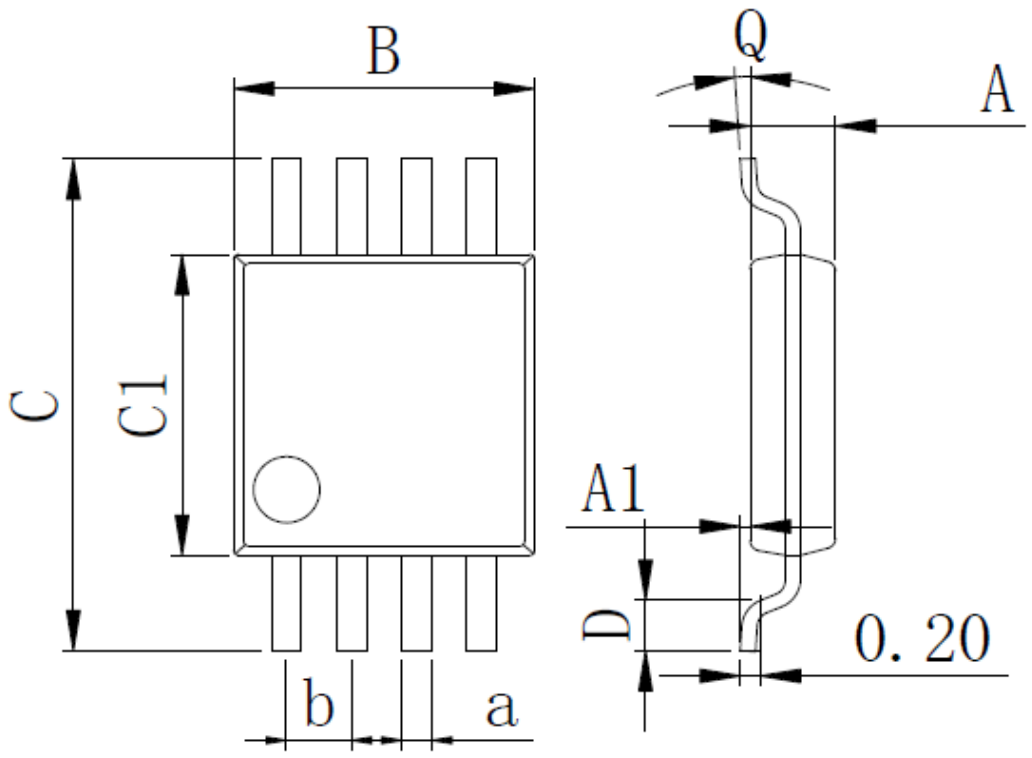
Physical Dimensions

SOP-8



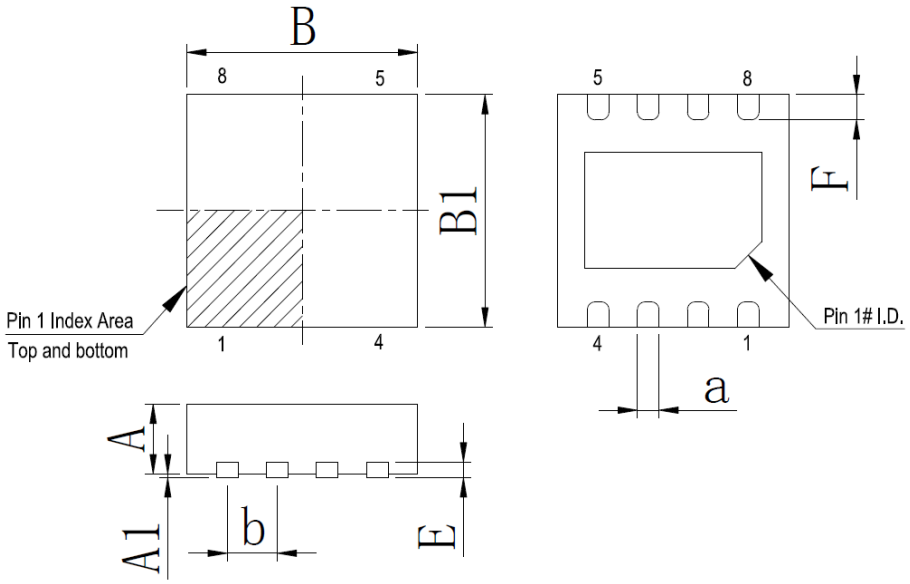
Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

MSOP-8



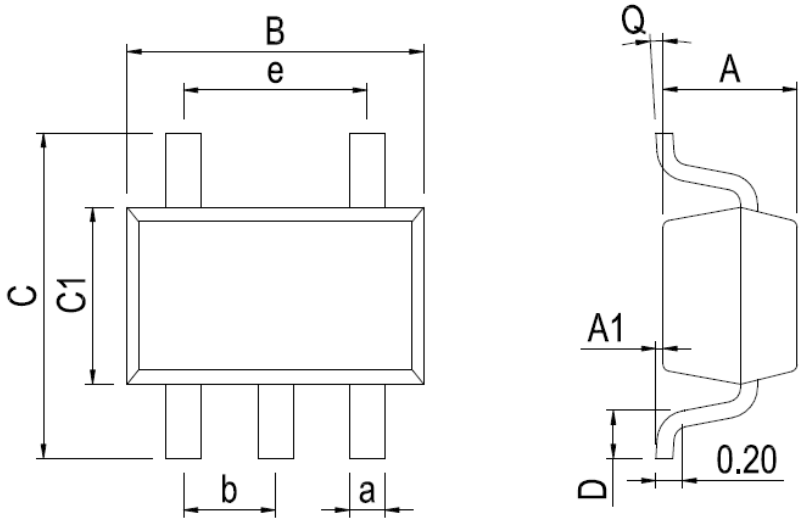
Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

DFN-8 3*3



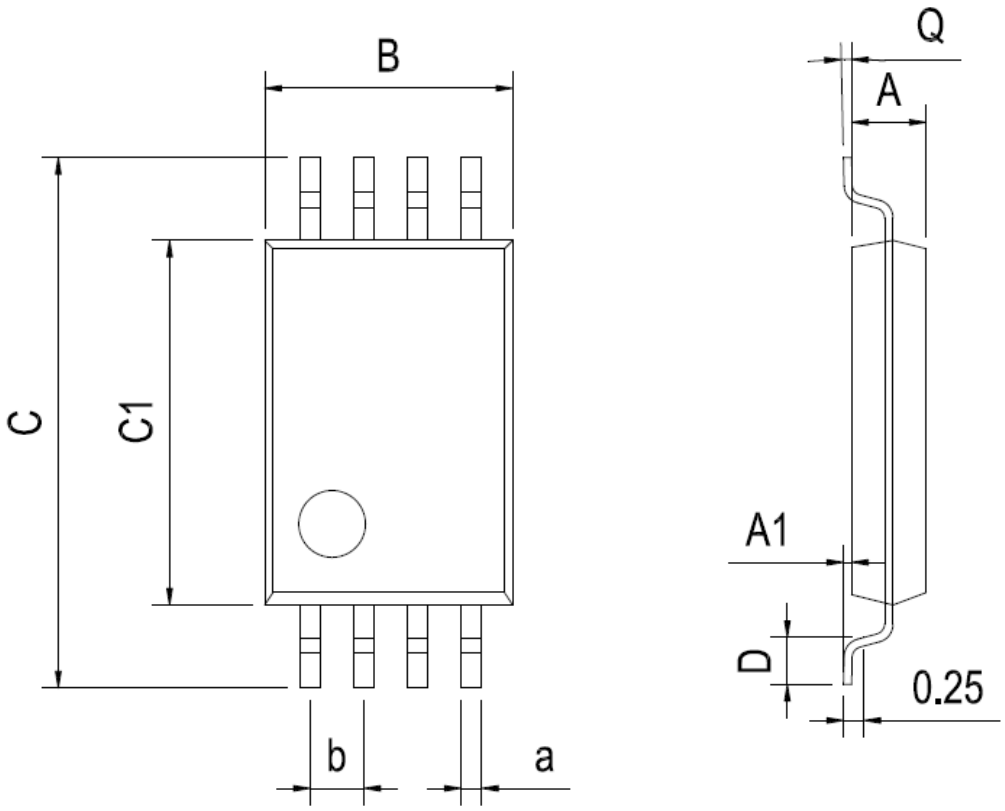
Dimensions In Millimeters(DFN-8 3*3)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0.00	2.90	2.90	0.20	0.30	0.20	0.65BSC
Max:	0.95	0.05	3.10	3.10	0.25	0.50	0.34	

SOT23-5



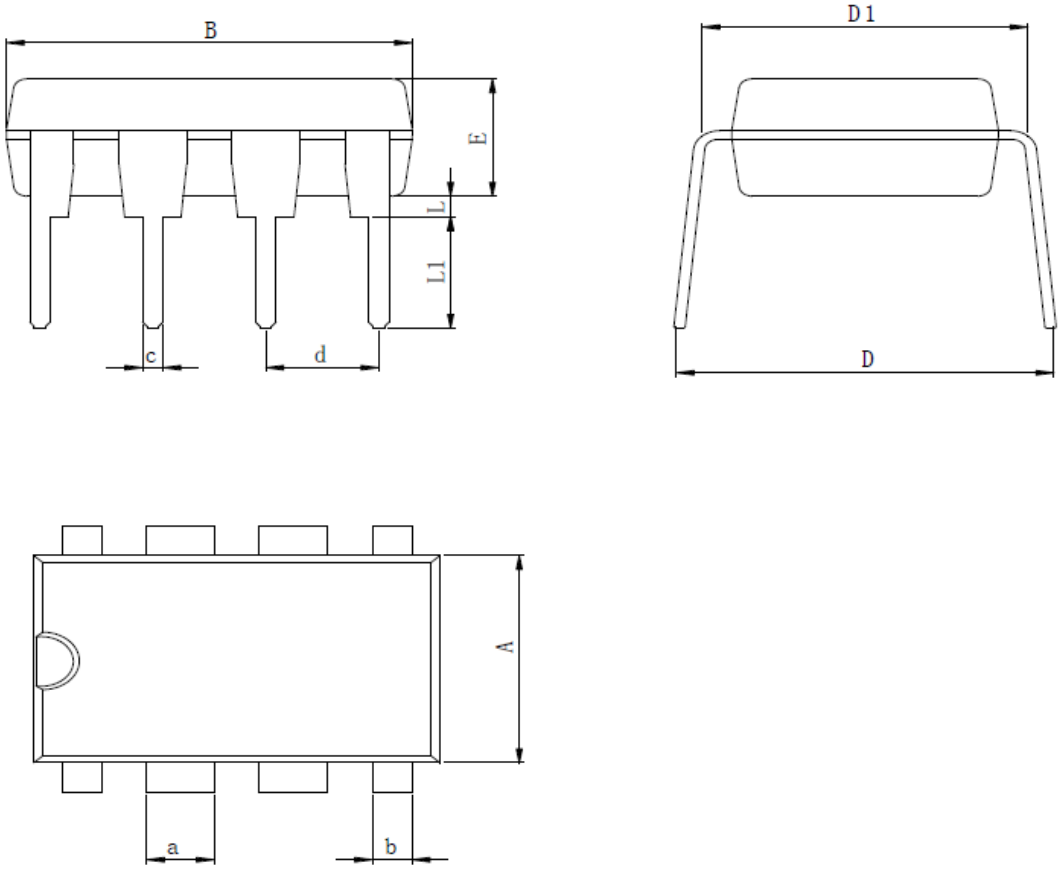
Dimensions In Millimeters(SOT23-5)										
Symbol:	A	A1	B	C	C1	D	Q	a	b	e
Min:	1.00	0.00	2.82	2.65	1.50	0.30	0°	0.30	0.95	1.90
Max:	1.15	0.15	3.02	2.95	1.70	0.60	8°	0.50	BSC	BSC

TSSOP-8 (4.4*3.0)



Dimensions In Millimeters(TSSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	2.90	6.20	4.30	0.40	0°	0.20	0.65
Max:	0.95	0.20	3.10	6.60	4.50	0.80	8°	0.25	BSC

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	BSC

Ordering Information

Device	Package Type	Marking	Packing	Packing Qty
QN24C02CN	DIP-8	24C02C	TUBE	2000pes/box
QN24C02CM/TR	SOP-8	24C02C	REEL	2500pes/reel
QN24C02CMM/TR	MSOP-8	24C02C,C02C	REEL	3000pcs/reel
QN24C02CDQ/TR	DFN-8 3*3	C02C	REEL	5000pcs/reel
QN24C02CM5/TR	SOT-23-5	2CMU	REEL	3000pcs/reel
QN24C02CMT/TR	TSSOP-8	24C02C	REEL	2500pcs/reel