YT9215SCH Datasheet

LAYER 2 MANAGED 5+2 PORT 10/100/1000M SWITCH CONTROLLER

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General Description

YT9215SCH is a LQFP128 E-PAD, high-performance 5+2-port Gigabit Ethernet switch. It integrates five PHY support 1000Base-T/100Base-TX/10Base-Te, and two extra MAC ports for specific applications that support MII/RMII/RGMII/SGMII/1000Base-X/100Base-FX/2500Base-X. YT9215SCH is also embedded with a RISC-V microprocessor.

The integrated GIGA-PHY complies with 10BASE-Te, 100BASE-TX, and 1000BASE-T IEEE standard 802.3 and also supports Motorcomm's proprietary LRE100-4 feature, which makes the device can auto-negotiate and link up with LRE100-4 compliant link partners. LRE100-4 in extended cable length applications up to 400 meters at 100Mbps over CAT5E cable.

The YT9215SCH Extension GMAC1 and Extension GMAC2 support xMII or SerDes interfaces for connecting with an external PHY, MAC, external CPU, or RISC in specific applications and also support providing an optical port directly by SerDes. xMII refers to Reduced Gigabit Media Independent Interface (RGMII), Media Independent Interface (MII), and Reduced Media Independent Interface (RMII). The SerDes supports IEEE 100Base-FX, IEEE 1000Base-X, and IEEE 2500Base-X.

YT9215SCH integrates a 4K look-up table with an efficient hashing algorithm for address searching and learning, each entry can be configured as a static entry.

YT9215SCH supports IEEE 802.1Q VLAN and has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol-and-port-based, VLAN translation, flow-based capability, MAC-based, and IP-subnet-based VLAN, which can be supported by configuration. It also supports IVL, SVL, and IVL/SVL for flexible network topology architecture.

The YT9215SCH supports standard 802.3x flow control frames for full duplex and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources. The YT9215SCH supports storm control.

To support flexible traffic classification, the YT9215SCH supports 384-hardware entry ACL rule checks and multiple action options. The 384 entries are composed of 48 rows, each row has 8 entries. To support the long rule, rule extension is supported by any combinations of the 8 entries for each row. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority/DSCP value in 802.1q/Q tag, and rate policing.

Key Features

- High performance, nonblocking, 7 port Ethernet Switch integrating
  - Five 10/100/1000Mbps PHYs with Advanced Cable Status Diagnostic (CSD) features
  - Each PHY supports 10/100/1000M full duplex connectivity (half duplex only supported in 10/100M mode)
  - Full duplex and half duplex operation with IEEE 802.3x flow control and backpressure
- Interface
  - Embedded 5-port 1000Base-T/100Base-TX/10Base-Te PHY

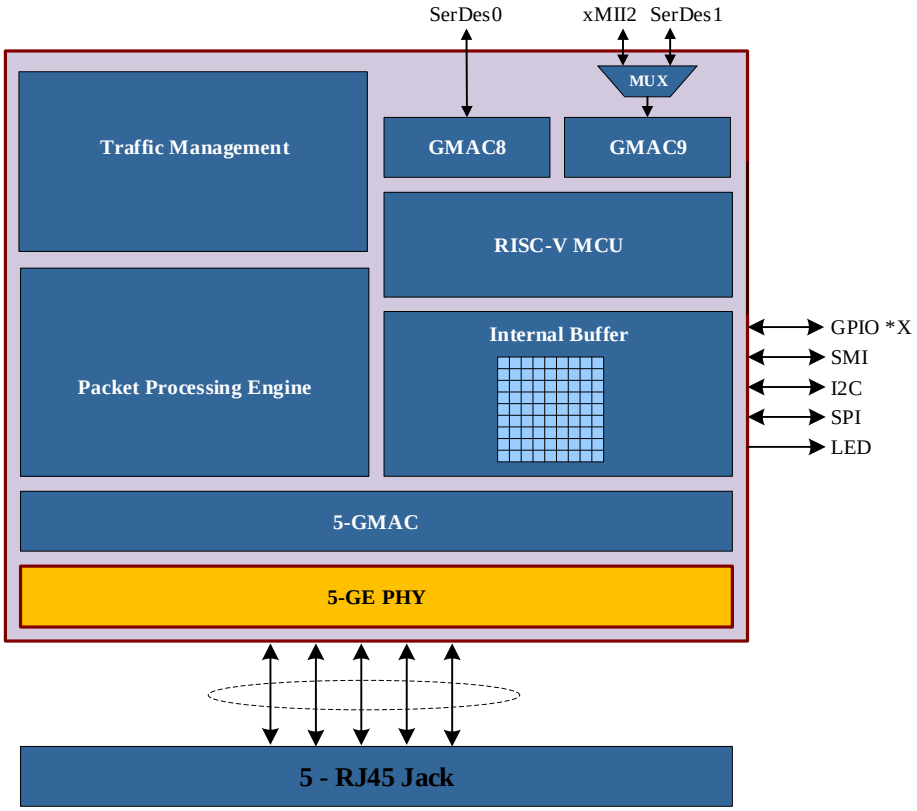
  - Embedded two 3.125Gbps/1.25Gbps SerDes for 2500Base-X/SGMII/1000Base-X/ 100Base-FX
  - Embedded one RGMII/MII/RMII interface
- Advanced Features
  - Support parallel LED or serial LED outputs
  - Support SPI/SMI/I2C Slave interface
  - Support SMI/I2C Master interface
  - Support 1 interrupt output to external CPU for notification
  - Support 64K-byte EEPROM space for configuration
  - Link On Cable Length Power Saving
  - Link Down Power Saving
  - Support 9K byte jumbo frames
- Support 2 IEEE 802.3ad Link aggregation port groups
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Unknown DA filter mask
  - Support Port Isolation
  - Support Broadcast/Multicast/Unknown DA storm control protects the system from attack by hackers
  - Supports DOS attack prevention
- Control, Management and Statistics
  - Support RFC MIB Counters
    - MIB-II (RFC 1213)
    - Ethernet-Like MIB (RFC 3635)
    - Interface Group MIB (RFC 2863)
    - RMON (RFC 2819)
    - Bridge MIB (RFC 1493)
    - Bridge MIB Extension (RFC 2674)
  - Support OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol)
  - Support Loop Detection
- Packet Process Engine
  - Support 802.1Q VLANs
  - Support 4K VLANs
  - Support untag definition in each VLAN
  - Support VLAN policing and VLAN forwarding decision
  - Support Port-based, Tag-based, and Protocol-based VLAN
  - Support per port egress VLAN tagging and untagging
  - Support IEEE 802.1D/s/w Spanning Tree Protocols

- Support Multicast VLAN (MVR)
- Supports IVL, SVL, and IVL/SVL
- Support IEEE 802.1ad Stacking VLAN
- Support VLAN translation (1:1/2:1/2:2/ N:1/1:N)
- Support IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN
- Support ACL Rules
- Support Hardware/Software IGMP/MLD Snooping
  - Support Fast Leave
  - Support IGMPV1/V2/V3
  - Static/Dynamic Router port
- Mirror
  - Port-based mirror
  - Flow-based mirror
- Support reserved multicast control
- Support WOL

- Support Quality of Service (QoS)
  - Supports queue-based DWRR/SP, packet/byte modes are both supported for DWRR
  - Support min-max queue-based shaping, packet/byte modes are both supported
  - Support single token bucket for port-based shaping, packet/byte modes are both supported
  - Support per port Input Bandwidth Control, packet/byte modes are both supported
  - trTCM color aware/blind packet/byte modes
  - Traffic classification based on multiple source type
  - Support 8 unicast queues and 4 multicast queues for each port
  - Tail drop is supported for UQ/MQ, WRED is supported for UQ
- Microprocessor
  - Integrated RISC-V microprocessor
  - Support Flash Interface (Dual mode/Single mode)
- 25MHz crystal or 3.3V OSC input
- LQFP 128-pin E-PAD package

Block Diagram

Figure 1 Block Diagram



System Applications

- 5-Port 1000Base-T+1-Port RGMII + 1-Port 2500Base-X Switch
- 5-Port 1000Base-T+2-Port 2500Base-X/1000Base-X/100Base-FX Switch
- 5-Port 1000Base-T Router with Single MII/RGMII
- 5-Port 1000Base-T Router with Dual SGMII
- 5-Port 1000Base-T NVR
- 5-Port 1000Base-T ONU

Revision History

Revision	Release Date	Description
V1.03	2025-02-10	● Update t6 parameter description of Master SMI Timing, see 7.4.4 Master SMI Timing Characteristics. ● Update t6 max of Slave SMI Timing Parameter, see 7.4.7 Slave SMI Timing Characteristics. ● Update t3, t4, and t5 parameter description of Slave SPI Timing, see 7.4.8 Slave SPI Timing Characteristics. ● Add parameter RMS Jitter (12kHz~20MHz), see 7.6 Oscillator/External Clock Requirement.
V1.02	2024-12-12	● Update TskewR value, Data Input Hold Time min value, and AC Coupling Capacitor max value, see 7.4 AC Characteristics. ● Update Mechanical Information, see 9 Mechanical Information. ● Update the slave I2C format， see 5.5.1 Slave I2C Interface for External CPU. ● Update document style and description.
V1.01	2024-01-19	● Modify chapter 1 pin assignment; ● Modify chapter 4.2 autoload strap pin; ● Modify chapter 7.3 DC characteristics – VDDL voltage; ● Modify chapter 7.4 RGMII/SerDes characteristics; ● Modify chapter 9 mechanical information – EPAD, package;
V1.0	2023-08-04	First version.

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1.1 Pin Assignment

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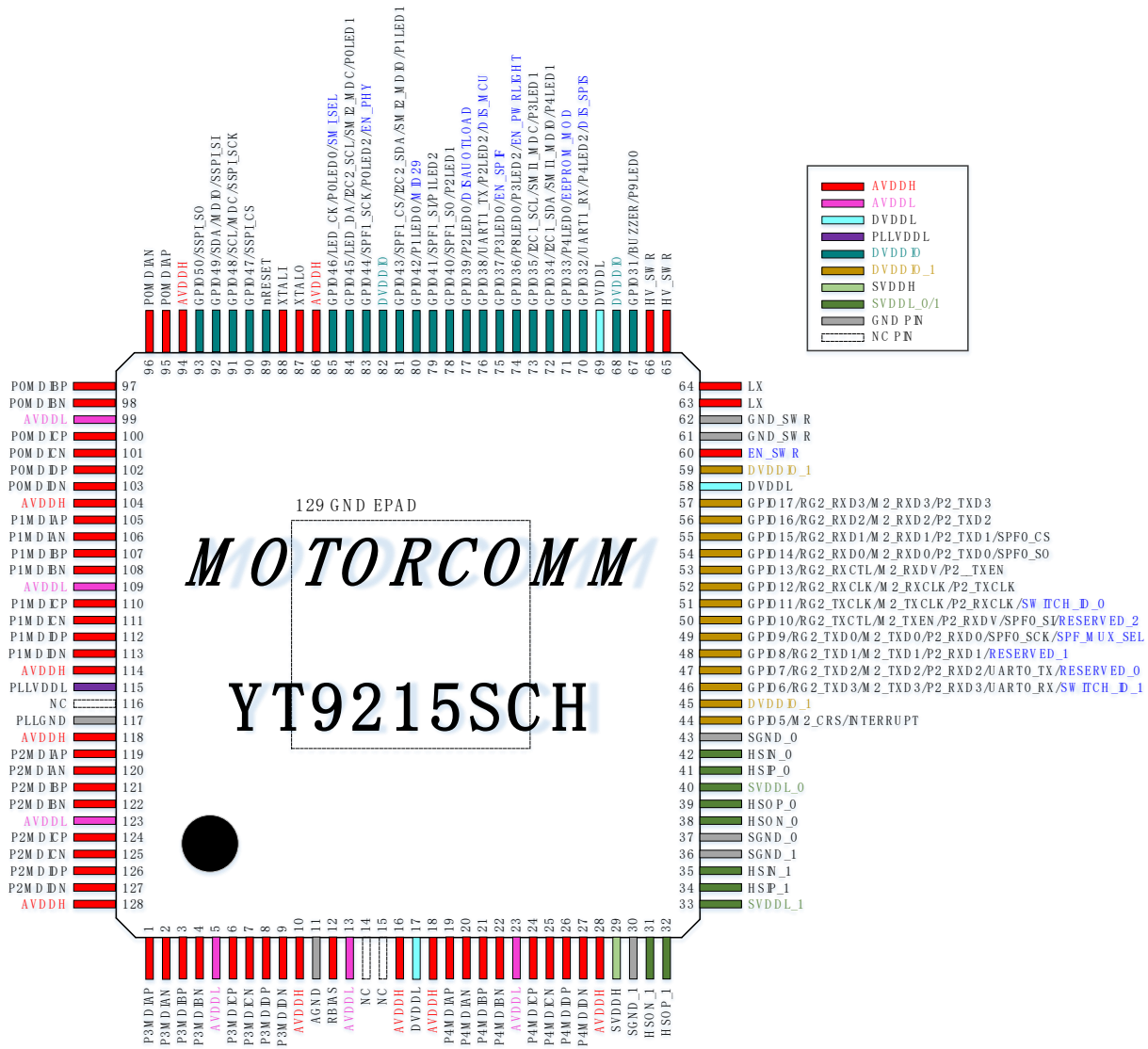


1.2 Pin Assignment Table

Some pins have multiple functions. Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Digital Power Pin
- G: Digital Ground Pin
- PU: Internal Pull Up
- LI: Latched Input During Power Up
- OD: Open Drain
- AI: Analog Input
- AO: Analog Output
- AIO: Analog Bidirectional Input and Output
- AP: Analog Power Pin
- AG: Analog Ground Pin
- PD: Internal Pull Down
- XT: Crystal Related

Table 1 Pin Assignment

No.	Pin Name	Type
1	P3MDIAP	AIO
2	P3MDIAN	AIO
3	P3MDIBP	AIO
4	P3MDIBN	AIO
5	AVDDL	AP
6	P3MDICP	AIO
7	P3MDICN	AIO
8	P3MDIDP	AIO
9	P3MDIDN	AIO
10	AVDDH	AP
11	AGND	AG
12	RBIAS	AO
13	AVDDL	AP
14	NC	-
15	NC	-
16	AVDDH	AP
17	DVDDL	P
18	AVDDH	AP
19	P4MDIAP	AIO
20	P4MDIAN	AIO
21	P4MDIBP	AIO
22	P4MDIBN	AIO
23	AVDDL	AP
24	P4MDICP	AIO
25	P4MDICN	AIO
26	P4MDIDP	AIO
27	P4MDIDN	AIO
28	AVDDH	AP
29	SVDDH	AP
30	SGND_1	AG
31	HSON_1	AO
32	HSOP_1	AO
33	SVDDL_1	AP
34	HSIP_1	AI
35	HSIN_1	AI
36	SGND_1	AG
37	SGND_0	AG
38	HSON_0	AO
39	HSOP_0	AO
40	SVDDL_0	AP
41	HSIP_0	AI
42	HSIN_0	AI
43	SGND_0	AG
44	GPIO5/M2_CRS/INTERRUPT	IO/PD
45	DVDDIO_1	P
46	GPIO6/RG2_TXD3/M2_TXD3/P2_RXD3/UART0_RX/SWITCH_ID_1	IO/LI/PD
47	GPIO7/RG2_TXD2/M2_TXD2/P2_RXD2/UART0_TX/RESERVED_0	IO/LI/PU
48	GPIO8/RG2_TXD1/M2_TXD1/P2_RXD1/RESERVED_1	IO/LI/PU
49	GPIO9/RG2_TXD0/M2_TXD0/P2_RXD0/SPF0_SCK/SPF_MUX_SEL	IO/PD
50	GPIO10/RG2_TXCTL/M2_TXEN/P2_RXDV/SPF0_SI/RESERVED_2	IO/LI/PD
51	GPIO11/RG2_TXCLK/M2_TXCLK/P2_RXCLK/SWITCH_ID_0	IO/LI/PD
52	GPIO12/RG2_RXCLK/M2_RXCLK/P2_TXCLK	IO/PU

No.	Pin Name	Type
53	GPIO13/RG2_RXCTL/M2_RXDV/P2_TXEN	IO/PU
54	GPIO14/RG2_RXD0/M2_RXD0/P2_TXD0/SPF0_SO	IO/PU
55	GPIO15/RG2_RXD1/M2_RXD1/P2_TXD1/SPF0_CS	IO/PU
56	GPIO16/RG2_RXD2/M2_RXD2/P2_TXD2	IO/PU
57	GPIO17/RG2_RXD3/M2_RXD3/P2_TXD3	IO/PU
58	DVDDL	P
59	DVDDIO_1	P
60	EN_SWR	AI
61	GND_SWR	AG
62	GND_SWR	AG
63	LX	AO
64	LX	AO
65	HV_SWR	AP
66	HV_SWR	AP
67	GPIO31/BUZZER/P9LED0	IO/PU
68	DVDDIO	P
69	DVDDL	P
70	GPIO32/UART1_RX/P4LED2/DIS_SPIS	IO/LI/PU
71	GPIO33/P4LED0/EEPROM_MOD	IO/LI/PU
72	GPIO34/I2C1_SDA/SMI1_MDIO/P4LED1	IO/PU/OD
73	GPIO35/I2C1_SCL/SMI1_MDC/P3LED1	IO/PU/OD
74	GPIO36/P8LED0/P3LED2/EN_PWRLIGHT	IO/LI/PU
75	GPIO37/P3LED0/EN_SPIF	IO/LI/PU
76	GPIO38/UART1_TX/P2LED2/DIS_MCU	IO/LI/PU
77	GPIO39/P2LED0/DISAUOTLOAD	IO/LI/PU
78	GPIO40/SPF1_SO/P2LED1	IO/PU
79	GPIO41/SPF1_SI/P1LED2	IO/PU
80	GPIO42/P1LED0/MID29	IO/LI/PU
81	GPIO43/SPF1_CS/I2C2_SDA/SMI2_MDIO/P1LED1	IO/PU/OD
82	DVDDIO	P
83	GPIO44/SPF1_SCK/P0LED2/EN_PHY	IO/LI/PU

No.	Pin Name	Type
84	GPIO45/LED_DA/I2C2_SCL/SMI2_MDC/P0LED1	IO/PU/OD
85	GPIO46/LED_CK/P0LED0/SMI_SEL	IO/LI/PU
86	AVDDH	AP
87	XTALO	XT
88	XTALI	XT
89	nRESET	AI/PU
90	GPIO47/SSPI_CS	IO/PU
91	GPIO48/SCL/MDC/SSPI_SCK	IO/PU/OD
92	GPIO49/SDA/MDIO/SSPI_SI	IO/PU/OD
93	GPIO50/SSPI_SO	IO/PU
94	AVDDH	AP
95	P0MDIAP	AIO
96	P0MDIAN	AIO
97	P0MDIBP	AIO
98	P0MDIBN	AIO
99	AVDDL	AP
100	P0MDICP	AIO
101	P0MDICN	AIO
102	P0MDIDP	AIO
103	P0MDIDN	AIO
104	AVDDH	AP
105	P1MDIAP	AIO
106	P1MDIAN	AIO
107	P1MDIBP	AIO
108	P1MDIBN	AIO
109	AVDDL	AP
110	P1MDICP	AIO
111	P1MDICN	AIO
112	P1MDIDP	AIO
113	P1MDIDN	AIO
114	AVDDH	AP
115	PLLVDDL	AP
116	NC	-
117	PLLGND	AG
118	AVDDH	AP
119	P2MDIAP	AIO
120	P2MDIAN	AIO
121	P2MDIBP	AIO
122	P2MDIBN	AIO
123	AVDDL	AP

No.	Pin Name	Type
124	P2MDICP	AIO
125	P2MDICN	AIO
126	P2MDIDP	AIO

No.	Pin Name	Type
127	P2MDIDN	AIO
128	AVDDH	AP
129	GND EPAD	G

2 Pin Description

2.1 MDI Interface Pins

Table 2 Transceiver Interface

No.	Pin Name	Type	Description
95	P0MDIAP	AIO	Port 0 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
96	P0MDIAN	AIO	
97	P0MDIBP	AIO	Port 0 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
98	P0MDIBN	AIO	
100	P0MDICP	AIO	Port 0 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
101	P0MDICN	AIO	
102	P0MDIDP	AIO	Port 0 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
103	P0MDIDN	AIO	
105	P1MDIAP	AIO	Port 1 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
106	P1MDIAN	AIO	
107	P1MDIBP	AIO	Port 1 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
108	P1MDIBN	AIO	
110	P1MDICP	AIO	Port 1 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
111	P1MDICN	AIO	
112	P1MDIDP	AIO	Port 1 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
113	P1MDIDN	AIO	
119	P2MDIAP	AIO	Port 2 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
120	P2MDIAN	AIO	
121	P2MDIBP	AIO	Port 2 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
122	P2MDIBN	AIO	
124	P2MDICP	AIO	Port 2 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
125	P2MDICN	AIO	
126	P2MDIDP	AIO	Port 2 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
127	P2MDIDN	AIO	
1	P3MDIAP	AIO	Port 3 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
2	P3MDIAN	AIO	
3	P3MDIBP	AIO	Port 3 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
4	P3MDIBN	AIO	
6	P3MDICP	AIO	Port 3 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
7	P3MDICN	AIO	
8	P3MDIDP	AIO	Port 3 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
9	P3MDIDN	AIO	
19	P4MDIAP	AIO	Port 4 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
20	P4MDIAN	AIO	
21	P4MDIBP	AIO	Port 4 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
22	P4MDIBN	AIO	
24	P4MDICP	AIO	

No.	Pin Name	Type	Description
25	P4MDICN	AIO	Port 4 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
26	P4MDIDP	AIO	Port 4 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
27	P4MDIDN	AIO	

2.2 RGMII Interface Pins

Table 3 RGMII 2 Interface Pins

No.	Pin Name	Type	Description
51	RG2_TXCLK	O/LI/PD	RGMII transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed.
50	RG2_TXCTL	O/LI/PD	RGMII Transmit Control Signal from the MAC.
46	RG2_TXD3	O/LI/PD	RGMII transmit Data. Data is transmitted from MAC to PHY via TXD [3:0].
47	RG2_TXD2	O/LI/PU	
48	RG2_TXD1	O/LI/PU	
49	RG2_TXD0	O/PD	
52	RG2_RXCLK	I/PU	RGMII continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream.
53	RG2_RXCTL	I/PU	RGMII receives the Control Signal to the MAC.
57	RG2_RXD3	I/PU	RGMII receives Data. Data is transmitted from PHY to MAC via RXD [3:0].
56	RG2_RXD2	I/PU	
55	RG2_RXD1	I/PU	
54	RG2_RXD0	I/PU	

2.3 MII Interface Pins

Table 4 MII2 Interface Pins

No.	Pin Name	Type	Description
51	M2_TXCLK/ P2_RXCLK	IO/LI/PD	● M_TXCLK Pin in MII MAC Mode. MII Transmit Clock (input). Used to synchronize M_TXD [3:0], and M_TXEN. M_TXCLK is an input pin in MII MAC mode. ● P_RXCLK Pin in MII PHY Mode. MII Receive Clock (output). Used to synchronize P_RXD [3:0], and P_RXDV. P_RXCLK is an output pin in MII PHY mode. The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te.
50	M2_TXEN/ P2_RXDV	O/LI/PD	● M_TXEN Pin in MII MAC Mode. ● MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXC.

No.	Pin Name	Type	Description
			● P_RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXC M_TXEN/P_RXDV is an output pin in MII MAC mode/MII PHY mode.
46	M2_TXD3/ P2_RXD3	O/LI/PD	● M_TXD [3:0] Pin in MII MAC Mode. MII Transmit Data Bus. M_TXD [3:0] is synchronous to M_TXC. ● P_RXD [3:0] Pin in MII PHY Mode. MII Receive Data Bus. P_RXD [3:0] is synchronous to P_RXC. M_TXD [3:0]/P_RXD [3:0] are output pins in MII MAC mode/MII PHY mode.
47	M2_TXD2/ P2_RXD2	O/LI/PU	
48	M2_TXD1/ P2_RXD1	O/LI/PU	
49	M2_TXD0/ P2_RXD0	O/LI/PD	
52	M2_RXCLK/ P2_TXCLK	IO/PU	● M_RXCLK Pin in MII MAC Mode. MII Receive Clock(input). Used to synchronize M_RXD [3:0], and M_RXDV. M_RXCLK is an input pin in MII MAC mode. ● P_TXCLK Pin in MII PHY Mode. MII Transmit Clock (output). Used to synchronize P_TXD [3:0], and P_TXEN. P_TXCLK is an output pin in MII PHY mode. The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te.
53	M2_RXDV/ P2_TXEN	IO/PU	● M_RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on the M_RXD bus. M_RXDV is synchronous to M_RXC. ● P_TXEN Pin in MII PHY Mode. MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXC. M_RXDV/P_TXEN is an input pin in MII MAC mode/MII PHY mode.
57	M2_RXD3/ P2_TXD3	I/PU	● M_RXD [3:0] Pin in MII MAC Mode. MII Receive Data Bus. M_RXD [3:0] is synchronous to M_RXC. ● P_TXD [3:0] Pin in MII 1 PHY Mode. MII Transmit Data Bus. P_TXD [3:0] is synchronous to P_TXC. M_RXD [3:0]/P_TXD [3:0] are input pins in MII MAC mode/MII PHY mode.
56	M2_RXD2/ P2_TXD2	I/PU	
55	M2_RXD1/ P2_TXD1	I/PU	
54	M2_RXD0/ P2_TXD0	I/PU	
44	M1_CRS	I/PD	Carrier Sense Input in MII MAC mode when operating in 10/100M half-duplex modes. This pin should be pulled low with a 1kΩ resistor if not used.

2.4 RMII Interface Pins

Table 5 RMII2 Interface Pins

No.	Pin Name	Type	Description
51	M2_TXCLK/ P2_RXCLK	IO/LI/PD	REF_CLK pin in RMII Mode. ● In RMII MAC Mode, REF_CLK is an input pin. ● In RMII PHY Mode, REF_CLK is an output pin. REF_CLK is a 50MHz clock that provides the timing reference for CRSDV, RXD [1:0], TXEN, and TXD [1:0].
50	M2_TXEN/ P2_RXDV	O/LI/PD	● TXEN Pin in RMII MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REF_CLK. ● CRSDV Pin in RMII PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receiving medium is nonidle synchronized with REF_CLK. M_TXEN/P_RXDV is an output pin in MII MAC mode/MII PHY mode.
48	M2_TXD1/ P2_RXD1	O/LI/PU	● TXD [1:0] Pin in RMII MAC Mode, synchronous to REF_CLK. ● RXD [1:0] Pin in RMII PHY Mode, synchronous to REF_CLK. M_TXD [1:0]/P_RXD [1:0] are output pins in MII MAC mode/MII PHY mode.
49	M2_TXD0/ P2_RXD0	O/PD	
53	M2_RXDV/ P2_TXEN	I/PU	● CRSDV Pin in RMII MAC Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is nonidle synchronized with REF_CLK. ● TXEN Pin in RMII PHY Mode. ● The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REF_CLK. M_RXDV/P_TXEN is an input pin in MII MAC mode/MII PHY mode.
55	M2_RXD1/ P2_TXD1	I/PU	● RXD [1:0] Pin in RMII MAC Mode, is synchronous to RXC. ● TXD [1:0] Pin in RMII PHY Mode, is synchronous to TXC.
54	M2_RXD0/ P2_TXD0	I/PU	

2.5 High-Speed Serial Interface Pins

Table 6 High-Speed Serial Interface 0 Pins

No.	Pin Name	Type	Description
38	HSON_0	AO	High-Speed Serial Interface 0 Pins: support 3.125GHz or 1.25GHz. Differential serial output interface.
39	HSOP_0	AO	
41	HSIP_0	AI	High-Speed Serial Interface 0 Pins: support 3.125GHz or 1.25GHz. Differential serial input interface.
42	HSIN_0	AI	

Table 7 High-Speed Serial Interface 1 Pins

No.	Pin Name	Type	Description
31	HSON_1	AO	High-Speed Serial Interface 1 Pins: support 3.125GHz or 1.25GHz. Differential serial output interface.
32	HSOP_1	AO	
34	HSIP_1	AI	High-Speed Serial Interface 1 Pins: support 3.125GHz or 1.25GHz. Differential serial input interface.
35	HSIN_1	AI	

2.6 Parallel LED Pins

Table 8 Parallel LED Pins

No.	Pin Name	Type	Description
67	P9LED0	IO/PU	This pin can indicate P9LED0 by software configuration which means extra MAC port 1 LED0.
70	P4LED2/ DIS_SPIS	IO/LI/PU	Default port 4 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
72	P4LED1	IO/PU/OD	Default port 4 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
71	P4LED0/ EEPROM_MOD	IO/LI/PU	Default port 4 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
74	P3LED2/ P8LED0/ EN_PWRLIGHT	IO/LI/PU	Default port 3 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
73	P3LED1	IO/PU/OD	Default port 3 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
75	P3LED0/ EN_SPIF	IO/LI/PU	Default port 3 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
76	P2LED2/ DIS_MCU	IO/LI/PU	Default port 2 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
78	P2LED1	IO/PU	Default port 2 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
77	P2LED0/ DISAUTOLOAD	IO/LI/PU	Default port 2 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
79	P1LED2	IO/PU	Default port 1 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
81	P1LED1	IO/PU/OD	Default port 1 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM

No.	Pin Name	Type	Description
80	P1LED0/ MID29	IO/LI/PU	Default port 1 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
83	P0LED2/ EN_PHY	IO/LI/PU	Default port 0 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
84	P0LED1	IO/PU/OD	Default port 0 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
85	P0LED0/ SMI_SEL	IO/LI/PU	Default port 0 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM

2.7 Serial LED Pins

Table 9 Serial LED Pins

No.	Pin Name	Type	Description
85	LED_CK	IO/LI/PU	Serial Mode LED Clock Signal.
84	LED_DA	IO/PU/OD	Serial Mode LED Data Signal.

2.8 SPI Flash Pins

Table 10 SPI Flash 0 Interface Pins

No.	Pin Name	Type	Description
55	SPF0_CS	IO/PU	SPI Flash 0 chip select signal.
54	SPF0_SO	IO/PU	● In Serial I/O Mode SPI Serial Flash 0 Serial Data Output (YT9215SCH input pin) ● In Dual I/O Mode SPI FLASH 0 bi-directional pin (this is MSB)
50	SPF0_SI	IO/LI/PD	● In Serial I/O Mode SPI Serial Flash 0 Serial Data Input (YT9215SCH output pin) ● In Dual I/O Mode SPI FLASH 0 bi-directional pin (this is LSB)
49	SPF0_SCK	IO/PD	SPI Flash 0 Clock.

Table 11 SPI Flash 1 Interface Pins

No.	Pin Name	Type	Description
81	SPF1_CS	IO/PU	SPI Flash 1 chip select signal.
78	SPF1_SO	IO/PU	● In Serial I/O Mode SPI Serial Flash 1 Serial Data Output (YT9215SCH input pin) ● In Dual I/O Mode SPI Flash 1 bi-directional pin (this is MSB)

79	SPF1_SI	IO/LI/PD	• In Serial I/O Mode SPI Serial Flash 1 Serial Data Input (YT9215SCH output pin) • In Dual I/O Mode SPI Flash 1 bi-directional pin (this is LSB)
83	SPF1_SCK	IO/PD	SPI Flash 1 Clock.

2.9 UART Interface Pins

Table 12 UART 0 Interface Pins

No.	Pin Name	Type	Description
46	UART0_RX	IO/LI/PD	UART RX pin.
47	UART0_TX	IO/LI/PU	UART TX pin.

Table 13 UART 1 Interface Pins

No.	Pin Name	Type	Description
70	UART1_RX	IO/LI/PU	UART RX pin.
76	UART1_TX	IO/LI/PU	UART TX pin.

2.10 Master I2C Interface Pins

Table 14 Master I2C 1 Interface Pins

No.	Pin Name	Type	Description
73	I2C1_SCL	IO/PU/OD	SCL pin in Group1 Master I2C.
72	I2C1_SDA	IO/PU/OD	SDA pin in Group1 Master I2C.

Table 15 Master I2C 2 Interface Pins

No.	Pin Name	Type	Description
84	I2C2_SCL	IO/LI/PU	SCL pin in Group2 Master I2C.
81	I2C2_SDA	IO/PU/OD	SDA pin in Group2 Master I2C.

2.11 Master SMI Interface Pins

Table 16 Master SMI 1 Interface Pins

No.	Pin Name	Type	Description
73	SMI1_MDC	IO/PU/OD	MDC pin in Group1 Master SMI.
72	SMI1_MDIO	IO/PU/OD	MDIO pin in Group1 Master SMI.

Table 17 Master SMI 2 Interface Pins

No.	Pin Name	Type	Description
84	SMI2_MDC	IO/LI/PU	MDC pin in Group2 Master SMI.
81	SMI2_MDIO	IO/PU/OD	MDIO pin in Group2 Master SMI.

2.12 Management Interface Pins

Table 18 Management Interface Pins

No.	Pin Name	Type	Description
90	SSPI_CS	IO/PU	SPI slave Mode Chip Select Input.
91	SCL/ MDC/ SSPI_SCK	IO/PU/OD	● EEPROM auto load mode serial clock output ● I2C slave mode serial clock input ● MDC/MDIO slave mode serial clock input ● SPI slave Mode serial clock input
92	SDA/ MDIO/ SSPI_SI	IO/PU/OD	● EEPROM auto load mode serial data input ● I2C slave mode serial data ● MDC/MDIO slave mode serial data ● SPI slave Mode serial data input
93	SSPI_SO	IO/PU	SPI slave Mode serial data output

2.13 GPIO Pins

Table 19 GPIO Pins

No.	Pin Name	Type	Description
44	GPIO5	IO/PD	General Purpose Input/ Output Interfaces IO5.
46	GPIO6	IO/LI/PD	General Purpose Input/ Output Interfaces IO6.
47	GPIO7	IO/LI/PU	General Purpose Input/ Output Interfaces IO7.
48	GPIO8	IO/LI/PU	General Purpose Input/ Output Interfaces IO8.
49	GPIO9	IO/PD	General Purpose Input/ Output Interfaces IO9.
50	GPIO10	IO/LI/PD	General Purpose Input/ Output Interfaces IO10.
51	GPIO11	IO/LI/PD	General Purpose Input/ Output Interfaces IO11.
52	GPIO12	IO/PU	General Purpose Input/ Output Interfaces IO12.
53	GPIO13	IO/PU	General Purpose Input/ Output Interfaces IO13
54	GPIO14	IO/PU	General Purpose Input/ Output Interfaces IO14.
55	GPIO15	IO/PU	General Purpose Input/ Output Interfaces IO15.
56	GPIO16	IO/PU	General Purpose Input/ Output Interfaces IO16.
57	GPIO17	IO/PU	General Purpose Input/ Output Interfaces IO17.
67	GPIO31	IO/PU	General Purpose Input/ Output Interfaces IO31.
70	GPIO32	IO/LI/PU	General Purpose Input/ Output Interfaces IO32.
71	GPIO33	IO/LI/PU	General Purpose Input/ Output Interfaces IO33.
72	GPIO34	IO/PU/OD	General Purpose Input/ Output Interfaces IO34.

73	GPIO35	IO/PU/OD	General Purpose Input/ Output Interfaces IO35.
74	GPIO36	IO/LI/PU	General Purpose Input/ Output Interfaces IO36.
75	GPIO37	IO/LI/PU	General Purpose Input/ Output Interfaces IO37.
76	GPIO38	IO/LI/PU	General Purpose Input/ Output Interfaces IO38.
77	GPIO39	IO/LI/PU	General Purpose Input/ Output Interfaces IO39.
78	GPIO40	IO/PU	General Purpose Input/ Output Interfaces IO40.
79	GPIO41	IO/PU	General Purpose Input/ Output Interfaces IO41.
80	GPIO42	IO/LI/PU	General Purpose Input/ Output Interfaces IO42.
81	GPIO43	IO/PU/OD	General Purpose Input/ Output Interfaces IO43.
83	GPIO44	IO/LI/PU	General Purpose Input/ Output Interfaces IO44.
84	GPIO45	IO/PU/OD	General Purpose Input/ Output Interfaces IO45.
85	GPIO46	IO/LI/PU	General Purpose Input/ Output Interfaces IO46.
90	GPIO47	IO/PU	General Purpose Input/ Output Interfaces IO47.
91	GPIO48	IO/PU/OD	General Purpose Input/ Output Interfaces IO48.
92	GPIO49	IO/PU/OD	General Purpose Input/ Output Interfaces IO49.
93	GPIO50	IO/PU	General Purpose Input/ Output Interfaces IO50.

2.14 Configuration Pins

Table 20 Configuration Pins

No.	Pin Name	Type	Description
46	SWITCH_ID_1	IO/LI/PD	Switch_ID [1:0] for slave SMI and slave I2C format.
51	SWITCH_ID_0	IO/LI/PD	
49	SPF_MUX_SEL	IO/PD	SPI FLASH Interface Position Select. Pull Up: Select Spi-Flash-0 pin 49\50\54\55. Pull Down: Select Spi-Flash-1 pin 78\79\81\83.
60	EN_SWR	AI	Disable/Enable the internal switching regulator. Pull Down: Disable SWR Pull Up: Enable SWR.
70	DIS_SPIS	IO/LI/PU	Disable Slave SPI Interface for External CPU Access YT9215SCH Register Pull Up: Disable SPI Slave Interface and refer to [STRAP_SMI_SEL] Pull Down: Enable SPI Slave Interface
71	EEPROM_MOD	IO/LI/PU	EEPROM Mode Selection. Pull Up: EEPROM 24Cxx Size greater than 16Kbits (24C32~) Pull Down: EEPROM 24Cxx Size less than or equal to 16Kbit (24C02~24C16).
74	EN_PWRLIGHT	IO/LI/PU	Disable/Enable the LED function When Powered On. Pull Up: Enable LED Pull Down: Disable LED.
75	EN_SPIF	IO/LI/PU	Enable SPI FLASH Interface. Pull Up: Enable the Flash interface Pull Down: Disable Flash interface

No.	Pin Name	Type	Description
76	DIS_MCU	IO/LI/PU	Disable Embedded MCU. Pull Up: Disable embedded MCU upon power on or reset Pull Down: Enable embedded MCU upon power on or reset
77	DISAUTOLOAD	IO/LI/PU	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload upon power on or reset Pull Down: Enable EEPROM autoload upon power on or reset
80	MID29	IO/LI/PU	Slave SMI (MDC/MDIO) Device Address. Pull Up: Slave SMI (MDC/MDIO) Device Address is 0x1d Pull Down: Slave SMI (MDC/MDIO) Device Address is 0x0
83	EN_PHY	IO/LI/PU	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY
85	SMI_SEL	IO/LI/PU	EEPROM SMI/MII Management Interface Selection. Pull Up: EEPROM SMI interface when DIS_SPIS = 1 Pull Down: MII Management interface when DIS_SPIS = 1
47	RESERVED_0	-	Reserved. This pin must be pulled high via an external 4.7kΩ resistor to DVDDIO_1 upon power on.
48	RESERVED_1	-	Reserved. This pin must be pulled high via an external4.7kΩ resistor to DVDDIO_1 upon power on.
50	RESERVED_2	-	Reserved. This pin must be pulled high via an external 4.7kΩ resistor to DVDDIO_1 upon power on.

2.15 Power Related Pins

Table 21 Power Related Pins

No.	Pin Name	Type	Description
68, 82	DVDDIO	P	Digital power.
45, 59	DVDDIO_1	P	Digital power for Extension Port 1.
17, 58, 69	DVDDL	P	Digital power.
10, 16, 18, 28, 86, 94, 104, 114, 118, 128	AVDDH	AP	Analog power.
5, 13, 23, 99, 109, 123	AVDDL	AP	Analog power.
29	SVDDH	AP	SerDes power.
40	SVDDL_0	AP	SerDes power for group 0.
33	SVDDL_1	AP	SerDes power for group 1.
115	PLLVDDL	AP	PLL Power.
11	AGND	AG	Analog GND.
37, 43	SGND_0	AG	SerDes GND.
30, 36	SGND_1	AG	SerDes GND.
117	PLLGND	AG	PLL GND.
129	GND EPAD	G	GND

2.16 Clock Pins

Table 22 Clock Pins

No.	Pin Name	Type	Description
88	XTAL_I	XT	25MHz Crystal Input pin. If use an external oscillator or clock from another device. ● When connecting an external 25MHz oscillator or clock from another device to the XTAL_O pin, XTAL_I must be shorted to GND. ● When connecting an external 25MHz oscillator or clock from another device to the XTAL_I pin, keep the XTAL_O floating.
87	XTAL_O	XT	25MHz Crystal Output pin. If use an external oscillator or clock from another device. ● When connecting an external 25MHz oscillator or clock from another device to the XTAL_O pin, XTAL_I must be shorted to GND. ● When connecting an external 25MHz oscillator or clock from another device to the XTAL_I pin, keep the XTAL_O floating.

2.17 Reset Pins

Table 23 Reset Pins

No.	Pin Name	Type	Description
89	nRESET	AI/PU	Hardware reset, active low. Requires an external pull-up resistor

2.18 Miscellaneous Pins

Table 24 Miscellaneous Pin

No.	Pin Name	Type	Description
12	RBIAS	AO	Bias Resistor. An external 2.49kΩ ± 1% resistor must be connected between the RBIAS pin and GND
14, 15, 116	NC	-	Not connect. Must be left floating in normal operation.

3 Integrated PHY Functional Overview

YT9215SCH integrates five 10/100/1000M Giga PHY ports. Each PHY port supports 1000Base-T, 100Base-TX, and 10Base-Te by four signal pairs, namely MDIAP/N, MDIBP/N, MDICP/N, and MDIDP/N. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. For 1000Base-T, all four pairs are used in both directions at the same time. For 100Base-TX and 10Base-Te, only pairs MDIAP/N and MDIBP/N are used.

3.1 Transmit Encoder Modes

3.1.1 1000BASE-T

In 1000BASE-T mode, the PHY port scrambles data bytes to be transmitted from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5E UTP cable.

3.1.2 100BASE-TX

In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

3.1.3 10BASE-Te

In 10BASE-Te mode, the PHY port transmits Manchester-encoded data.

3.2 Receive Decoder Modes

3.2.1 1000BASE-T

In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately, and data is output to the MAC interfaces.

3.2.2 100BASE-TX

In 100BASE-TX mode, the received data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to MAC interfaces after data stream delimiters have been translated.

3.2.3 10BASE-Te

In 10BASE-Te mode, the recovered 10BASE-Te signal is decoded from Manchester and then aligned.

3.3 Echo Canceller

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as patch panel discontinuity and variations in cable impedance along the twisted pair cable, also result in

drastic SNR degradation on the received signal. The PHY port implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

3.4 NEXT Canceller

The 1000BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled together, significant high-frequency crosstalk occurs between adjacent pairs in the bundle. The PHY port uses three parallel NEXT cancellers on each receive channel to cancel high-frequency crosstalk. The PHY port cancels NEXT by subtracting an estimate of these signals from the equalizer output.

3.5 Baseline Wander Canceller

Baseline wander results from Ethernet links that AC couple to the transceivers and from AC coupling that cannot maintain voltage levels for longer than a short time. As a result, transmitted pulses are distorted, resulting in erroneous sampled values for affected pulses. Baseline wander is more problematic in the 1000BASE-T environment than in 100BASE-TX due to the DC baseline shift in the transmit and receive signals. The YT9215SCH device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

3.7 Auto-Negotiation

The integrated PHY port negotiates its operation mode using the auto-negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto-negotiation supports choosing the mode of operation automatically by comparing its abilities and abilities received from the link partner.

Auto-negotiation is enabled for YT9215SCH by default and can be disabled by software control.

3.8 Auto Crossover and Polarity Correction

The integrated PHY port can detect and correct two types of cable errors: auto crossover of pairs within the UTP cable (between pair 0 and pair 1, and(or) between pair 2 and pair 3) and swapping of polarity within a pair.

4 General Function Description

4.1 Reset

4.1.1 Hardware Reset

YT9215SCH has a hardware reset pin (nRESET) which is low active. The reset signal should be active for at least 10ms. Hardware reset should be applied after power on correctly.

After the reset is released, the YT9215SCH will start the reset initialization procedures by the following steps:

1 All internal logic is reset to a known state, and all register is reset to default value.

2 Latch input value on configuration pins which are used as configuration information to provide flexible applications.

3 Complete the memory BIST process and initialize the packet buffer.

4 Autoload from the EEPROM, or boot from Flash or EEPROM by internal CPU if needed.

4.1.2 Software Reset

The YT9215SCH supports two software resets that can be triggered by programming switch global control register: a chip reset (CHIP_RESET, bit 31 of register 0x8_0000) and a software reset (SW_RESET, bit 1 of register 0x8_0000).

4.1.2.1 CHIP_RESET

The CHIP_RESET is set to 1 to take effect and self-clear. The chip will follow the steps below:

1 All the digital and analog circuits will be reset to default.

2 The packet buffer will be reinitialized and all the Lookup and VLAN tables will be cleared.

3 Autoload from the EEPROM, or boot from Flash or EEPROM by internal CPU if needed, and the chip will be configured again.

4 The integrated PHYs will restart the auto-negotiation process.

4.1.2.2 SW_RESET

The SW_RESET is also set to 1 to take effect and self-clear, and its function is similar to the CHIP_RESET except the analog circuit of integrated PHYs will not be reset.

4.2 Flexible Applications by Configuration Pins

According to the system application, user can select the most suitable mode by configuration pins DISAUTOLOAD, DIS_MCU, EN_SPIF, DIS_SPI and SMI_SEL, shown in the following table.

Table 25 Flexible Applications

DISAUTOLOAD	DIS_MCU	EN_SPIF	DIS_SPI	SMI_SEL	Initial Stage Loading Data*	
					From	To
0	0	0	1	1	EEPROM	RAM
0	0	1	X	X	XIP	

DISAUTOLOAD	DIS_MCU	EN_SPIF	DIS_SPI	SMI_SEL	Initial Stage Loading Data*	
					From	To
0	1	0	X	X	EEPROM	Register
0	1	1	X	X	Flash	RAM
Others					No Action	

Note*: Initial Stage means power on, hardware reset, or software reset.

4.3 IEEE 802.3x Full Duplex Flow Control

YT9215SCH supports IEEE 802.3x flow control in 10/100/1000M full duplex modes. The flow control ability can be decided by the result of Auto-Negotiation or software configuration.

In most cases, MAC ports with integrated PHY get flow control ability by Auto-Negotiation, and two extra MAC ports with MII/RMII/RGMII by software configuration.

4.4 Half Duplex Flow Control

When the PHY port works in 10/100M half-duplex modes, it will collide with the link partner when transmitting and receive data at the same time. Then this will make the buffer overflow and drop packets. YT9215SCH supports two methods (jam mode and defer mode) to avoid this.

The maximum retry count limitation is 16 defined in IEEE 802.3. But for YT9215SCH the retry count limitation is configurable and will not drop packet by default.

4.5 FDB Table

4.5.1 Lookup and Forward

YT9215SCH MAC address table consists of a 4K-entry FDB table. On receiving a packet, YT9215SCH uses DA, and FID to search the 4K-entry FDB table.

- If there is an entry matched, the received packet will be forwarded to the corresponding destination port.
- If there is no entry matched, YT9215SCH can flood the packet according to the VLAN configuration.

4.5.2 MAC Address Learning

When a packet is received, YT9215SCH uses the source MAC address and FID to search the 4K-entry FDB table.

- If there is a match with one of the entries, YT9215SCH will update the entry with new information.
- If there is no matching entry, the packet information is learned into the entry.

4.5.3 MAC Address Aging

The aging mechanism of MAC address is as follows: When a packet flow reaches a port, the port learns the MAC address dynamically.

- If the port keeps receiving this packet flow, the corresponding MAC address is updated continuously and will not be aged.
- If the packet flow stops, the MAC address is deleted after the aging time. The aging time of YT9215SCH is between 5 and 327,675 seconds (typically 300 seconds).

4.6 IVL SVL and IVL/SVL

YT9215SCH supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (Both Independent and Shared VLAN Learning).

4.7 Reserved Multicast Address

YT9215SCH supports the ability to drop/forward/copy IEEE 802.3 specified reserved multicast MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting for these reserved multicast MAC addresses is forwarding. Frames with multicast MAC address 01-80-C2-00-00-01 (802.3x Pause) will always be dropped.

4.8 Storm Control

YT9215SCH supports storm control for broadcast, multicast, and unknown DA, each storm type can be enabled/disabled per port, and default is disabled. If the RX rate of these types of packets exceeds the configured rate, all following storm packets will be dropped. The rate can be configured with packet mode (pps) or byte mode (bps).

4.9 Port Security

YT9215SCH supports the following security mechanism to prevent malicious attacks:

- Per-port enable/disable SA auto-learning
- Per-port enable/disable FDB aging update
- Per-port enable/disable unknown DA packet drop

4.10 MIB

YT9215SCH supports following MIB standards for common management.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

4.11 Port Mirror

YT9215SCH supports 1 group of port mirror for all ports. The TX/RX or both direction packets from each mirrored port can be mirrored to the monitor port.

4.12 VLAN Function

YT9215SCH supports a 4K VLAN table. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs, which also support the IVC (VLAN Translate) function. Ingress-filtering, egress-filtering, and accept-frame-type options provide flexible VLAN configuration:

- Ingress Filtering: Packets from an input port not in the VLAN member will be dropped.
- Egress Filtering: Packets to an output port not in the VLAN member will be dropped.
- Accept Frame Type: the input port can be configured as “Accept All”, “Accept Tagged”, “Accept Untagged”, and “Drop All”.

The packets at the output port can be inserted or removed VLAN tag. For untagged packets, YT9215SCH can insert a VLAN TAG or remove the VLAN TAG from tagged frames.

4.12.1 Port-Based VLAN

The 4K-entry VLAN Table designed into YT9215SCH provides full flexibility for users to configure the input ports to associate with different VLAN entries. Each input port can join with more than one VLAN entry.

Port-based VLAN mapping is the simplest and most effective mapping rule. It defines VLAN members based on device ports. All the packets received from a given input port will be forwarded to this port’s VLAN members.

4.12.2 IEEE 802.1Q Tag-Based VLAN

In 802.1Q VLAN mapping, the device uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. YT9215SCH compares the VID in the VLAN tag with the 4K VLAN Table to determine the packet forwarding action.

4.12.3 Port VID

YT9215SCH supports Port VID (PVID) for each port. When an untagged or priority-tagged packet is forwarded to the output port without hitting other assigned vid rules and the egress tag mode set tagged, the device supports inserting a PVID in the VLAN tag.

4.13 QoS Function

YT9215SCH supports 8 unicast priority queues, 4 multicast priority queues, and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1Q Tag-based priority, VLAN entry-based priority, MAC SA-based priority, MAC DA-based priority, DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in YT9215SCH, the packet’s priority will be assigned based on the priority selection table.

Per-queue in each output port can be set as Strict Priority (SP) or Deficit Weighted Round Robin (DWRR) for the packet scheduling algorithm.

4.13.1 Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, if flow control is enabled, send out a “pause ON” frame; if flow control is disabled, drop the input packet. Per-port input bandwidth control rates can be set from 9Kbps to 2.5Gbps (in 9Kbps steps).

4.13.2 Priority Assignment

Priority assignment specifies the priority of a received packet based on various rules. YT9215SCH can recognize the QoS priority information of receiving packets to give a different service priority.

YT9215SCH identifies the priority of packets based on seven types of QoS priority information:

- Port-based priority
- 802.1Q-based priority
- DSCP-based priority
- ACL-based priority
- VLAN entry-based priority
- MAC SA-based priority
- MAC DA -based priority

4.13.3 Priority Queue Scheduling

The packet scheduler controls the various traffics (control packets sending a sequence of the priority queue), the YT9215SCH scheduling algorithm is Deficit Weighted Round Robin (DWRR), that supports byte-based or packet-based.

In addition, each queue of each port can select Strict Priority or DWRR packet scheduling, and DWRR can co-exist with the SP schedule.

4.13.4 IEEE 802.1Q and DSCP Remarking

YT9215SCH supports the IEEE 802.1Q and DSCP remarking functions. If the remarking function is enabled, when packets egress from one of the 12 queues, the packet’s 802.1Q priority and DSCP can be remarked to a configured value. 802.1Q priority & DSCP value can be remarked based on internal priority.

4.14 IGMP & MLD Snooping Function

YT9215SCH supports hardware IGMPv1/v2/v3 snooping and MLDv1/v2 snooping. These multicast groups are learned and deleted/aged out automatically. For data packets of a known multicast group, YT9215SCH forwards them according to the learned group membership.

YT9215SCH supports bypassing designated IP multicast address with global control and per ingress port join/leave packets allowed control.

YT9215SCH supports IGMP Dynamic Router Port Learning, dynamic router port enable control is based on a per-port basis. The aging time can be configured by SW, the router port will be removed when timeout.

YT9215SCH supports IGMP/MLD Hardware Fast Leave, when left, the multicast group will be marked as invalid again.

YT9215SCH supports IGMP/MLD Packet Copy/Trap/Flood based on global control.

4.15 IEEE 802.1x Function

YT9215SCH supports IEEE 802.1x Port-based.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- Guest VLAN

4.15.1 Port-Based Access Control

Each port of YT9215SCH can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

4.15.2 Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

4.15.3 Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when the port authorization direction is “BOTH”. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

4.15.4 Guest VLAN

When YT9215SCH enables the Port-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, YT9215SCH will drop all packets from this port. If configuring Guest VLAN, YT9215SCH will allow packets from unauthorized ports to be forwarded to a limited VLAN domain.

4.16 Spanning Tree

IEEE 802.1D Spanning Tree allows bridges to prevent and resolve Layer 2 forwarding loops automatically. Switches exchange BPDUs and configuration messages and selectively enable and disable forwarding on specified ports. YT9215SCH supports 16 STP instances and four statuses (Disabled/Blocking/Learning /Forwarding) for each port when the CPU implements the STP/RSTP/MSTP function.

4.17 Embedded RISC-V

A RISC-V MCU is embedded in YT9215SCH to support software management/protocol functions. The RISC-V MCU can transmit to or receive frames from the switch core. The features of the RISC-V MCU are listed below:

- On-chip 64K SRAM
- On-chip 16K boot ROM
- 2K I-Cache
- Up to 8M-Byte serial I/O, dual I/O SPI Flash supported

4.18 Cable Status Diagnostic

Physical layer transceivers of YT9215SCH support the Motorcomm Advanced Cable Status Diagnostic (CSD) feature. Some of the possible problems that can be diagnosed in each differential pair. The results of CSD are summarized as normal, open, and short.

4.19 LED Indicators

The YT9215SCH supports parallel and serial mode LEDs for each port. Each port has three LED indicator pins, LED0, LED1, and LED2. Each LED of each port may have different indicator information defined in Table 26. LED0 default indicates Link/Act, LED1 default indicates 1000M_Link, and LED2 default indicates 100M_Link.

YT9215SCH supports the power-on-blinking feature by the EN_PWRLIGHT pin and software configuration. The LEDs will blink once after reset.

Table 26 LED Definitions

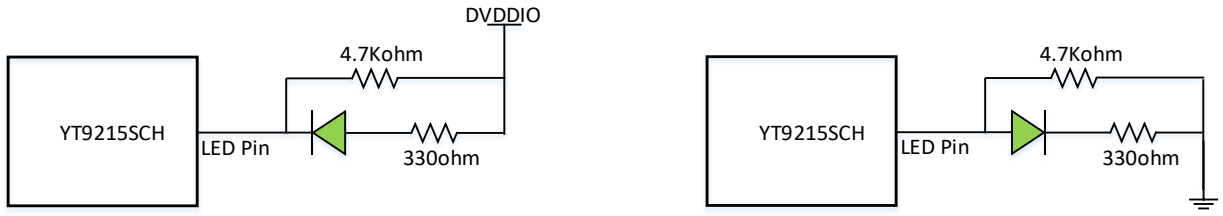
LED Definition	Description
Full	Full Duplex Indicator. LED on when the corresponding port link at full duplex.
Half	Half Duplex Indicator. LED on when the corresponding port link at half duplex.
Link	Link Indicator. LED on when the corresponding port link up.
1000M_Link	1000Mbps Link Indicator. LED on when the corresponding port link at 1000Mbps.
100M_Link	100Mbps Link Indicator. LED on when the corresponding port link at 100Mbps.
10M_Link	10Mbps Link Indicator. LED on when the corresponding port link at 10Mbps.
Act	Activity Indicator. LED blinks when the corresponding port is transmitting or receiving.
1000M_Act	1000Mbps Activity Indicator. LED blinks when the corresponding port link at 1000Mbps and is transmitting or receiving.
100M_Act	100Mbps Activity Indicator. LED blinks when the corresponding port link at 100Mbps and is transmitting or receiving.
10M_Act	10Mbps Activity Indicator. LED blinks when the corresponding port link at 10Mbps and is transmitting or receiving.
TX_Act	TX Activity Indicator. LED blinks when the corresponding port is transmitting.
RX_Act	RX Activity Indicator. LED blinks when the corresponding port is received.
EEE_Act	EEE Mode Indicator. LED blinks when the corresponding port enters EEE mode.
Loop_Act	Loop Detection Indicator. LED blinks when the corresponding port detects a loop.

4.19.1 Parallel LED Mode

In parallel LED mode, each PHY port has three LED indicator pins.

LED signals are active low by default. The LED pins also support hardware configuration functions, so they are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. When the pin input is pulled high upon reset, the pin output is active low for LED function after reset. When the pin input is pulled down upon reset, the pin output is active high for LED function after reset. Typical values for pull-up/pull-down resistors are 4.7kΩ.

Figure 3 Pull-Up and Pull-Down of LED Pins



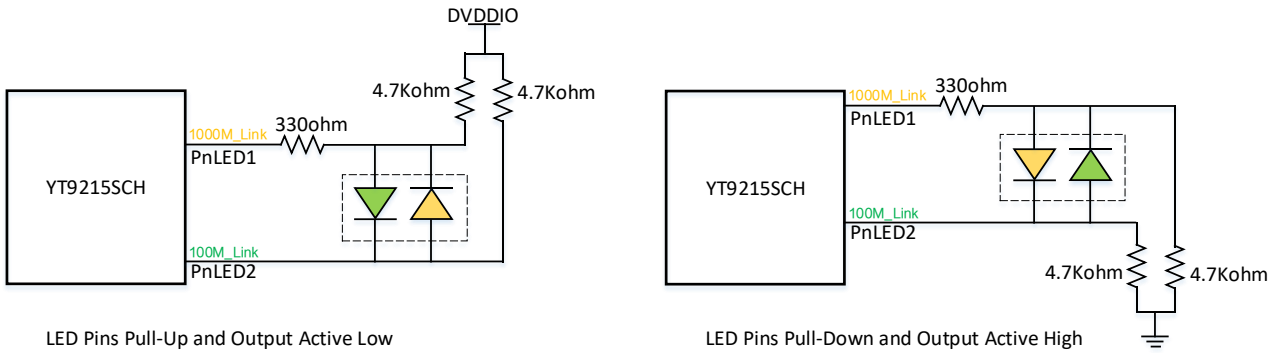
LED Pins Pull-Up and Output Active Low

LED Pins Pull-Down and Output Active High

The LED Pins can also support Bi-color LED applications. Both LED pins connected to the Bi-color LED should have the same polarity active, and the LED definition of both will not appear at the same time.

For example: PnLED1 and PnLED2 will be Pull-Up or Pull-Down together. The PnLED1 definition is 1000M_link. Nevertheless, the PnLED2 definition is 100M_link. PnLED1 and PnLED2 will not be ON at the same time.

Figure 4 Typical Application for Bi-color LED



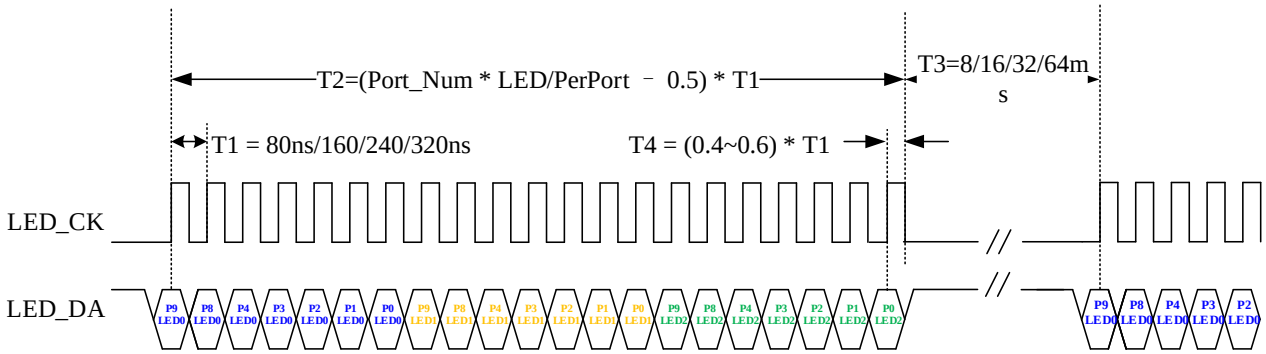
LED Pins Pull-Up and Output Active Low

LED Pins Pull-Down and Output Active High

4.19.2 Serial LED Mode

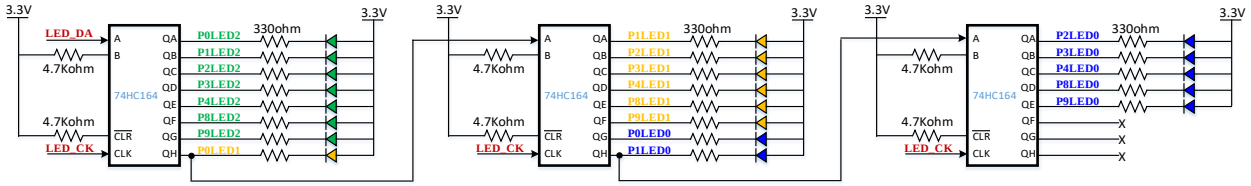
LED_CK and LED_DA pins of the YT9215SCH device are used for the serial LED mode. In this mode, each port supports up to three LED indicators, LED0, LED1, and LED2. If only two LED indicators are needed, LED0 and LED1 will be used. Similarly, LED0 will be used if only one LED indicator is needed.

Figure 5 Serial LED Mode



In this mode, a parallel-out serial shift register device, such as 74HC164, converts LED_CK and LED_DA signals to parallel signals to drive LED indicators. Typical usage is shown in the following diagram.

Figure 6 Typical Usage With 74HC164



4.20 Link Down Power Saving

Physical layer transceivers of YT9215SCH support link-down power saving, also called sleep mode. When the UTP port link down and no signals over the UTP cable for 40 seconds, Physical layer transceivers will enter sleep mode. In this mode, some circuits of physical layer transceivers will be disabled, and the power consumption of the whole chip will be lower.

Once detecting signals over the UTP cable, the physical layer transceiver will exit sleep mode to normal mode.

4.21 Energy Efficient Ethernet

YT9215SCH supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation.

IEEE 802.3az is an extension of the IEEE 802.3 standard. It defines the PHY transceivers to operate in Low Power Idle (LPI) mode which supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY transceiver's circuitry and save power consumption.

When Low Power Idle mode is enabled by MAC and PHY, the YT9215SCH MAC uses Low Power Idle signaling to indicate to the PHY that a period of idle in the data stream is expected. Both local and link partner PHY transceivers may use this information to enter power-saving modes.

4.22 Interrupt Pin for External CPU

The YT9215SCH provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with the mask.

When the port link-up or link-down interrupt mask is enabled, the YT9215SCH will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

5 Interface Descriptions

5.1 SPI Flash Interface

YT9215SCH supports two group SPI flash interfaces. Both support Serial I/O and Dual I/O operation modes, 3-byte address mode access, and up to 8Mbyte size flash. The value of the configuration pin SPF_MUX_SEL upon power on or reset will decide which SPI interface to use. See Table 25 to find out how to decide whether RISC-V MCU works in XIP mode or loads from Flash to RAM.

Figure 7 XIP On Flash

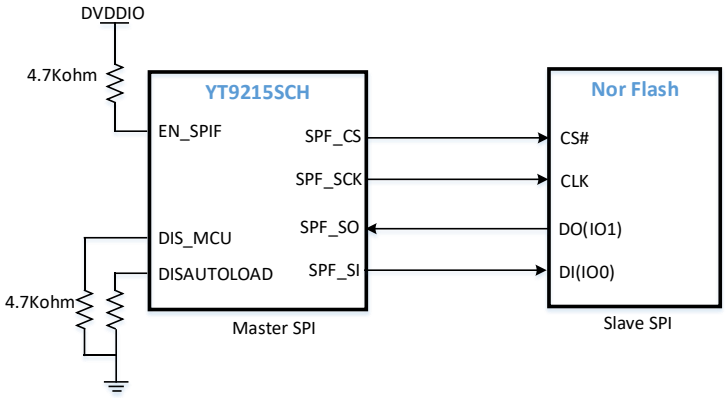
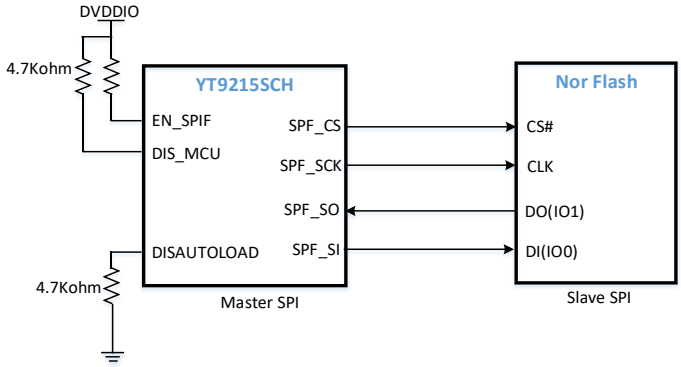


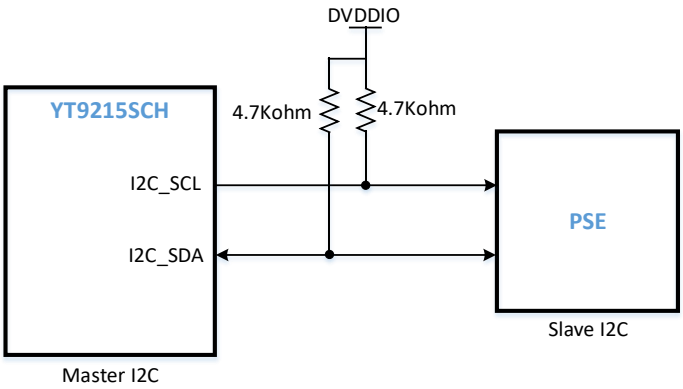
Figure 8 Load From Flash To RAM



5.2 Master I2C Interface

YT9215SCH supports two group Master I2C interfaces to access peripheral slave I2C devices. Due to the I2C interface pins being shared with other functions, it needs to enable the I2C function by software programming. Besides, it should be noted that the type of I2C interface is Open Drain. Pull-Up resistors, for example, 4.7kΩ should be connected to SCL and SDA signals.

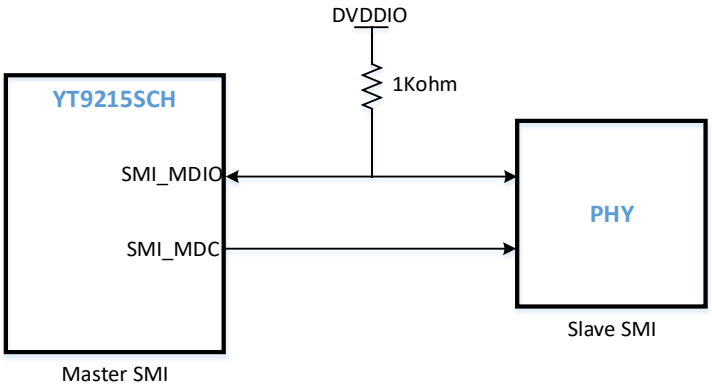
Figure 9 Master I2C Interface Connection Example



5.3 Master SMI Interface

YT9215SCH also supports two group Master Serial Management Interfaces (SMI). The SMI interface supports to access external devices, such as PHY transceivers and is compatible with IEEE 802.3u clause 22 and clause 45. SMI (MDC/MDIO) pins are shared with other features, so it should be enabled by register configuration. MDIO pin type is Open Drain, a Pull-Up resistor, for example, 1kΩ must be connected to the MDIO signal.

Figure 10 Master SMI (MDC/MDIO) Interface Connection Example

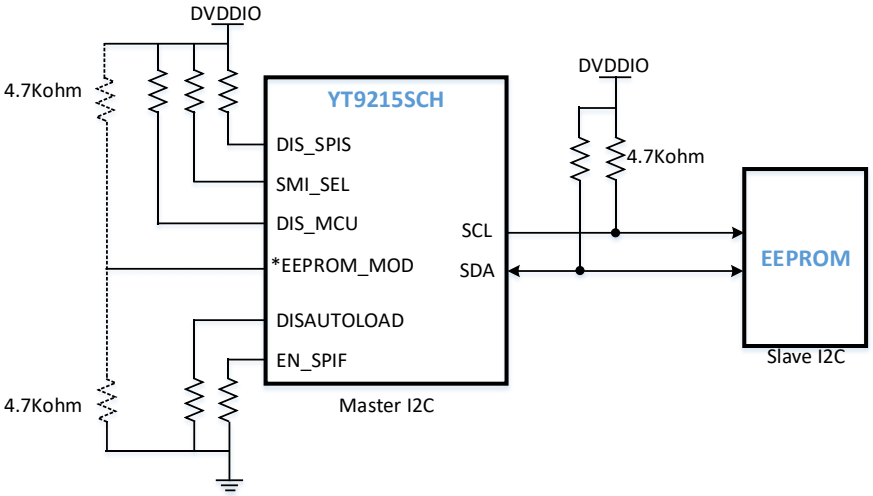


5.4 Master I2C Interface for EEPROM Auto-load

The EEPROM auto-load interface of the YT9215SCH uses the serial bus I2C to read the Serial EEPROM. After YT9215SCH power on or reset, it drives SCL and SDA to read the data from the EEPROM by configuration pins. See Table 18 and Table 25 for more details about the EEPROM auto-load interface.

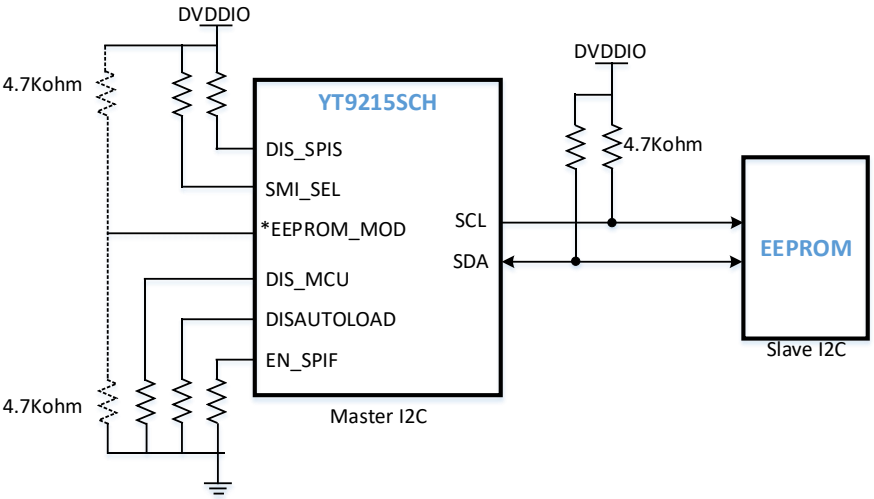
As shown in the following figure, Pull-Up resistors, for example, 4.7kΩ should be connected to SCL and SDA signals.

Figure 11 Auto-load From EEPROM To Register



Note*:
EEPROM_MOD = 0, less than or equal to 16Kbit;
EEPROM_MOD = 1, greater than or equal to 32Kbits;

Figure 12 Auto-load From EEPROM To RAM



Note*:
EEPROM_MOD = 0, less than or equal to 16Kbit;
EEPROM_MOD = 1, greater than or equal to 32Kbits;

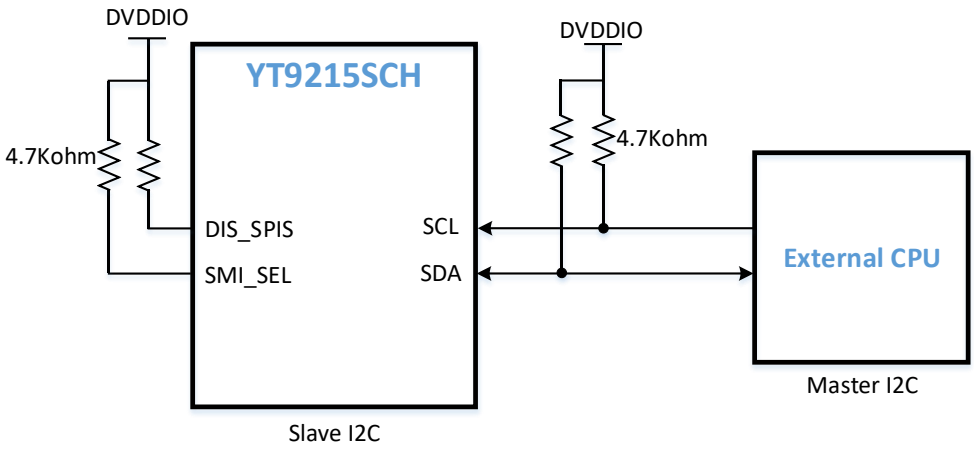
By the size of the word address (1 byte or 2 bytes), EEPROM can be divided into two sizes: 2Kbit~16Kbit and 32Kbit~512Kbit. YT9215SCH supports the two types of EEPROM, and the configuration pin EEPROM_MOD decides which size to be used.

5.5 Management Interfaces

5.5.1 Slave I2C Interface for External CPU

YT9215SCH registers can be accessed via slave I2C interface (SCK and SDA) by an external CPU. The configuration pins DIS_SPIS and SMI_SEL should be high up on power on or reset, to select slave I2C interface.

Figure 13 Slave I2C Interface Connection Example



The slave I2C format is derived from the standard I2C, as shown in the following diagram. Switch_ID[1:0] comes from the configuration pins SWITCH_ID_1 and SWITCH_ID_0. C stands for the even parity check of ADDR[31:2].

- C = 0, if there is an even number of '1' in ADDR[31:2].
- C = 1, if there is an odd number of '1' in ADDR[31:2].

Figure 14 External CPU Write Register into YT9215SCH By Slave I2C

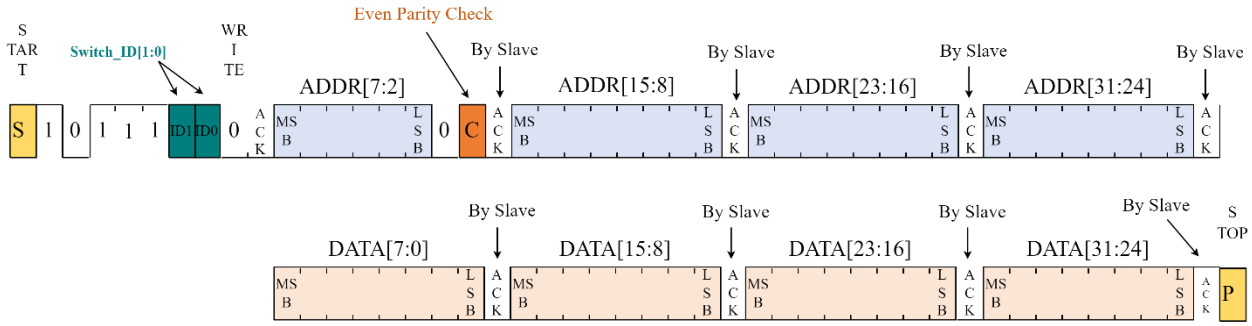
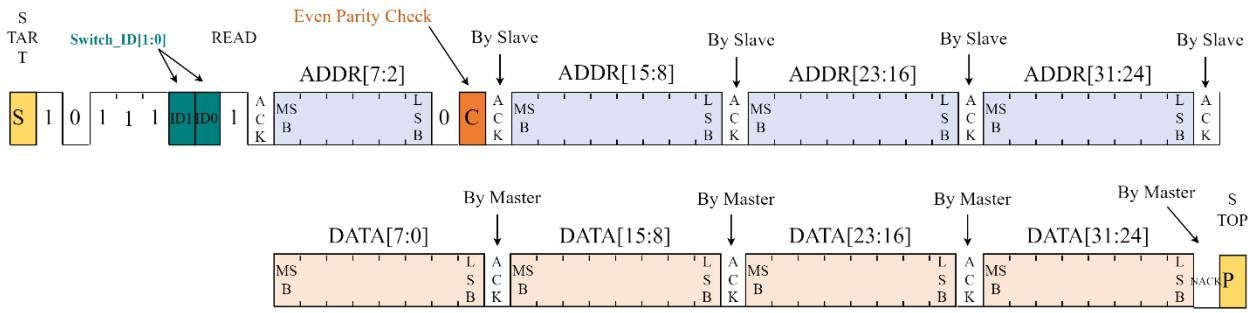


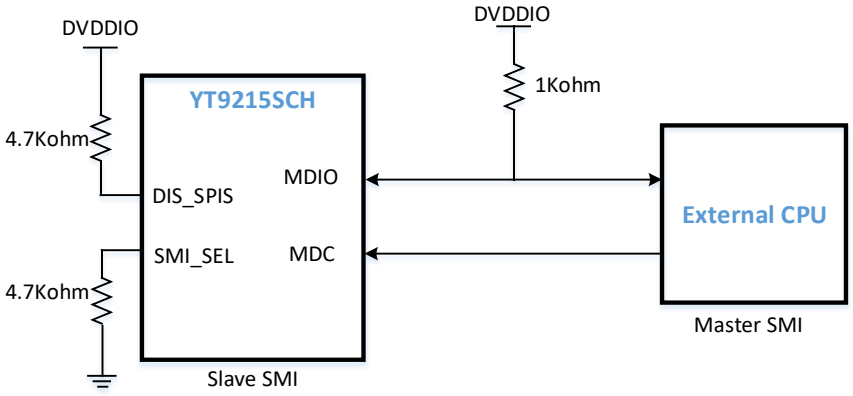
Figure 15 External CPU Read Register from YT9215SCH By Slave I2C



5.5.2 Slave SMI Interface for External CPU

If the configuration pin DIS_SPIS is high and the SMI_SEL is low or high upon power on or reset, the slave SMI (MDC/MDIO) is selected to access YT9215SCH registers.

Figure 16 External CPU Read Register from YT9215SCH By Slave SMI



5.5.3 Slave SPI Interface for External CPU

An SPI-Slave Management Interface can be enabled via configuration pins to access YT9215SCH.

When the CPU writes data to the YT9215SCH internal register via the SPI interface, the first 8-bits is OP code, and the write command OP code is 8h'02.

When the CPU reads data from the YT9215SCH internal register via the SPI interface, the first 8-bits OP code is 8h'03.

Figure 17 External CPU write command frame format

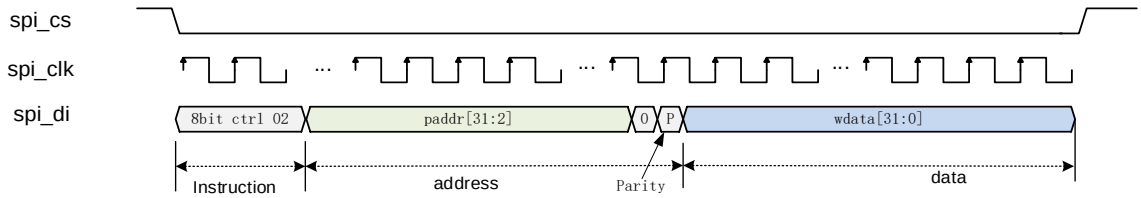
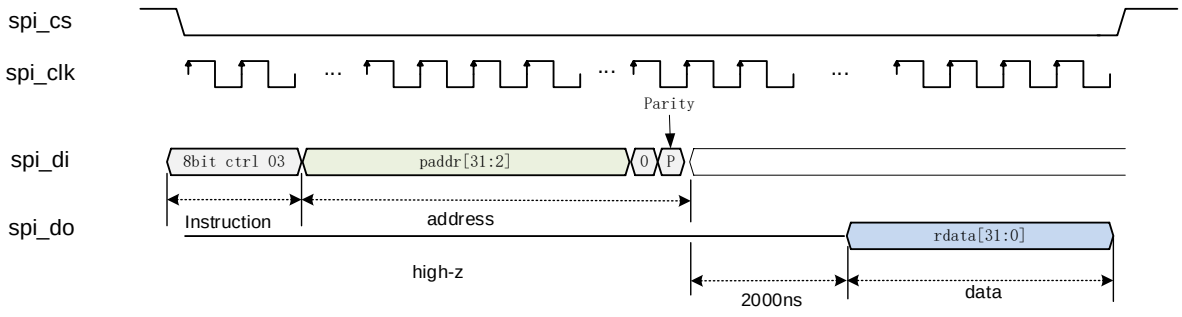


Figure 18 External CPU read command frame format



5.6 General Purpose Interface

The YT9215SCH supports two extension interfaces. The two Extension GMAC (GMAC1 and GMAC2) both support SGMII MAC mode, SGMII PHY mode, 1000Base-X mode, 100Base-FX mode, and 2500Base-X mode via register configuration. GMAC2 also supports RGMII mode, MII MAC mode, MII PHY mode, RMII MAC mode, or RMII PHY mode via register configuration.

5.6.1 Extension Ports SGMII MAC/PHY Mode (10/100/1000Mbps)

The two Extension GMAC (GMAC1 and GMAC2) both support SGMII MAC/PHY interfaces to an external CPU.

5.6.2 Extension Ports Fiber Mode (100FX/1000BX/2500BX)

The two Extension GMAC (GMAC1 and GMAC2) both support Fiber (100FX/1000BX/2500BX) interfaces to an external CPU or optical module.

5.6.3 Extension Ports RGMII Mode (10/100/1000Mbps)

The Extension GMAC2 of the YT9215SCH supports single-port RGMII interfaces to an external CPU.

5.6.4 Extension Ports MII MAC/PHY Mode Interface (10/100Mbps)

The Extension GMAC2 of the YT9215SCH supports MII MAC/PHY mode interfaces to an external CPU.

5.6.5 Extension Ports RMII MAC/PHY Mode Interface (10/100Mbps)

The Extension GMAC2 of the YT9215SCH supports RMII MAC/PHY mode interfaces to an external CPU.

6 Power Requirements

6.1 Power Sequence

Figure 19 Power Sequence Diagram

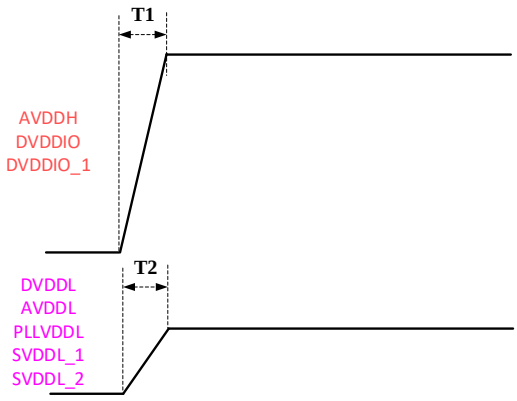


Table 27 Power Sequence Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
T1	Rising time of AVDDH, SVDDH, DVDDIO, DVDDIO_1.	0.5	-	-	ms
T2	Rising time of DVDDL, AVDDL, PLLVDDL, SVDDL_1, SVDDL_2.	0.5	-	15	ms

The requirement for rising time of DVDDL, AVDDL, PLLVDDL, SVDDL_1, SVDDL_2 is only specific to the external power supply.

6.2 Power Consumption

Test Condition: Port 0~4 works as 1000BT. TT IC with AVDDH/DVDDIO/DVDDIO_2 = 3.3V and DVDDL/AVDDL/PLLVDDL = 1.15V at room temperature.

Table 28 YT9215SCH Power Consumption

Condition	AVDDH, SVDDH, DVDDIO, DVDDIO_1 (3.3V)	DVDDL, AVDDL, PLLVDDL, SVDDL_1, SVDDL_2 (1.15V)	Power Consumption (mW)
Link Down	127mA	212mA	662.9
5 UTP Link Up (UTP@1000Mbps)	286mA	582mA	1613.1
5 UTP Traffic (UTP @1000Mbps)	286mA	655mA	1697.05
5 UTP + 1 RGMII Traffic (UTP/RGMII@1000Mbps)	286mA	666mA	1709.7
5 UTP + 1 RGMII + 1 Serdes (1G) Traffic (UTP/RGMII/Serdes @1000Mbps)	306mA	717mA	1834.35
5 UTP + 2 Serdes Traffic	330mA	784mA	1990.6

Condition	AVDDH, SVDDH, DVDDIO, DVDDIO_1 (3.3V)	DVDDL, AVDDL, PLLVDDL, SVDDL_1, SVDDL_2 (1.15V)	Power Consumption (mW)
(UTP@1000Mbps Serdes@2500Mbps)			

6.3 Power Ripple

The AVDDH/DVDDIO/DVDDIO_1 supply ripple should be under 100mV. The DVDDL ripple should be under 80mV, and the AVDDL, SVDDL_1, SVDDL_2, and PLLVDDL ripple should be under 50mV.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 29 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO, AVDDH, SVDDH_1, SVDDH_2, DVDDIO_1, Supply Referenced to GND and AGND	GND-0.3	+3.70	V
DVDDL, AVDDL, PLLVDDL, SVDDL_1, SVDDL_2, Supply Referenced to GND, AGND, and PLLGND	GND-0.3	+1.40	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

7.2 Recommended Operating Range

Table 30 Recommended Operating Range

Parameter		Min	TYP	Max	Units
Ambient Operating Temperature (Ta)		-40	-	85	°C
AVDDH Supply Voltage Range		3.135	3.3	3.63	V
DVDDIO Supply Voltage Range	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
DVDDIO_1 Supply Voltage Range (DVDDIO_1: Extension Port 1 Supports 1.8V, 2.5V, 3.3V)	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
	1.8V	1.62	1.8	1.98	V
DVDDL, AVDDL, PLLVDDL, SVDDL_1, SVDDL_2 Supply Voltage Range		1.08	1.15	1.32	V

7.3 DC Characteristics

Table 31 DC Characteristics

Symbol	Description	Min	Typ	Max	Unit
Voh (3.3V)	Minimum High Level Output Voltage	2.4	-	3.63	V
Vol (3.3V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Vih (3.3V)	Minimum High Level Input Voltage	2	-	-	V
Vil (3.3V)	Maximum Low Level Input Voltage	-	-	0.8	V
Voh (2.5V)	Minimum High Level Output Voltage	2	-	2.8	V
Vol (2.5V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Vih (2.5V)	Minimum High Level Input Voltage	1.7	-	-	V
Vil (2.5V)	Maximum Low Level Input Voltage	-	-	0.7	V

Symbol	Description	Min	Typ	Max	Unit
Voh (1.8V)	Minimum High Level Output Voltage	1.62	-	2.1	V
Vol (1.8V)	Maximum Low Level Output Voltage	-0.3	-	0.4	V
Vih (1.8V)	Minimum High Level Input Voltage	1.2	-	-	V
Vil (1.8V)	Maximum Low Level Input Voltage	-	-	0.5	V

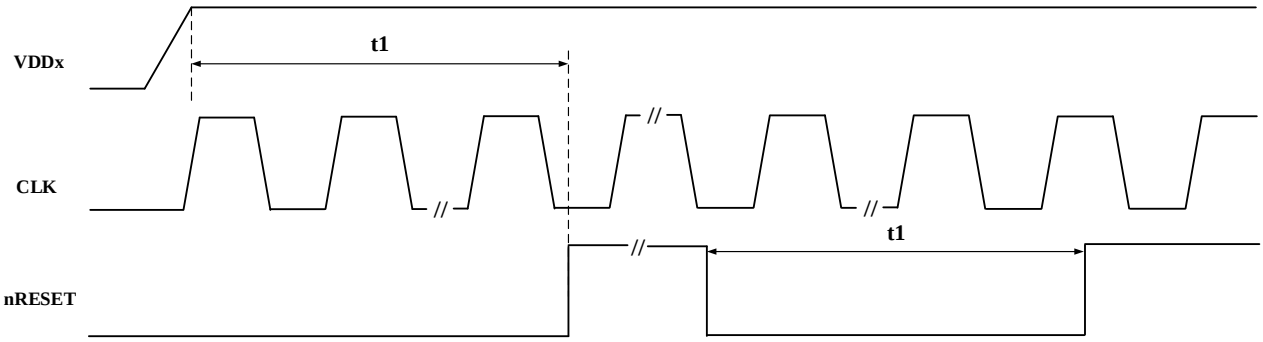
7.4 AC Characteristics

7.4.1 Reset Timing

Table 32 Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
t1	The duration from all powers is steady to nRESET de-asserted, or the nRESET assertion time after power up.	10	-	-	ms

Figure 20 Reset Timing Diagram



7.4.2 SPI Flash Interface Timing Characteristics

Figure 21 SPI Flash Interface Timing

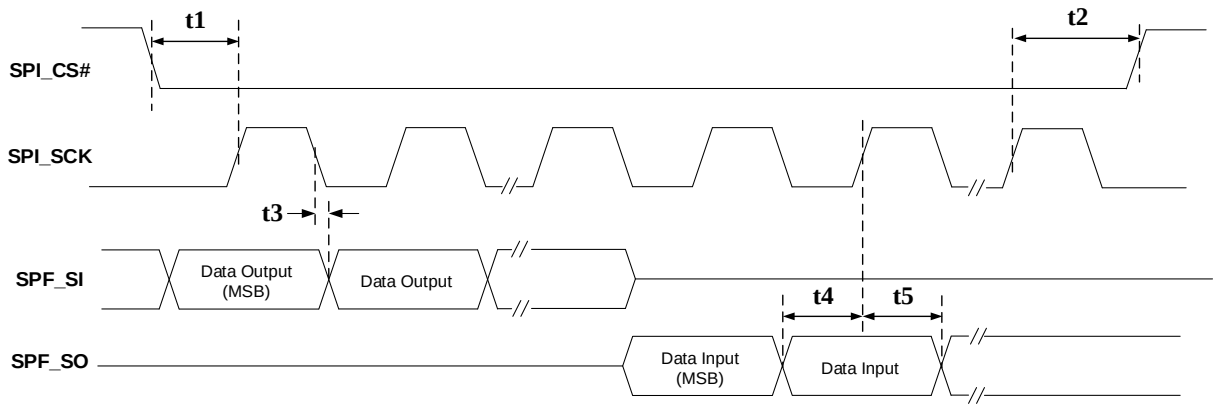


Table 33 SPI Flash Interface Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
Freq	Clock Frequency of SPI_SCK	-	31.25	-	MHz
t1	SPI_CS# Active Setup Time relative to SPI_SCK	20	-	-	ns
t2	SPI_CS# Not Active Hold Time relative to SPI_SCK	80	-	-	ns
t3	SPI_SI Output Valid Time	0	-	15	ns
t4	SPI_SO Input Setup Time	2	-	-	ns
t5	SPI_SO Input Hold Time	0	-	-	ns

7.4.3 Master I2C Timing Characteristics

Figure 22 Master I2C Timing

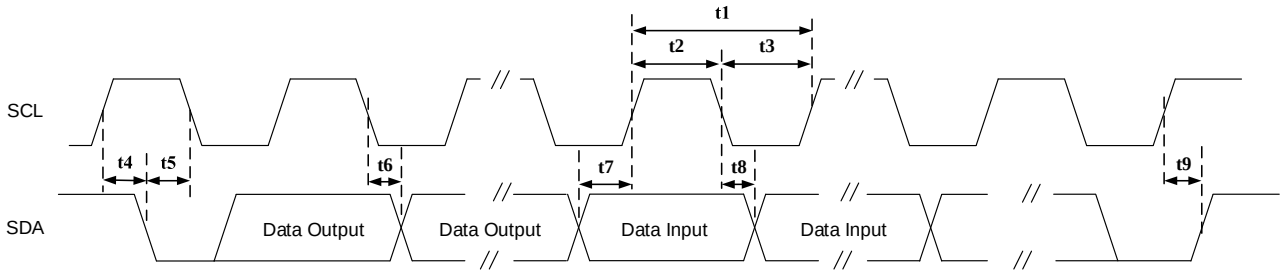


Table 34 Master I2C Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
Freq	Clock Frequency of SCL	-	100	1000	KHz
t1	SCL Clock Period	1	10	-	μs
t2	SCL High Time	0.3*t1	0.5*t1	-	μs
t3	SCL Low Time	0.3*t1	0.5*t1	-	μs
t4	START Setup Time	0.25*t1	-	-	μs
t5	START Hold Time	0.25*t1	-	-	μs
t6	SCL Low to Data Output Valid	0.1*t1	-	0.2*t1	μs
t7	Data Input Setup Time	0	-	-	ns
t8	Data Input Hold Time	200	-	-	ns
t9	Stop Setup Time	0.3*t1	-	-	μs

7.4.4 Master SMI Timing Characteristics

Figure 23 Master SMI Timing

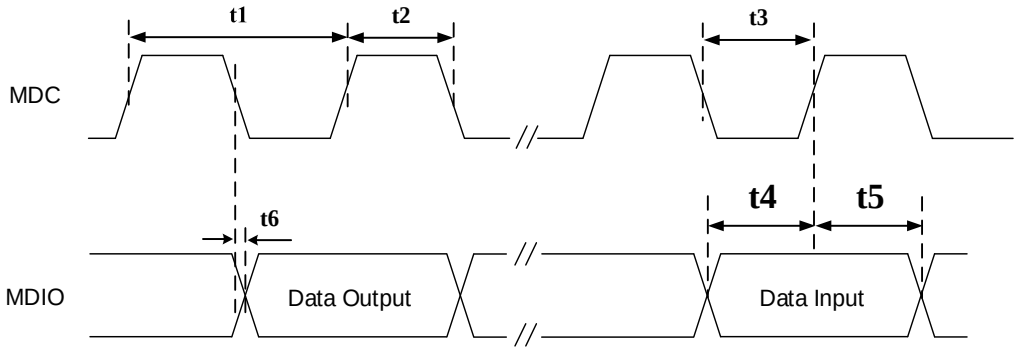


Table 35 Master SMI Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
t1	MDC Clock Period	250*	-	-	ns
t2	MDC High Time	100	-	-	ns
t3	MDC Low Time	100	-	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC falling edge (Data Output)	5	-	50*	ns

Note*: The MDIO pin type is Open Drain when working as Master SMI interface. Therefore, the minimum value of t1 and the maximum value of t6 depend on the value of the pull-up resistor on the MDIO signal. Parameters in Table 35 are the result under the condition of a pull-up 1kΩ resistor.

7.4.5 Master I2C for EEPROM Auto-load Timing Characteristics

Figure 24 Master I2C for EEPROM Auto-load Timing

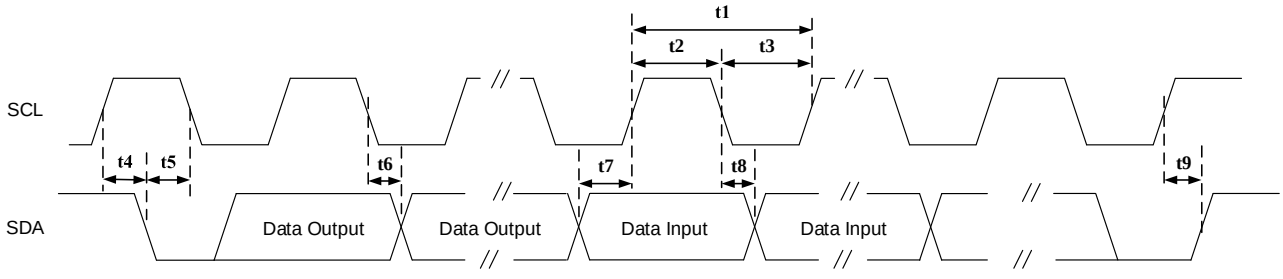


Table 36 Master I2C for EEPROM Auto-load Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
Tfreq	SCL Clock Frequency	-	100	800	KHz
t1	SCL Clock Period	1.25	10	-	μs
t2	SCL High Time	0.3*t1	0.5*t1	-	μs
t3	SCL Low Time	0.3*t1	0.5*t1	-	μs

Symbol	Description	Min	Typ	Max	Unit
t4	START Setup Time	0.25*t1	-	-	μs
t5	START Hold Time	0.25*t1	-	-	μs
t6	SCL Low to Data Output Valid	0.1*t1	-	0.2*t1	μs
t7	Data Input Setup Time	0	-	-	ns
t8	Data Input Hold Time	0	-	-	ns
t9	Stop Setup Time	0.3*t1	-	-	μs

7.4.6 Slave I2C Timing Characteristics

Figure 25 Slave I2C Timing

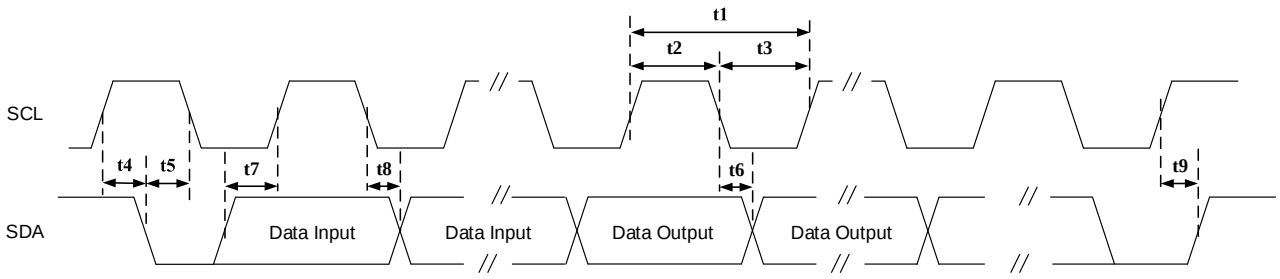


Table 37 Slave I2C Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
Tfreq	SCL Clock Frequency	-	-	400	KHz
t1	SCL Clock Period	2.5	-	-	μs
t2	SCL High Time	0.8		-	μs
t3	SCL Low Time	0.8		-	μs
t4	START Setup Time	0.3	-	-	μs
t5	START Hold Time	0.3	-	-	μs
t6	SCL Low to Data Output Valid	0.1	-	0.3	μs
t7	Data Input Setup Time	0	-	-	ns
t8	Data Input Hold Time	200	-	-	ns
t9	Stop Setup Time	0.3	-	-	μs

7.4.7 Slave SMI Timing Characteristics

Figure 26 Slave SMI Timing

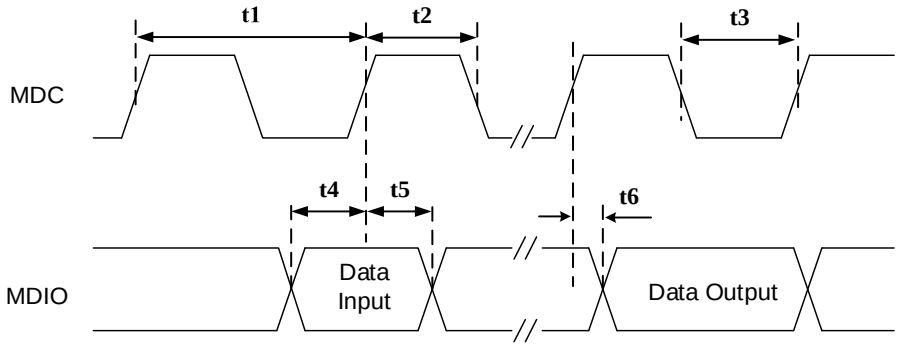


Table 38 Slave SMI Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
t1	MDC Clock Period	250*	-	-	ns
t2	MDC High Time	80	-	-	ns
t3	MDC Low Time	80	-	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC rising edge (Data Output)	5	-	125*	ns

Note*: The MDIO pin type is Open Drain when working as a slave SMI interface. Therefore, the minimum value of t1 and the maximum value of t6 depend on the value of the pull-up resistor on the MDIO signal. Parameters in Table 38 are the result under the condition of a pull-up 1kΩ resistor.

7.4.8 Slave SPI Timing Characteristics

Figure 27 Slave SPI Interface Timing

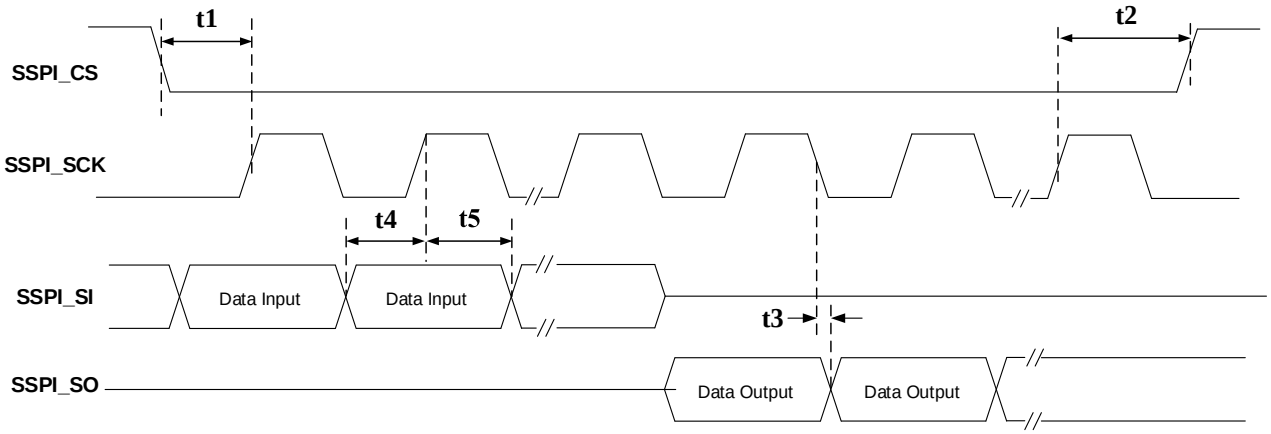


Table 39 Slave SPI Interface Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
Freq	Clock Frequency of SPI_SCK	-	-	5	MHz
t1	SSPI_CS# Active Setup Time relative to SPI_SCK	50			ns
t2	SSPI_CS# Not Active Hold Time relative to SPI_SCK	50			ns
t3	SSPI_SO Output Valid Time	0	-	80	ns
t4	SSPI_SI Input Setup Time	40	-	-	ns
t5	SSPI_SI Input Hold Time	40	-	-	ns

7.4.9 RGMII Timing W/O Delay

Figure 28 RGMII Timing W/O Delay

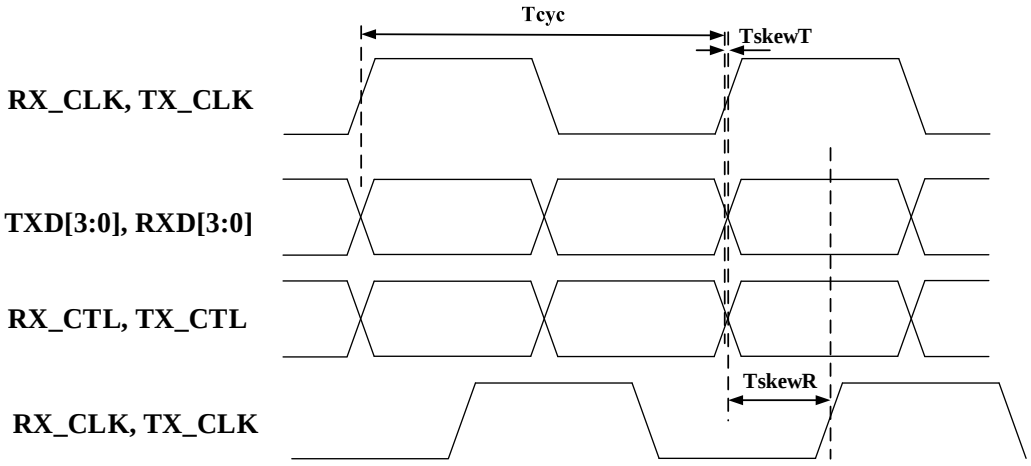


Table 40 RGMII Timing W/O Delay

Symbol	Description	Min	Typ	Max	Unit
TskewT	Data to clock output skew (at Transmitter)	-500	0	500	ps
TskewR	Data to clock output skew (at Receiver)	1	1.5	2.0	ns
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100T	40	50	60	%

7.4.10 RGMII Timing with Internal Delay

Figure 29 RGMII Timing with Internal Delay

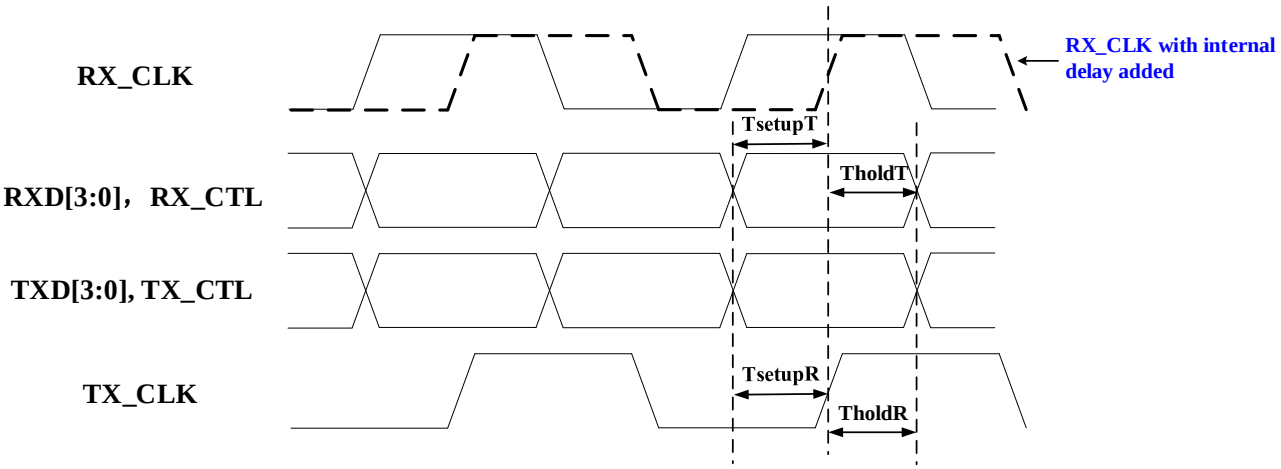


Table 41 RGMII Timing with internal delay

Symbol	Description	Min	Typ	Max	Unit
TsetupT	Data to Clock output Setup Time (at Transmitter integrated delay)	1.0	2.0	-	ns
TholdT	Clock to Data output Hold Time (at Transmitter integrated delay)	1.0	2.0	-	ns
TsetupR	Data to Clock input Setup Time (at Receiver integrated delay)	1.0	2.0	-	ns
TholdR	Data to Clock input Hold Time (at Receiver integrated delay)	1.0	2.0	-	ns

7.4.11 2500Base-X Characteristics

Table 42 2500Base-X Differential Transmitter Characteristics

Parameter		SYM	Min	Typ	Max	Unit	Note
Unit Interval		UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask		T_X1	-	-	0.2	UI	-
Eye Mask		T_X2	-	-	0.4	UI	-
Eye Mask		T_Y1	150	-	-	mV	-
Eye Mask		T_Y2	-	-	500	mV	-
Output Differential Voltage		$V_{TX-DIFF_{P-P}}$	350	500	900	mV	-
Output Jitter	TJ	$T_{TX-Jitter}$	-	-	0.3	UI	$T_{TX\text{-}JITTER\text{-}MAX}$ = 1 - $T_{TX\text{-}EYE\text{-}MIN}$ = 0.30UI
	DJ		-	-	0.165	UI	-
Minimum TX Eye Width		T_{TX-EYE}	0.7	-	-	UI	-
Output Rise Time		$T_{TX-Rise}$	0.125	-	-	UI	20%-80%
Output Fall Time		$T_{TX-Fall}$	0.125	-	-	UI	20%-80%
Output Differential Impendence		R_{TX}	80	100	120	Ω	-

Parameter	SYM	Min	Typ	Max	Unit	Note
AC Coupling Capacitor	C_{TX}	80	100	200	nF	-
Transmit Length in PCB	L_{TX}	-	-	15(*Note1)	inch	-

Note 1: If multiple SerDes mode is used in the system, the shortest trace allowed should be used on board.

Figure 30 2500Base-X Differential Transmitter Eye Diagram

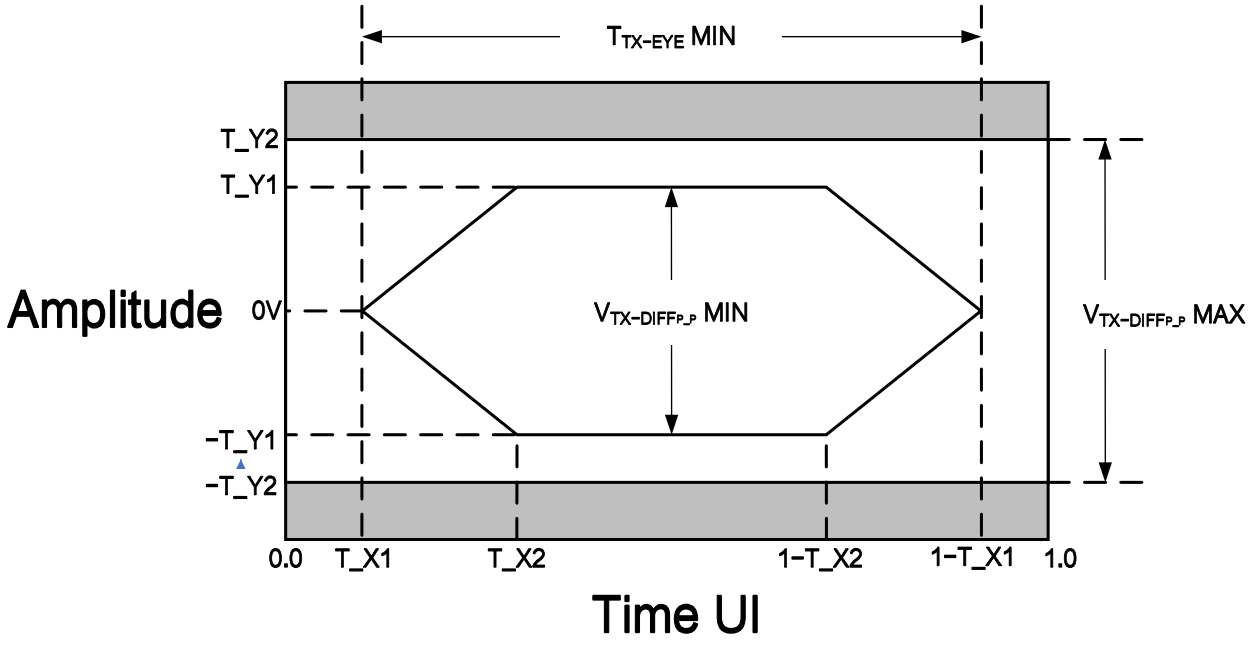
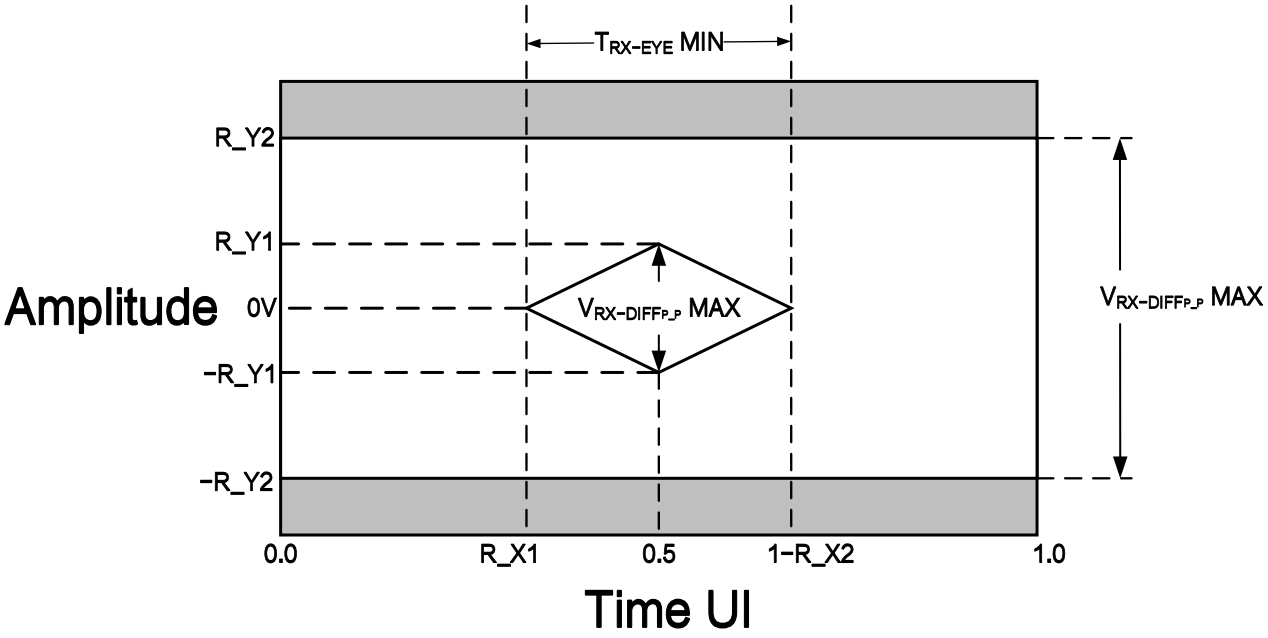


Table 43 2500Base-X Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask	R_X1	-	-	0.3	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	550	mV	-
Input Differential Voltage	$V_{RX-DIFF_{P-P}}$	200	-	1100	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-Jitter}$	-	-	0.6	UI	$T_{RX\text{-}JITTER\text{-}MAX} = 1 - T_{RX\text{-}EYE\text{-}MIN} = 0.6UI$
Input Differential Impendence	R_{RX}	80	100	120	Ω	-

Figure 31 2500Base-X Differential Receiver Eye Diagram



7.4.12 SGMII Characteristics

Table 44 SGMII Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mv	-
Eye Mask	T_Y2	-	-	500	mv	-
Output Differential Voltage	$V_{TX-DIFF_{P-P}}$	350	500	900	mv	-
Minimum TX Eye Width	T_{TX-EYE}	0.7	-	-	UI	-
Output Jitter	$T_{TX-Jitter}$	-	-	0.3	UI	$T_{TX-JITTER-MAX}$ = 1 - $T_{TX-EYE-MIN}$ = 0.30UI
Data Dependent Jitter		-	70	-	ps	-
Output Rise Time	$T_{TX-Rise}$	100	-	200	ps	20%-80%
Output Fall Time	$T_{TX-Fall}$	100	-	200	ps	20%-80%
Output Differential Impendence	R_{TX}	80	100	120	Ω	-
AC Coupling Capacitor	C_{TX}	80	100	200	nF	-
Transmit Length in PCB	L_{TX}	-	-	30(*Note1)	inch	-

Note 1: If multiple SerDes mode is used in the system, the shortest trace allowed should be used on board.

Figure 32 SGMII Differential Transmitter Eye Diagram

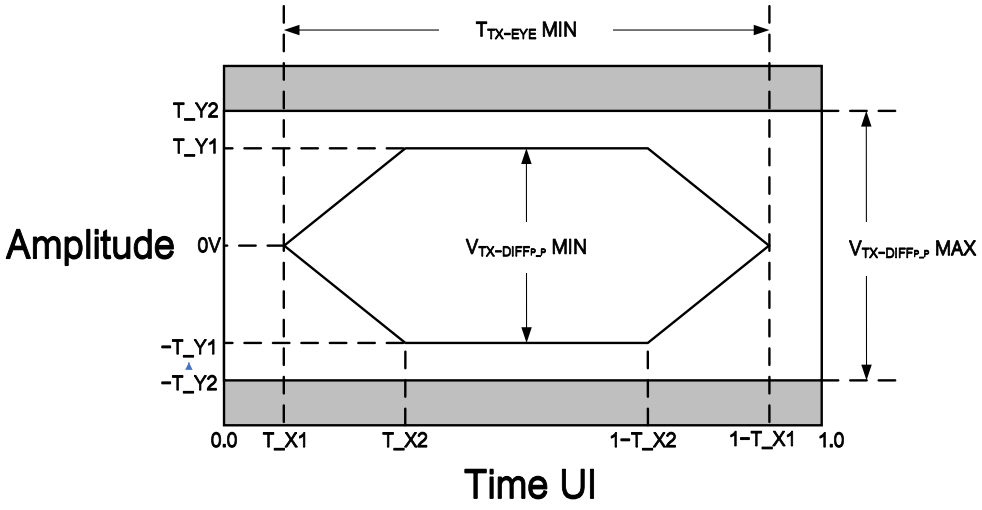
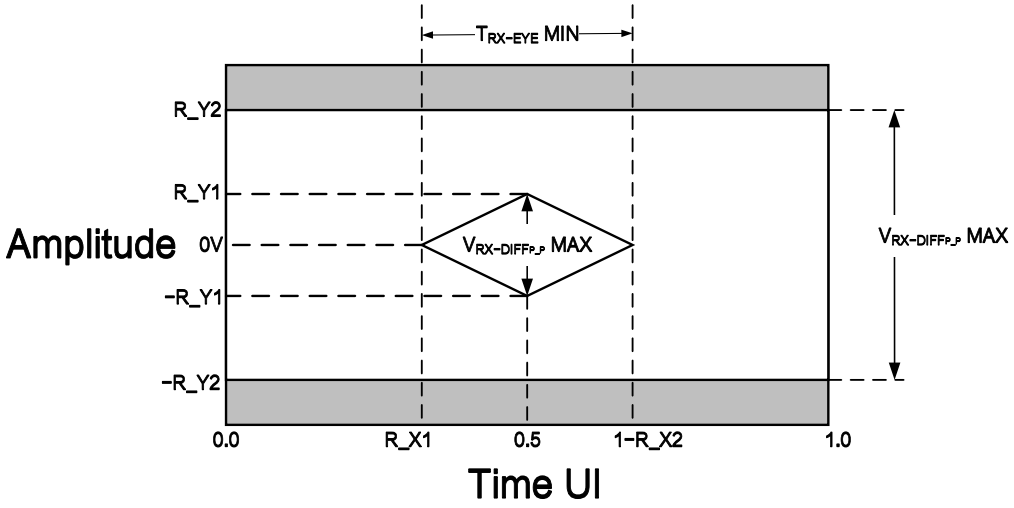


Table 45 SGMII Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	R_X1	-	-	0.3	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	550	mV	-
Input Differential Voltage	$V_{RX-DIFF_{P-P}}$	200	-	1100	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-Jitter}$	-	-	0.6	UI	$T_{RX\text{-}JITTER\text{-}MAX} = 1 - T_{RX\text{-}EYE\text{-}MIN} = 0.6UI$
Input Differential Impendence	R_{RX}	80	100	120	Ω	-

Figure 33 SGMII Differential Receiver Eye Diagram



7.4.13 1000Base-X Characteristics

Table 46 1000Base-X Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mv	-
Eye Mask	T_Y2	-	-	500	mv	-
Output Differential Voltage	$V_{TX-DIFF_{P-P}}$	350	500	900	mv	-
Minimum TX Eye Width	T_{TX-EYE}	0.7	-	-	UI	-
Output Jitter	$T_{TX-Jitter}$	-	-	0.3	UI	$T_{TX\text{-}JITTER\text{-}MAX}$ = 1 - $T_{TX\text{-}EYE\text{-}MIN}$ = 0.30UI
Output Rise Time	$T_{TX-Rise}$	0.075	-	-	UI	20%-80%
Output Fall Time	$T_{TX-Fall}$	0.075	-	-	UI	20%-80%
Output Impendence	R_{TX}	80	100	120	Ω	-
AC Coupling Capacitor	C_{TX}	80	100	200	nF	-
Transmit Length in PCB	L_{TX}	-	-	30(*Note1)	inch	-

Note 1: If multiple SerDes mode is used in the system, the shortest trace allowed should be used on board.

Figure 34 1000Base-X Differential Transmitter Eye Diagram

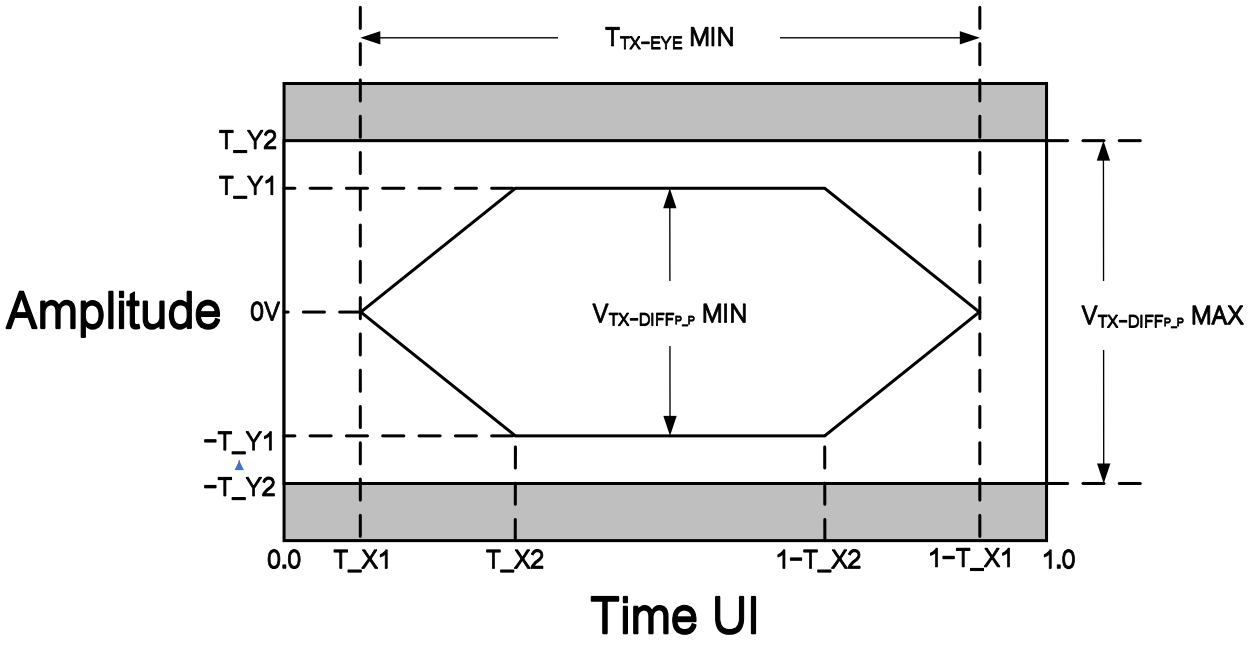
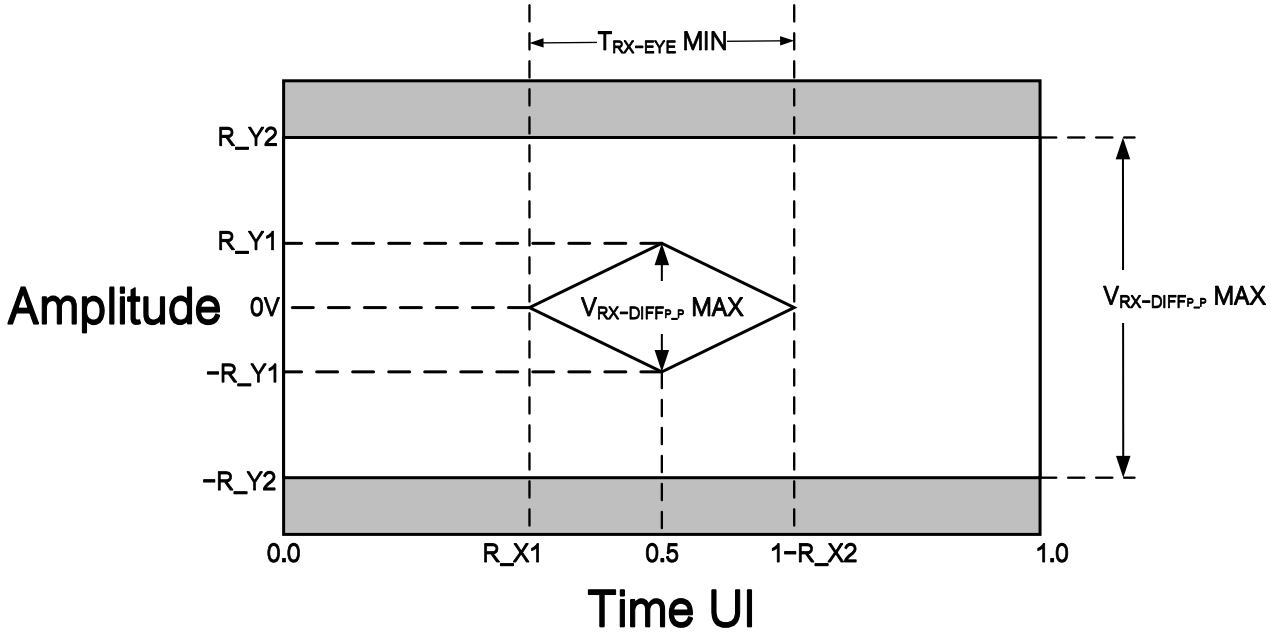


Table 47 1000Base-X Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm

Parameter	SYM	Min	Typ	Max	Unit	Note
Eye Mask	R_X1	-	-	0.3	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	550	mV	-
Input Differential Voltage	$V_{RX-DIFF_{P-P}}$	200	-	1100	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-Jitter}$	-	-	0.6	UI	$T_{RX\text{-}JITTER\text{-}MAX}$ = 1 – $T_{RX\text{-}EYE\text{-}MIN}$ = 0.6UI
Input Differential Impendence	R_{RX}	80	100	120	Ω	-

Figure 35 1000Base-X Differential Receiver Eye Diagram



7.4.14 100Base-FX Characteristics

Table 48 100Base-FX Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	7.9976	8	8.0024	ns	8ns ± 300ppm
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mv	-
Eye Mask	T_Y2	-	-	500	mv	-
Output Differential Voltage	$V_{TX-DIFF_{P-P}}$	350	500	900	mv	-
Minimum TX Eye Width	T_{TX-EYE}	0.7	-	-	UI	-
Output Jitter	$T_{TX-Jitter}$	-	-	0.3	UI	$T_{TX\text{-}JITTER\text{-}MAX}$ = 1 - $T_{TX\text{-}EYE\text{-}MIN}$ = 0.30UI
Output Rise Time	$T_{TX-Rise}$	0.075	-	-	UI	20%-80%
Output Fall Time	$T_{TX-Fall}$	0.075	-	-	UI	20%-80%

Parameter	SYM	Min	Typ	Max	Unit	Note
Output Impendence	R_{TX}	80	100	120	Ω	-
AC Coupling Capacitor	C_{TX}	80	100	200	nF	-
Transmit Length in PCB	L_{TX}	-	-	30(*Note1)	inch	-

Note 1: If multiple SerDes mode is used in the system, the shortest trace allowed should be used on board.

Figure 36 100Base-FX Differential Transmitter Eye Diagram

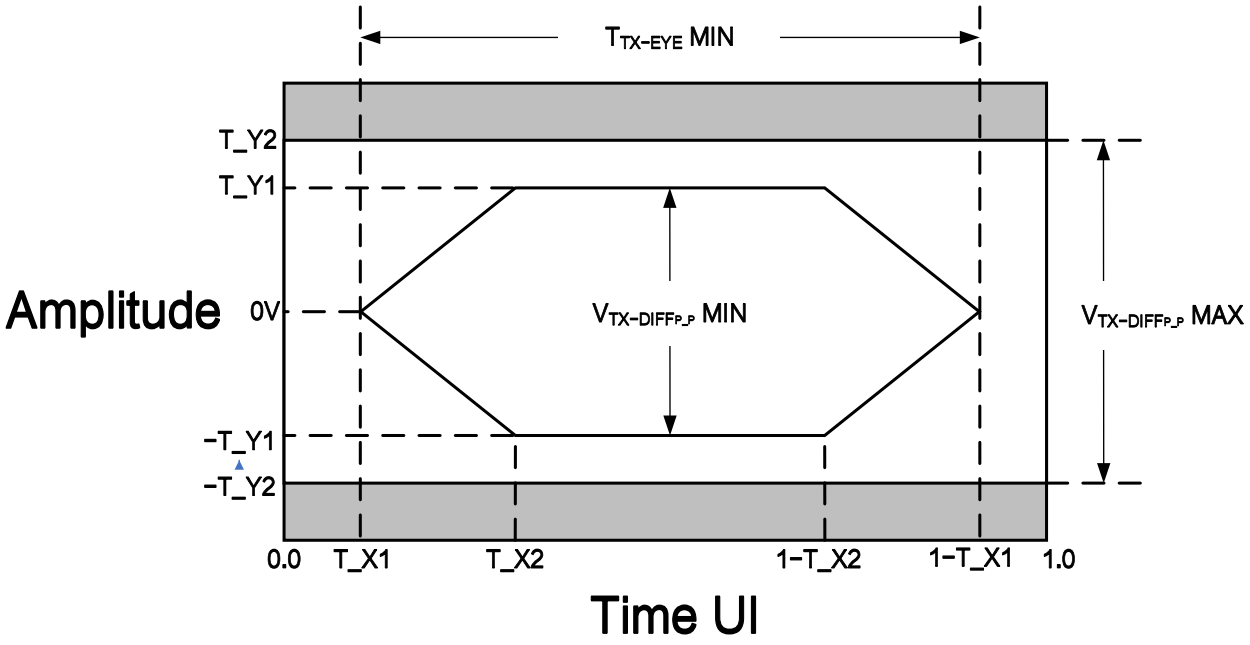
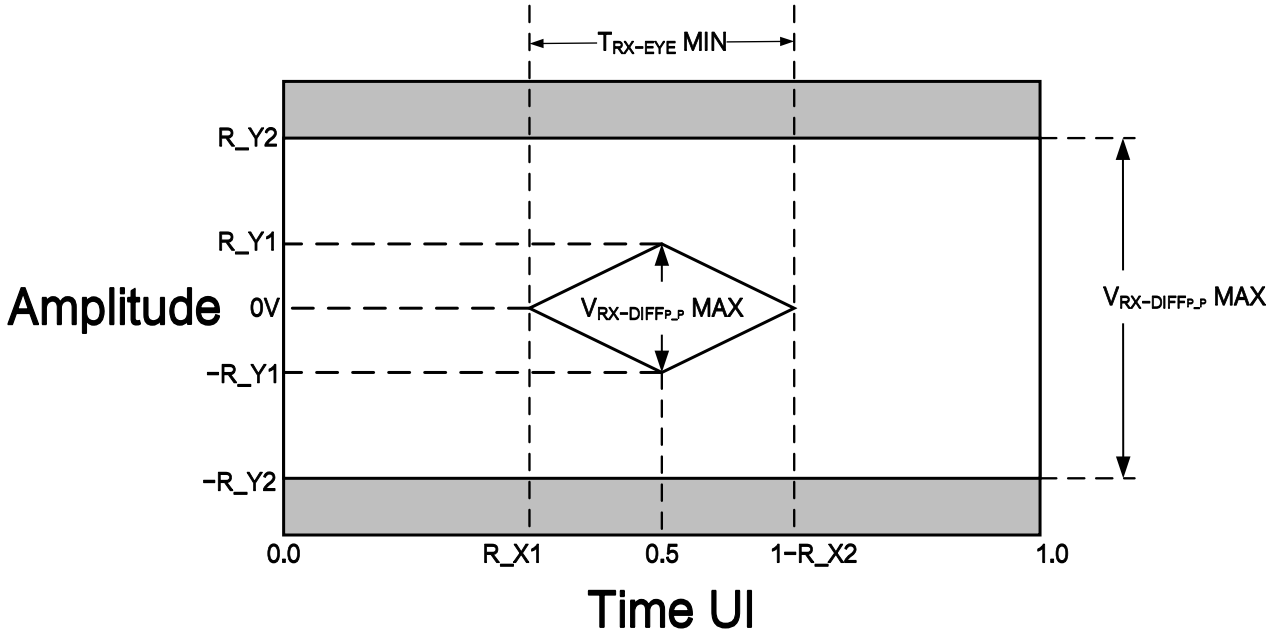


Table 49 100Base-FX Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	7.9976	8	8.0024	ns	8ns ± 300ppm
Eye Mask	R_X1	-	-	0.3	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	550	mV	-
Input Differential Voltage	$V_{RX-DIFF_{P-P}}$	200	-	1100	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-Jitter}$	-	-	0.6	UI	$T_{RX\text{-}JITTER\text{-}MAX} = 1 - T_{RX\text{-}EYE\text{-}MIN} = 0.6UI$
Input Differential Impendence	R_{RX}	80	100	120	Ω	-

Figure 37 100Base-FX Differential Receiver Eye Diagram



7.5 Crystal Requirement

Table 50 Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Parallel Resonant Crystal Reference Frequency	-	25	-	MHz
Fref Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-50	-	50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	Ω
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high-level	1.4	-	-	V
Vil	Crystal output low-level	-	-	0.7	V

7.6 Oscillator/External Clock Requirement

Table 51 Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency	-	25	-	MHz
Frequency Tolerance	-50	-	50	PPM
Duty Cycle	40	-	60	%
Vih	1.4	-	AVDDH+0.3	V
Vil	-	-	0.7	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns

Parameter	Min	Typ	Max	Unit
RMS Jitter (12kHz~20MHz)	-	-	1	ps

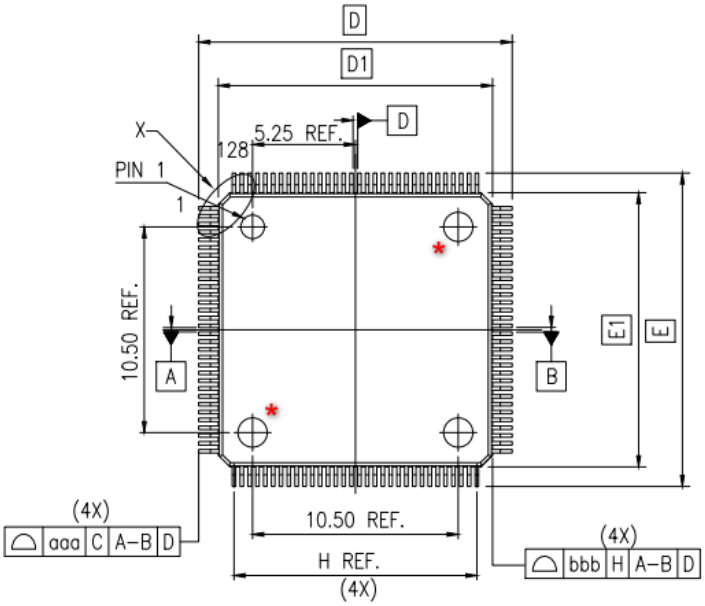
8 Thermal Resistance

Table 52 Thermal Resistance

Symbol	Description	Condition	Typ	Unit
θ_{JA}	Thermal resistance - junction to ambient $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no airflow TA=25°C	19.5	°C/W

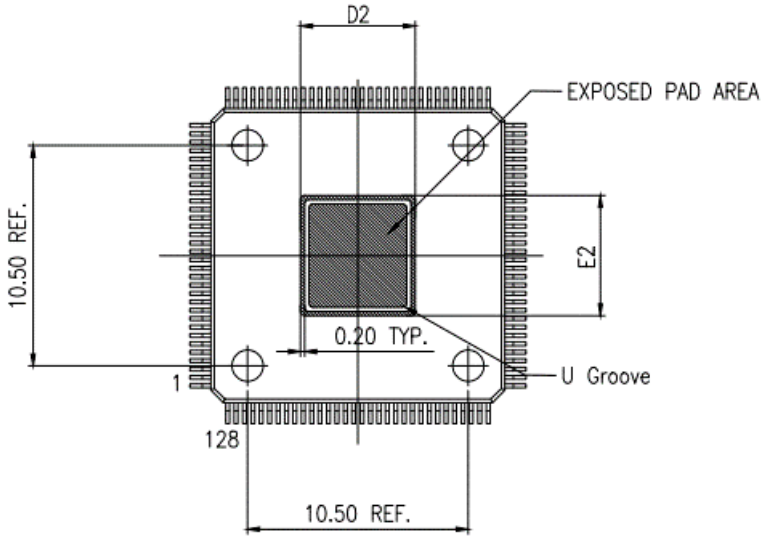
9 Mechanical Information

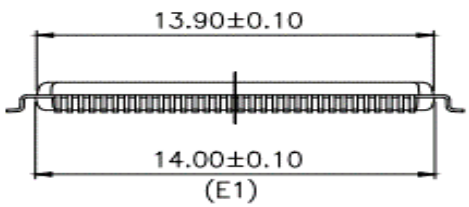
Figure 38 Top View



Note*: Another package's top view does not have two holes with '*'.

Figure 39 Bottom View





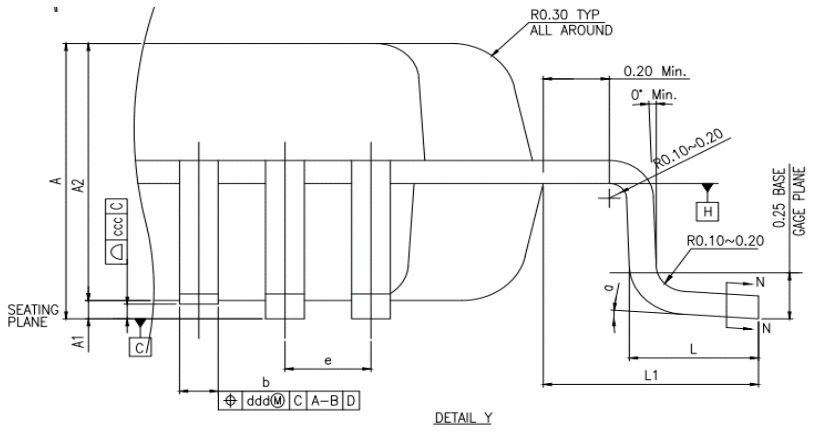


Table 53 Mechanical Dimensions in mm

	SYMBOL	Dimension in mm		
		MIN	TYP	MAX
OVERALL HEIGHT	A	-	-	1.6
STANDOFF	A1	-	-	0.15
PKG THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH	b	0.13	0.18	0.23
LEAD TIP TO TIP	D	15.85	16	16.15
LEAD TIP TO TIP	E	15.85	16	16.15
PKG LENGTH	D1	13.9	14	14.1
PKG WIDTH	E1	13.9	14	14.1
EP Size	D2	5.35	5.6	5.85
	E2	5.35	5.6	5.85
LEAD PITCH	e	0.4BSC		
FOOT LENGTH	L	0.45	0.6	0.75
LEAD LENGTH	L1	1.0 REF		

10 Ordering Information

Motorcomm offers a RoHS package that is compliant with RoHS.

Table 54 Ordering Information

Part Number	Grade	Package	Pack	Status	Operation Temp
YT9215SCH	Industrial	LQFP128-E	Tray 900ea	Mass Production	-40 ~ 85°C