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Motorcomm
YT9215SC Datasheet

LAYER 2 MANAGED 5+2 PORT 10/100/1000M SWITCH CONTROLLER

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General Description

YT9215SC is a LQFP128 E-PAD, high-performance 5+2-port Gigabit Ethernet switch. It integrates five PHY support 1000Base-T/100Base-T/10Base-Te, and supports two extra MAC ports for specific applications which support MII/RMII/RGMII/SGMII/1000Base-X/100Base-FX/2500 Base-X. YT9215SC is also embedded with a RSIC-V microprocessor.

The integrated GIGA-PHY complies with 10BASE-Te, 100BASE-TX, and 1000BASE-T IEEE standard 802.3 and also support Motorcomm proprietary LRE100-4 feature, which makes the device can auto-negotiate and link up with LRE100-4 compliant link partners. LRE100-4 in extended cable length applications up to 400 meter at 100Mbps over CAT5E cable.

The Extension GMAC1 and Extension GMAC2 of the YT9215SC support xMII or SerDes interfaces for connecting with an external PHY, MAC, external CPU or RISC in specific applications, and also support to provide optical port directly by SerDes. The xMII refer to Reduced Gigabit Media Independent Interface (RGMII), Media Independent Interface (MII), and Reduced Media Independent Interface (RMII). The SerDes support IEEE 100Base-FX, IEEE 1000Base-X and IEEE 2500Base-X.

YT9215SC integrates a 4K look-up table with an efficient hashing algorithm for address searching and learning, each of the entries can be configured as a static entry.

YT9215SC supports IEEE 802.1Q VLAN and has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol-and-port-based, VLAN translation ,Flow-based capability， and MAC-based, IP-subnet-based VLAN can be supported by configuration It also supports IVL, SVL, and IVL/SVL for flexible network topology architecture.

The YT9215SC supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources. The YT9215SC supports storm control.

In order to support flexible traffic classification, the YT9215SC supports 384-hardware entry ACL rule check and multiple actions options. The 384 entries are composed of 48 rows, each row has 8 entries. To support long rule, rule extension is supported by any combinations of the 8 entries for each row. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority/DSCP value in 802.1q/Q tag, and rate policing.

Key Features

- High performance, nonblocking, 7 port Ethernet Switch integrating:
  - Five 10/100/1000Mbps PHYs with Advanced Virtual Cable Tester (VCT) diagnostic features,
  - Each PHY supports 10/100/1000M full duplex connectivity (half duplex only supported in 10/100M mode)
  - Full duplex and half duplex operation with IEEE 802.3x flow control and backpressure
- Interface
  - Embedded 5-port 1000/100Base-T/ 10Base-Te PHY
  - Embedded two 2.5Gbps/1Gbps SerDes for 2500Base-X/SGMII/1000Base-X/ 100Base-FX
  - Embedded one RGMII/MII/RMII interface
- Advanced Features
  - Supports parallel LED or serial LED outputs
  - Supports SPI/MDIO/IIC Slave interface
  - Supports MDIO/IIC Master interface
  - Supports 1 interrupt output to external CPU for notification
  - Supports 16K-byte EEPROM space for configuration
  - Link On Cable Length Power Saving
  - Link Down Power Saving
  - Supports 9K byte jumbo frames
- Supports 2 IEEE 802.3ad Link aggregation port groups
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Unknown DA filter mask
  - Supports Port Isolation
  - Supports Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
  - Supports DOS attack prevent
- Control, Management and Statistics
  - Supports RFC MIB Counters
    - MIB-II (RFC 1213)
    - Ethernet-Like MIB (RFC 3635)
    - Interface Group MIB (RFC 2863)
    - RMON (RFC 2819)
    - Bridge MIB (RFC 1493)
    - Bridge MIB Extension (RFC 2674)
  - Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol)
  - Supports Loop Detection
- Packet Process Engine
  - Supports 802.1Q VLANs
  - Supports 4K VLANs
  - Supports untag definition in each VLAN

- Supports VLAN policing and VLAN forwarding decision
- Supports Port based, Tag based, and Protocol based VLAN
- Supports per port egress VLAN tagging and untagging
- Supports IEEE 802.1D/s/w Spanning Tree Protocols
- Support Multicast VLAN (MVR)
- Supports IVL, SVL, and IVL/SVL
- Supports IEEE 802.1ad Stacking VLAN
- Support VLAN translation (1:1/2:1/2:2/ N:1/1:N)
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN
- Supports ACL Rules
- Supports Hardware/Software IGMP/ MLD Snooping
  - Supports Fast Leave
  - Support IGMP V1/V2/V3
  - Static/Dynamic Router port
- Mirror
  - Port based mirror
  - Flow based mirror
- Support reserved multicast control
- Support WOL

- Quality of Service (QoS)
  - Supports Queue based DWRR/SP, packet/byte modes are both supported for DWRR
  - Support min-max queue based shaping, packet/byte modes are both supported
  - Support single token bucket for port based shaping, packet/byte modes are both supported
  - Supports per port Input Bandwidth Control, packet/byte modes are both supported
  - trTCM color aware/blind packet/byte modes
  - Traffic classification based on multiple source type
  - Support 8 unicast queues and 4 multicast queues for each port
  - Tail drop is supported for UQ/MQ, WRED is supported for UQ
- Microprocessor
  - Integrated RISC-V microprocessor
  - Supports Flash Interface (Dual mode/Single mode)
- 25MHz crystal or 3.3V OSC input
- TQFP 128-pin E-PAD package

Block Diagram

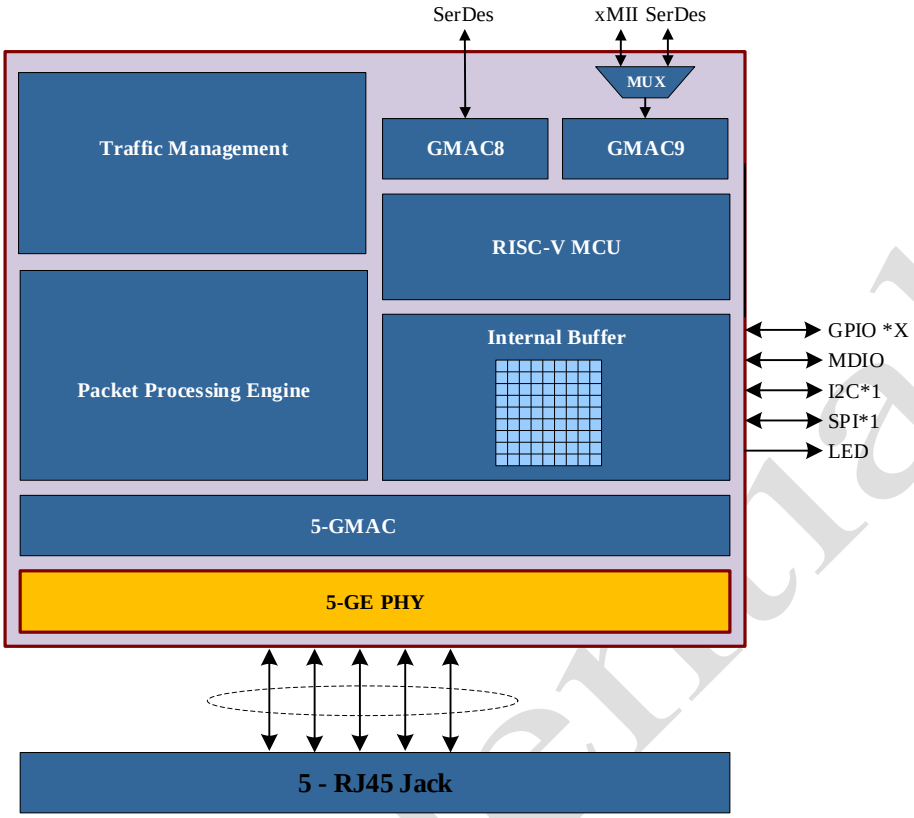

Figure 1. Block Diagram

System Applications

- 5-Port 1000Base-T+1-Port RGMII + 1-Port 2500Base-X Switch
- 5-Port 1000Base-T+2-Port 2500Base-X/1000Base-X/100Base-FX Switch
- 5-Port 1000Base-T Router with Single MII/RGMII
- 5-Port 1000Base-T Router with Dual SGMII
- 5-Port 1000Base-T NVR
- 5-Port 1000Base-T ONU

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Revision History

Revision	Release Date	Summary
Draft_V0.1	2022/09/02	First version.
Draft_V0.2	2022/10/18	General Description：More information and modification.
Draft_V0.3	2022/11/01	Modify 2.2: RGMII description.
Draft_V0.4	2022/12/01	Add 2.14: Configuration Pins, EN_SWR pin description. Modify 2.14: Configuration Pins, STRAP_EN_PWRLIGHT description change.
Draft_V0.5	2023/02/01	Modify 1: Power Requirements. Modify 2: Mechanical Information. Modify 3: RMII description.
Draft_V0.6	2023/02/17	Modify 1: Pin Assignment. Modify 2.5: Description change.
Draft_V0.7	2023/02/28	Modify 1, 2: Pin name change.

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1. Pin Assignment

1.1. Pin Assignment

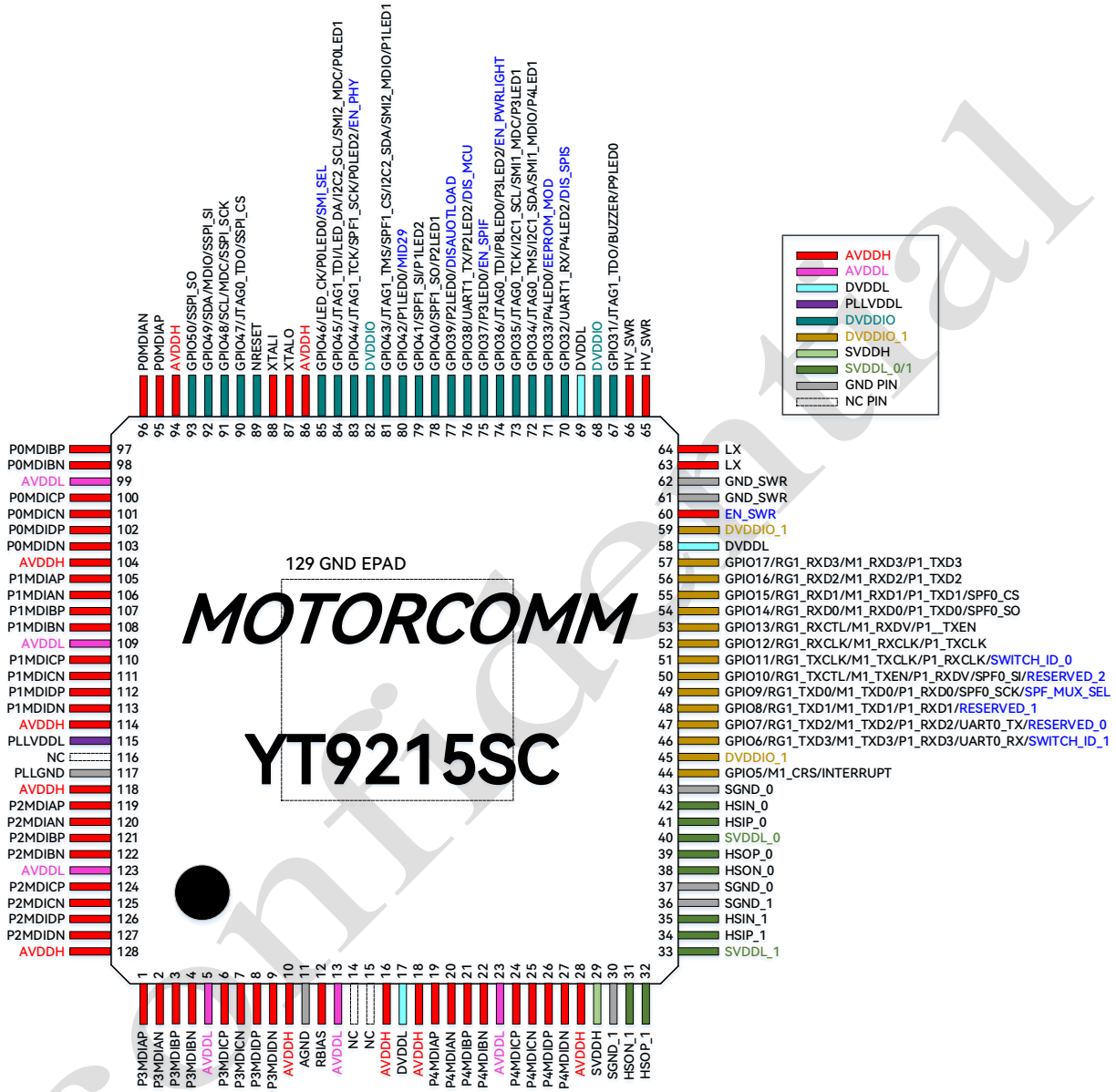


Figure 2. Pin Assignment

1.2. Pin Assignment Table

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Digital Power Pin
- G: Digital Ground pin
- PU: Internal pull up
- LI: Latched Input During Power UP
- OD: Open Drain
- AI: Analog Input
- AO: Analog Output
- AIO: Analog Bidirectional Input and Output
- AP: Analog Power pin
- AG: Analog Ground pin
- PD: Internal pull down
- XT: Crystal Related

Table 1. Pin Assignment

No.	Pin Name	Type
1	P3MDIAP	AIO
2	P3MDIAN	AIO
3	P3MDIBP	AIO
4	P3MDIBN	AIO
5	AVDDL	AP
6	P3MDICP	AIO
7	P3MDICN	AIO
8	P3MDIDP	AIO
9	P3MDIDN	AIO
10	AVDDH	AP
11	AGND	AG
12	RBIAS	AO
13	AVDDL	AP
14	NC	-
15	NC	-
16	AVDDH	AP
17	DVDDL	P
18	AVDDH	AP
19	P4MDIAP	AIO

No.	Pin Name	Type
20	P4MDIAN	AIO
21	P4MDIBP	AIO
22	P4MDIBN	AIO
23	AVDDL	AP
24	P4MDICP	AIO
25	P4MDICN	AIO
26	P4MDIDP	AIO
27	P4MDIDN	AIO
28	AVDDH	AP
29	SVDDH	AP
30	SGND_1	AG
31	HSON_1	AO
32	HSOP_1	AO
33	SVDDL_1	AP
34	HSIP_1	AI
35	HSIN_1	AI
36	SGND_1	AG
37	SGND_0	AG
38	HSON_0	AO

No.	Pin Name	Type
39	HSOP_0	AO
40	SVDDL_0	AP
41	HSIP_0	AI
42	HSIN_0	AI
43	SGND_0	AG
44	GPIO5/M1_CRS/INTERRUPT	IO/PD
45	DVDDIO_1	P
46	GPIO6/RG1_TXD3/M1_TXD3/P1_RXD3/UART0_RX/SWITCH_ID_1	IO/LI/PD
47	GPIO7/RG1_TXD2/M1_TXD2/P1_RXD2/UART0_TX/RESERVED_0	IO/LI/PU
48	GPIO8/RG1_TXD1/M1_TXD1/P1_RXD1/RESERVED_1	IO/LI/PU
49	GPIO9/RG1_TXD0/M1_TXD0/P1_RXD0/SPF0_SCK/SPF_MUX_SEL	IO/PD
50	GPIO10/RG1_TXCTL/M1_TXEN/P1_RXDV/SPF0_SI/RESERVED_2	IO/LI/PD
51	GPIO11/RG1_TXCLK/M1_TXCLK/P1_RXCLK/SWITCH_ID_0	IO/LI/PD
52	GPIO12/RG1_RXCLK/M1_RXCLK/P1_TXCLK	IO/PU
53	GPIO13/RG1_RXCTL/M1_RXDV/P1_TXEN	IO/PU
54	GPIO14/RG1_RXD0/M1_RXD0/P1_TXD0/SPF0_SO	IO/PU
55	GPIO15/RG1_RXD1/M1_RXD1/P1_TXD1/SPF0_CS	IO/PU
56	GPIO16/RG1_RXD2/M1_RXD2/P1_TXD2	IO/PU
57	GPIO17/RG1_RXD3/M1_RXD3/P1_TXD3	IO/PU
58	DVDDL	P

No.	Pin Name	Type
59	DVDDIO_1	P
60	EN_SWR	AI
61	GND_SWR	AG
62	GND_SWR	AG
63	LX	AO
64	LX	AO
65	HV_SWR	AP
66	HV_SWR	AP
67	GPIO31/JTAG1_TDO/BUZZER/P9LED0	IO/PU
68	DVDDIO	P
69	DVDDL	P
70	GPIO32/UART1_RX/P4LED2/DIS_SPIS	IO/LI/PU
71	GPIO33/P4LED0/EEPROM_MOD	IO/LI/PU
72	GPIO34/JTAG0_TMS/I2C1_SDA/SMI1_MDIO/P4LED1	IO/PU/OD
73	GPIO35/JTAG0_TCK/I2C1_SCL/SMI1_MDC/P3LED1	IO/PU/OD
74	GPIO36/JTAG0_TDI/P8LED0/P3LED2/EN_PWRLIGHT	IO/LI/PU
75	GPIO37/P3LED0/EN_SPIF	IO/LI/PU
76	GPIO38/UART1_TX/P2LED2/DIS_MCU	IO/LI/PU
77	GPIO39/P2LED0/DISAUOTLOAD	IO/LI/PU
78	GPIO40/SPF1_SO/P2LED1	IO/PU
79	GPIO41/SPF1_SI/P1LED2	IO/PU
80	GPIO42/P1LED0/MID29	IO/LI/PU
81	GPIO43/JTAG1_TMS/SPF1_CS/I2C2_SDA/SMI2_MDIO/P1LED1	IO/PU/OD
82	DVDDIO	P

No.	Pin Name	Type
83	GPIO44/JTAG1_TCK/SPF1_SCK/P0LED2/EN_PHY	IO/LI/PU
84	GPIO45/JTAG1_TDI/LED_DA/I2C2_SCL/SMI2_MDC/P0LED1	IO/PU/OD
85	GPIO46/LED_CK/P0LED0/SMI_SEL	IO/LI/PU
86	AVDDH	AP
87	XTALO	XT
88	XTALI	XT
89	NRESET	AI/PU
90	GPIO47/JTAG0_TDO/SSPI_CS	IO/PU
91	GPIO48/SCL/MDC/SSPI_SCK	IO/PU/OD
92	GPIO49/SDA/MDIO/SSPI_SI	IO/PU/OD
93	GPIO50/SSPI_SO	IO/PU
94	AVDDH	AP
95	P0MDIAP	AIO
96	P0MDIAN	AIO
97	P0MDIBP	AIO
98	P0MDIBN	AIO
99	AVDDL	AP
100	P0MDICP	AIO
101	P0MDICN	AIO
102	P0MDIDP	AIO
103	P0MDIDN	AIO

No.	Pin Name	Type
104	AVDDH	AP
105	P1MDIAP	AIO
106	P1MDIAN	AIO
107	P1MDIBP	AIO
108	P1MDIBN	AIO
109	AVDDL	AP
110	P1MDICP	AIO
111	P1MDICN	AIO
112	P1MDIDP	AIO
113	P1MDIDN	AIO
114	AVDDH	AP
115	PLLVDDL	AP
116	NC	–
117	PLLGND	AG
118	AVDDH	AP
119	P2MDIAP	AIO
120	P2MDIAN	AIO
121	P2MDIBP	AIO
122	P2MDIBN	AIO
123	AVDDL	AP
124	P2MDICP	AIO
125	P2MDICN	AIO
126	P2MDIDP	AIO
127	P2MDIDN	AIO
128	AVDDH	AP
129	GND EPAD	G

2. Pin Description

2.1. MDI Interface Pins

Table 2. Transceiver Interface

No.	Pin Name	Type	Description
95	P0MDIAP	AIO	Port 0 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
96	P0MDIAN	AIO	
97	P0MDIBP	AIO	Port 0 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
98	P0MDIBN	AIO	
100	P0MDICP	AIO	Port 0 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
101	P0MDICN	AIO	
102	P0MDIDP	AIO	Port 0 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
103	P0MDIDN	AIO	
105	P1MDIAP	AIO	Port 1 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
106	P1MDIAN	AIO	
107	P1MDIBP	AIO	Port 1 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
108	P1MDIBN	AIO	
110	P1MDICP	AIO	Port 1 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
111	P1MDICN	AIO	
112	P1MDIDP	AIO	Port 1 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
113	P1MDIDN	AIO	
119	P2MDIAP	AIO	Port 2 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
120	P2MDIAN	AIO	
121	P2MDIBP	AIO	Port 2 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
122	P2MDIBN	AIO	
124	P2MDICP	AIO	Port 2 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
125	P2MDICN	AIO	
126	P2MDIDP	AIO	Port 2 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
127	P2MDIDN	AIO	
1	P3MDIAP	AIO	Port 3 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
2	P3MDIAN	AIO	
3	P3MDIBP	AIO	Port 3 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
4	P3MDIBN	AIO	
6	P3MDICP	AIO	Port 3 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
7	P3MDICN	AIO	
8	P3MDIDP	AIO	Port 3 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
9	P3MDIDN	AIO	

19	P4MDIAP	AIO	Port 4 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
20	P4MDIAN	AIO	
21	P4MDIBP	AIO	Port 4 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
22	P4MDIBN	AIO	
24	P4MDICP	AIO	Port 4 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
25	P4MDICN	AIO	
26	P4MDIDP	AIO	Port 4 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
27	P4MDIDN	AIO	

2.2. RGMII Interface Pins

Table 3. RGMII

No.	Pin Name	Type	Description
51	RG1_TXCLK	IO/LI/PD	RGMII 1 transmit reference clock will be 125Mhz, 25MHz, or 2.5MHz depending on speed.
50	RG1_TXCTL	IO/LI/PD	RGMII 1 Transmit Control Signal from the MAC.
46	RG1_TXD3	IO/LI/PD	RGMII 1 transmit Data. Data is transmitted from MAC to PHY via TXD[3:0].
47	RG1_TXD2	IO/LI/PU	
48	RG1_TXD1	IO/LI/PU	
49	RG1_TXD0	IO/PD	
52	RG1_RXCLK	IO/PU	RGMII 1 continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream.
53	RG1_RXCTL	IO/PU	RGMII 1 receive Control Signal to the MAC.
57	RG1_RXD3	IO/PU	RGMII 1 receive Data. Data is transmitted from PHY to MAC via RXD[3:0].
56	RG1_RXD2	IO/PU	
55	RG1_RXD1	IO/PU	
54	RG1_RXD0	IO/PU	

2.3. MII Interface Pins

Table 4. MII Interface Pins

No.	Pin Name	Type	Description
51	M1_TXC/ P1_RXC	IO/LI/PD	1. M_TXC Pin in MII MAC Mode. MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. 2. P_RXC Pin in MII PHY Mode.

			MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te.
50	M1_TXEN/ P1_RXDV	IO/LI/PD	1. M_TXEN Pin in MII MAC Mode. MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN is synchronous to M_TXC. 2. P_RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV is synchronous to P_RXC.
46	M1_TXD3/ P1_RXD3	IO/LI/PD	1. M_TXD[3:0] Pin in MII MAC Mode. MII Transmit Data Bus. M_TXD[3:0] is synchronous to M_TXC. 2. P_RXD[3:0] Pin in MII PHY Mode. MII Receive Data Bus. P_RXD[3:0] is synchronous to P_RXC.
47	M1_TXD2/ P1_RXD2	IO/LI/PU	
48	M1_TXD1/ P1_RXD1	IO/LI/PU	
49	M1_TXD0/ P1_RXD0	IO/LI/PD	
52	M1_RXC/ P1_TXC	IO/PU	1. M_RXC Pin in MII 1 MAC Mode. MII Receive Clock(input). Used to synchronize M_RXD[3:0], and M_RXDV. 2. P_TXC Pin in MII PHY Mode. MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN. The frequency depends on the link speed, that is 25MHz at 100Base-TX , and 2.5MHz at 10Base-Te.
53	M1_RXDV/ P1_TXEN	IO/PU	1. M_RXDV Pin in MII MAC Mode. MII Receive Data Valid. This synchronous input is asserted when valid data is driven on M_RXD bus. M_RXDV is synchronous to M_RXC. 2. P_TXEN Pin in MII PHY Mode. MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN is synchronous to P_TXC.
57	M1_RXD3/ P1_TXD3	IO/PU	1. M_RXD[3:0] Pin in MII MAC Mode. MII Receive Data Bus. M_RXD[3:0] is synchronous to M_RXC. 2. P_TXD[3:0] Pin in MII 1 PHY Mode. MII Transmit Data Bus. P_TXD[3:0] is synchronous to P_TXC .
56	M1_RXD2/ P1_TXD2	IO/PU	
55	M1_RXD1/ P1_TXD1	IO/PU	

54	M1_RXD0/ P1_TXD0	IO/PU	

2.4. RMII Interface Pins

Table 5. RMII Interface Pins

No.	Pin Name	Type	Description
51	M1_TXC/ P1_RXC	IO/LI/PD	REFCLK pin in RMII Mode. 1. In RMII MAC Mode, REFCLK is an input pin. 2. In RMII PHY Mode, REFCLK is an output pin. REF_CLK is a 50Mhz clock that provides the timing reference for CRSDV, RXD[1:0], TXEN, TXD[1:0].
50	M1_TXEN/ P1_RXDV	IO/LI/PD	1. TXEN Pin in RMII MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK. 2. CRSDV Pin in RMII PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is nonidle synchronized with REFCLK.
48	M1_TXD1/ P1_RXD1	IO/LI/PU	1. TXD[1:0] Pin in RMII MAC Mode, synchronous to REFCLK. 2. RXD[1:0] Pin in RMII PHY Mode, synchronous to REFCLK.
49	M1_TXD0/ P1_RXD0	IO/PD	
53	M1_RXDV/ P1_TXEN	IO/PU	1. CRSDV Pin in RMII MAC Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is nonidle synchronized with REFCLK. 2. TXEN Pin in RMII PHY Mode. The synchronous input indicates that valid data is being driven on the TXD bus. TXEN is synchronous to REFCLK.
55	M1_RXD1/ P1_TXD1	IO/PU	1. RXD[1:0] Pin in RMII MAC Mode, is synchronous to RXC. 2. TXD[1:0] Pin in RMII PHY Mode, is synchronous to TXC .
54	M1_RXD0/ P1_TXD0	IO/PU	

2.5. High-Speed Serial Interface Pins

Table 6. High-Speed Serial Interface Pins

No.	Pin Name	Type	Description
31	HSON_1	AO	High-Speed Serial Interface Pins: support 3.125GHz or 1.25GHz. Differential serial output interface.
32	HSOP_1	AO	
34	HSIP_1	AI	High-Speed Serial Interface Pins: support 3.125GHz or 1.25GHz. Differential serial input interface.
35	HSIN_1	AI	
38	HSON_0	AO	High-Speed Serial Interface Pins: support 3.125GHz or 1.25GHz. Differential serial output interface.
39	HSOP_0	AO	
41	HSIP_0	AI	High-Speed Serial Interface Pins: support 3.125GHz or 1.25GHz. Differential serial input interface.
42	HSIN_0	AI	

2.6. Parallel LED Pins

Table 7. Parallel LED Pins

No.	Pin Name	Type	Description
70	P4LED2	IO/LI/PU	Default port 4 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
72	P4LED1	IO/PU/OD	Default port 4 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
71	P4LED0	IO/LI/PU	Default port 4 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
74	P3LED2	IO/LI/PU	Default port 3 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
73	P3LED1	IO/PU/OD	Default port 3 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
75	P3LED0	IO/LI/PU	Default port 3 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
76	P2LED2	IO/LI/PU	Default port 2 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
78	P2LED1	IO/PU	Default port 2 Parallel LED LED1 Output Signal.

			The LED indicates information is defined by register or EEPROM
77	P2LED0	IO/LI/PU	Default port 2 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
79	P1LED2	IO/PU	Default port 1 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
81	P1LED1	IO/PU/OD	Default port 1 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
80	P1LED0	IO/LI/PU	Default port 1 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
83	P0LED2	IO/LI/PU	Default port 0 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
84	P0LED1	IO/PU/OD	Default port 0 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
85	P0LED0	IO/LI/PU	Default port 0 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM

2.7. Serial LED Pins

Table 8. Serial LED Pins

No.	Pin Name	Type	Description
85	LED_CK	IO/LI/PU	Serial Mode LED Clock Signal.
84	LED_DA	IO/PU/OD	Serial Mode LED Data Signal.

2.8. SPI FLASH Pins

Table 9. SPI FLASH Interface Pins

No.	Pin Name	Type	Description
55	SPF0_CS	IO/PU	SPI FLASH chip select signal.
81	SPF1_CS	IO/PU/OD	

54	SPF0_SO	IO/PU	In Serial I/O Mode, SPI Serial FLASH Serial Data Output (YT9215SC input pin) In Dual I/O Mode, SPI FLASH bi-directional pin (this is MSB)
78	SPF1_SO	IO/PU	
50	SPF0_SI	IO/LI/PD/OD	In Serial I/O Mode SPI Serial FLASH Serial Data Input (YT9215SC output pin) In Dual I/O Mode SPI FLASH bi-directional pin (this is LSB)
79	SPF1_SI	IO/PU	
49	SPF0_SCK	IO/PD/OD	SPI FLASH Clock.
83	SPF1_SCK	IO/LI/PU	

2.9. JTAG Interface Pins

Table 10. JTAG Interface Pins

No.	Pin Name	Type	Description
67	JTAG1_TDO	IO/PU	Test Data Out.
84	JTAG1_TDI	IO/PU/OD	Test Data In.
81	JTAG1_TMS	IO/PU/OD	Test Mode Select.
83	JTAG1_TCK	IO/LI/PU	Test Clock.
90	JTAG0_TDO	IO/PU	Test Data Out.
74	JTAG0_TDI	IO/LI/PU	Test Data In.
72	JTAG0_TMS	IO/PU/OD	Test Mode Select.
73	JTAG0_TCK	IO/PU/OD	Test Clock.

2.10. UART Interface Pins

Table 11. UART Interface Pins

No.	Pin Name	Type	Description
46	UART0_RX	IO/LI/PD	UART RX pin.
47	UART0_TX	IO/LI/PU	UART TX pin.
70	UART1_RX	IO/LI/PU	UART RX pin.
76	UART1_TX	IO/LI/PU	UART TX pin.

2.11. Master I2C and MDIO Interface Pins

Table 12. Master I2C and MDIO Interface Pins

No.	Pin Name	Type	Description
73	I2C1_SCL/ SMI1_MDC	IO/PU/OD	SCL pin in Group1 Master I2C. MDC pin in Group1 Master SMI.
72	I2C1_SDA/ SMI1_MDIO	IO/PU/OD	SDA pin in Group1 Master I2C. MDIO pin in Group1 Master SMI.
84	I2C2_SCL/ SMI2_MDC	IO/LI/PU	SCL pin in Group2 Master I2C. MDC pin in Group2 Master SMI.
81	I2C2_SDA/ SMI2_MDIO	IO/PU/OD	SDA pin in Group2 Master I2C. MDIO pin in Group2 Master SMI.

2.12. Management Interface Pins

Table 13. Management Interface Pins

No.	Pin Name	Type	Description
90	SSPI_CS	IO/PU	SPI slave Mode Chip Select Input.
91	SCL/ MDC/ SSPI_SCK	IO/PU/OD	1. EEPROM auto load mode serial clock output 2. I2C slave mode serial clock input 3. MDC/MDIO slave mode serial clock input 4. SPI slave Mode serial clock input
92	SDA/ MDIO/ SSPI_SI	IO/PU/OD	1. EEPROM auto load mode serial data input 2. I2C slave mode serial data 3. MDC/MDIO slave mode serial data 4. SPI slave Mode serial data input
93	SSPI_SO	IO/PU	SPI slave Mode serial data output

2.13. GPIO Pins

Table 14. GPIO Pins

No.	Pin Name	Type	Description
44	GPIO5	IO/PD	General Purpose Input/Output Interfaces IO5.
46	GPIO6	IO/LI/PD	General Purpose Input/Output Interfaces IO6.
47	GPIO7	IO/LI/PU	General Purpose Input/Output Interfaces IO7.
48	GPIO8	IO/LI/PU	General Purpose Input/Output Interfaces IO8.
49	GPIO9	IO/PD	General Purpose Input/Output Interfaces IO9.
50	GPIO10	IO/LI/PD	General Purpose Input/Output Interfaces IO10.
51	GPIO11	IO/LI/PD	General Purpose Input/Output Interfaces IO11.

52	GPIO12	IO/PU	General Purpose Input/Output Interfaces IO12.
53	GPIO13	IO/PU	General Purpose Input/Output Interfaces IO13
54	GPIO14	IO/PU	General Purpose Input/Output Interfaces IO14.
55	GPIO15	IO/PU	General Purpose Input/Output Interfaces IO15.
56	GPIO16	IO/PU	General Purpose Input/Output Interfaces IO16.
57	GPIO17	IO/PU	General Purpose Input/Output Interfaces IO17.
67	GPIO31	IO/PU	General Purpose Input/Output Interfaces IO31.
70	GPIO32	IO/LI/PU	General Purpose Input/Output Interfaces IO32.
71	GPIO33	IO/LI/PU	General Purpose Input/Output Interfaces IO33.
72	GPIO34	IO/PU/OD	General Purpose Input/Output Interfaces IO34.
73	GPIO35	IO/PU/OD	General Purpose Input/Output Interfaces IO35.
74	GPIO36	IO/LI/PU	General Purpose Input/Output Interfaces IO36.
75	GPIO37	IO/LI/PU	General Purpose Input/Output Interfaces IO37.
76	GPIO38	IO/LI/PU	General Purpose Input/Output Interfaces IO38.
77	GPIO39	IO/LI/PU	General Purpose Input/Output Interfaces IO39.
78	GPIO40	IO/PU	General Purpose Input/Output Interfaces IO40.
79	GPIO41	IO/PU	General Purpose Input/Output Interfaces IO41.
80	GPIO42	IO/LI/PU	General Purpose Input/Output Interfaces IO42.
81	GPIO43	IO/PU/OD	General Purpose Input/Output Interfaces IO43.
83	GPIO44	IO/LI/PU	General Purpose Input/Output Interfaces IO44.
84	GPIO45	IO/PU/OD	General Purpose Input/Output Interfaces IO45.
85	GPIO46	IO/LI/PU	General Purpose Input/Output Interfaces IO46.
90	GPIO47	IO/PU	General Purpose Input/Output Interfaces IO47.
91	GPIO48	IO/PU/OD	General Purpose Input/Output Interfaces IO48.
92	GPIO49	IO/PU/OD	General Purpose Input/Output Interfaces IO49.
93	GPIO50	IO/PU	General Purpose Input/Output Interfaces IO50.

2.14. Configuration Pins

Table 15. Configuration Pins

No.	Pin Name	Type	Description
46	SWITCH_ID_1	IO/LI/PD	Switch_ID[1:0] for slave MDC/MDIO format.
51	SWITCH_ID_0	IO/LI/PD	
49	SPF_MUX_SEL	IO/PD	SPI FLASH Interface Position Select. Pull Up: Select Spi-Flash-0 pin 49\50\54\55. Pull Down: Select Spi-Flash-1 pin 78\79\81\83.
60	EN_SWR	AI	Disable/Enable internal switching regulator. Pull Down: Disable SWR

			Pull Up: Enable SWR.
70	DIS_SPIS	IO/LI/PU	Disable Slave SPI Interface for External CPU Access YT9215SC Register Pull Up: Disable SPI Slave Interface and refer to [STRAP_SMI_SEL] Pull Down: Enable SPI Slave Interface
71	EEPROM_MOD	IO/LI/PU	EEPROM Mode Selection. Pull Up: EEPROM 24Cxx Size greater than 16Kbits (24C32~) Pull Down: EEPROM 24Cxx Size less than or equal to 16Kbit (24C02~24C16).
74	EN_PWRLIGHT	IO/LI/PU	Disable/Enable LED function When Powered On. Pull Up: Enable LED Pull Down: Disable LED.
75	EN_SPIF	IO/LI/PU	Enable SPI FLASH Interface. Pull Up: Enable FLASH interface Pull Down: Disable FLASH interface
76	DIS_MCU	IO/LI/PU	Disable Embedded MCU. Pull Up: Disable embedded MCU upon power on or reset Pull Down: Enable embedded MCU upon power on or reset
77	DISAUTOLOAD	IO/LI/PU	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload upon power on or reset Pull Down: Enable EEPROM autoload upon power on or reset
80	MID29	IO/LI/PU	Slave SMI (MDC/MDIO) Device Address. Pull Up: Slave SMI (MDC/MDIO) Device Address is 0x1d Pull Down: Slave SMI (MDC/MDIO) Device Address is 0x0
83	EN_PHY	IO/LI/PU	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY
85	SMI_SEL	IO/LI/PU	EEPROM SMI/MII Management Interface Selection. Pull Up: EEPROM SMI interface when DIS_SPIS = 1 Pull Down: MII Management interface when DIS_SPIS = 1

2.15. Power Related Pins

Table 16. Power Related Pins

No.	Pin Name	Type	Description
68, 82	DVDDIO	P	Digital power 3.3V
45, 59	DVDDIO_1	P	Digital power 3.3V for Extension Port 1

17, 58, 69	DVDDL	P	Digital power 1.1V
10, 16, 18, 28, 86, 94, 104, 114, 118, 128	AVDDH	AP	Analog power 3.3V
5, 13, 23, 99, 109, 123	AVDDL	AP	Analog power 1.1V
29	SVDDH	AP	SerDes power 3.3V
40	SVDDL_0	AP	SerDes power 1.1V for group 0.
33	SVDDL_1		SerDes power 1.1V for group 1.
115	PLLVDDL	AP	PLL Power 1.1V.
11	AGND	AG	Analog GND.
37, 43	SGND_0	AG	SerDes GND.
30, 36	SGND_1	AG	SerDes GND.
117	PLLGND	AG	PLL GND.
129	GND EPAD	G	GND

2.16. Clock Pins

Table 17. Clock Pins

No.	Pin Name	Type	Description
88	XTAL_I	XT	25MHz Crystal Input pin. If use external oscillator or clock from another device. 1. When connect an external 25Hhz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25Hhz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.
87	XTAL_O	XT	25Mhz Crystal Output pin. If use external oscillator or clock from another device. 1. When connect an external 25Hhz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. 2. When connect an external 25Hhz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.

2.17. Reset Pins

Table 18. Reset Pins

No.	Pin Name	Type	Description
89	NRESET	AI/PU	Hardware reset, active low. Requires an external pull-up resistor

2.18. Miscellaneous Pins

Table 19. Miscellaneous Pin

No.	Pin Name	Type	Description
14, 15, 116	NC	-	Not connect. Must be left floating in normal operation.
47	RESERVED_1	-	Reserved. This pin must be pulled high via an external 4.7k ohm resistor to DVDDIO upon power on.
48	RESERVED_2	-	Reserved. This pin must be pulled high via an external 4.7k ohm resistor to DVDDIO upon power on.
50	RESERVED_3	-	Reserved. This pin must be pulled high via an external 4.7k ohm resistor to DVDDIO upon power on.

3. Power Requirements

3.1. Absolute Maximum Ratings

Table 20. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (T_j)	–	+125	°C
Storage Temperature	−45	+125	°C
DVDDIO, DVDDIO_1, DVDDIO_2, AVDDH, SVDDH, Supply Referenced to GND and AGND	GND−0.3	+3.70	V
DVDDL, AVDDL, PLLVDDL, SVDDL_0, SVDDL_1, Supply Referenced to GND, AGND and PLLGND	GND−0.3	+1.40	V
Digital Input Voltage	GND−0.3	VDDIO+0.3	V

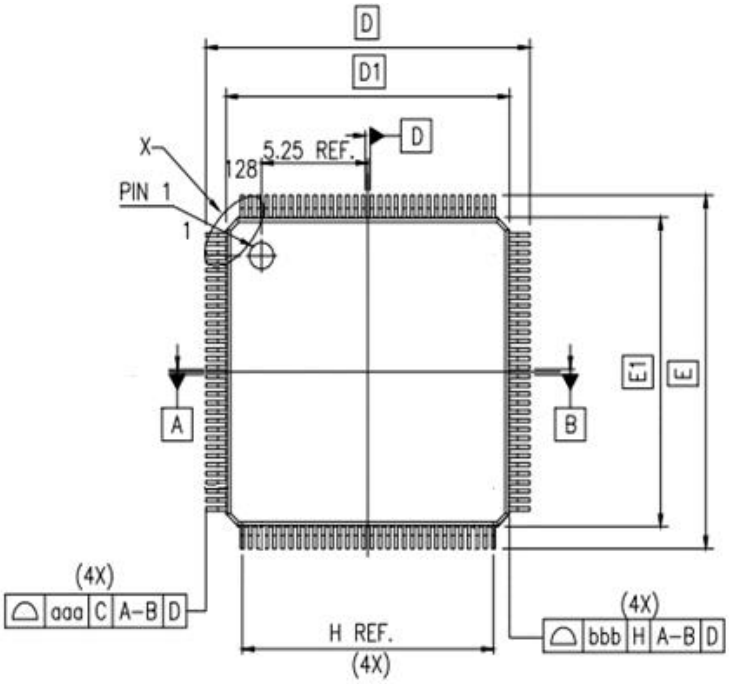
3.2. Recommended Operating Range

Table 21. Recommended Operating Range

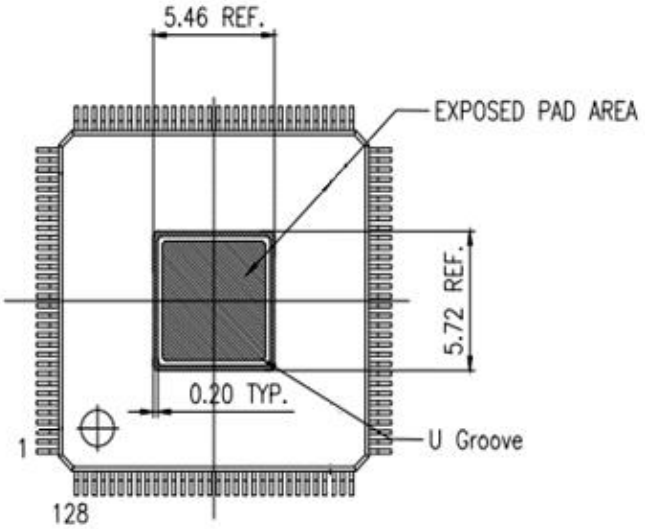
Parameter		Min	TYP	Max	Units
Ambient Operating Temperature (T_a)		0	–	70	°C
DVDDIO, AVDDH, SVDDH Supply Voltage Range		3.135	3.30	3.63	V
DVDDIO_1 Supply Voltage Range (DVDDIO_1: Extension Port 2 Supports 1.8V, 2.5V, 3.3V)	3.3V	3.135	3.30	3.63	V
	2.5V	2.25	2.50	2.75	V
	1.8V	1.62	1.80	1.98	V
DVDDL, AVDDL, PLLVDDL, SVDDL_0, SVDDL_1, Supply Voltage Range		1.045	1.10	1.32	V

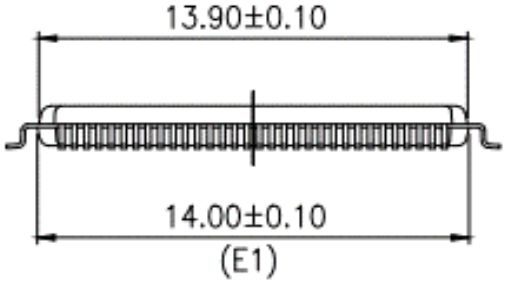
4. Mechanical Information

Top View



Bottom View





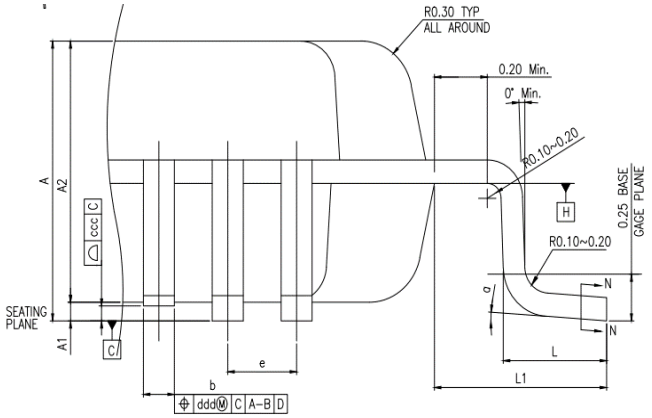


Table 22. Mechanical Dimensions in mm

	SYMBOL	MIN	NOM	MAX
OVERALL HEIGHT	A	–	–	1.6
STANDOFF	A1	–	–	0.127
PKG THICKNESS	A2	1.35	1.4	1.45
LEAD WIDTH	b	0.13	0.18	0.23
LEAD TIP TO TIP	D	15.85	16	16.15
LEAD TIP TO TIP	E	15.85	16	16.15
PKG LENGTH	D1	13.9	14	14.1
PKG WIDTH	E1	13.9	14	14.1
	E-PAD	5.72 REF x5.46 REF.		
LEAD PITCH	e	0.4BSC		
FOOT LENGTH	L	0.45	0.6	0.75
LEAD LENGTH	L1	1.0 REF.		

5. Ordering Information

Motorcomm offers a RoHS package that is compliant with RoHS.

Table 23. Ordering Information

Part Number	Grade	Package	Pack	Status	Operation Temp
YT9215SC	Consumer	LQFP128-pin	Tray 900e.a	Engineering Sample	0 ~70 °C