

CMD60R650D/CMU60R650D

600V, 576mΩ typ., 7A N-Channel Super Junction Power MOSFET

General Description

The 60R650D is power MOSFET using Cmos's advanced super junction technology that can realize very low on resistance, gate charge and reduced tendency for ringing. As a result, its switching loss is very low, making it optimized for switching applications. Moreover, these user friendly devices offer the advantages of improved ruggedness and remarkable ESD capability by integrated Zener diode, making it an ideal choice for designers.

Features

- Multi-layer Epitaxial Chip Technology
- Low On-Resistance
- 100% avalanche tested
- RoHS Compliant

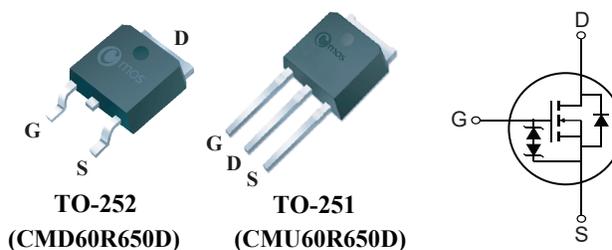
Product Summary

BVDSS	R _{DS(on)} max.	ID
600V	0.65Ω	7A

Applications

- Adapter
- PFC power supply stages
- DC-DC converters

TO-252/251 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	600	V
V _{GS}	Gate-Source Voltage	±30	V
I _D @T _C =25°C	Continuous Drain Current	7	A
I _D @T _C =100°C	Continuous Drain Current	4.2	A
I _{DM}	Pulsed Drain Current	28	A
EAS	Single Pulse Avalanche Energy ¹	183	mJ
P _D @T _C =25°C	Total Power Dissipation	75	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient	---	133	°C/W
R _{θJC}	Thermal Resistance Junction-case	---	1.67	°C/W

Electrical Characteristics(T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	600	---	---	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =4.5A	---	576	650	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	2.0	---	4.0	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =600V, V _{GS} =0V	---	---	1	μA
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±30V, V _{DS} =0V	---	---	±10	μA
g _{fs}	Forward Transconductance	V _{DS} =20V, I _D =4.5A	---	4.2	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	16	---	Ω
Q _g	Total Gate Charge	I _D =3.2A	---	22	---	nC
Q _{gs}	Gate-Source Charge	V _{DD} =480V	---	3.5	---	
Q _{gd}	Gate-Drain Charge	V _{GS} =0 to 10V	---	12	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =400V V _{GS} =10V R _G =10Ω, I _D =3A	---	11	---	ns
T _r	Rise Time		---	25	---	
T _{d(off)}	Turn-Off Delay Time		---	35	---	
T _f	Fall Time		---	27	---	
C _{iss}	Input Capacitance	V _{DS} =100V, V _{GS} =0V, f=1MHz	---	300	---	pF
C _{oss}	Output Capacitance		---	29	---	
C _{rss}	Reverse Transfer Capacitance		---	2	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current	V _G =V _D =0V, Force Current	---	---	7	A
I _{SM}	Pulsed Source Current		---	---	28	A
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =4.5A	---	0.85	1.4	V
t _{rr}	Reverse Recovery Time	I _S =3A, V _{DS} =400V	---	190	---	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	---	1.3	---	μC

Note :

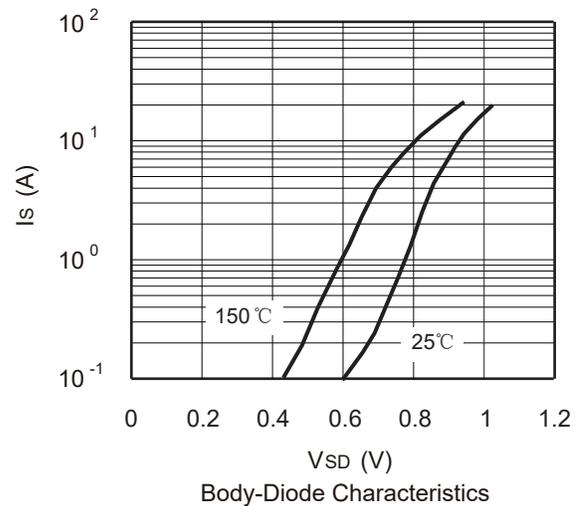
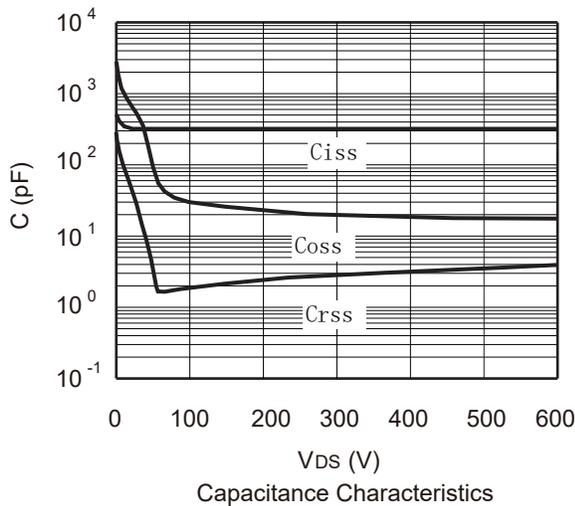
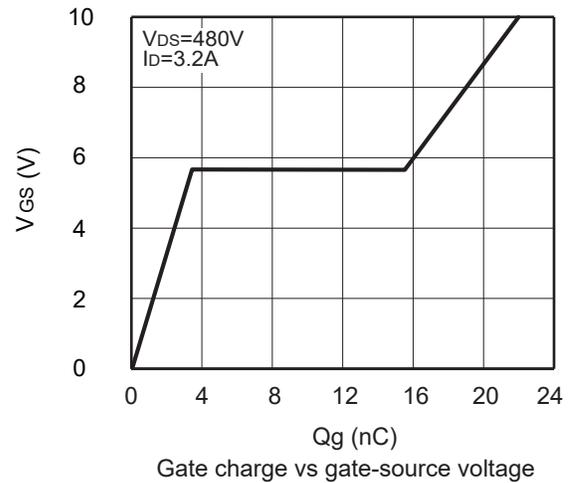
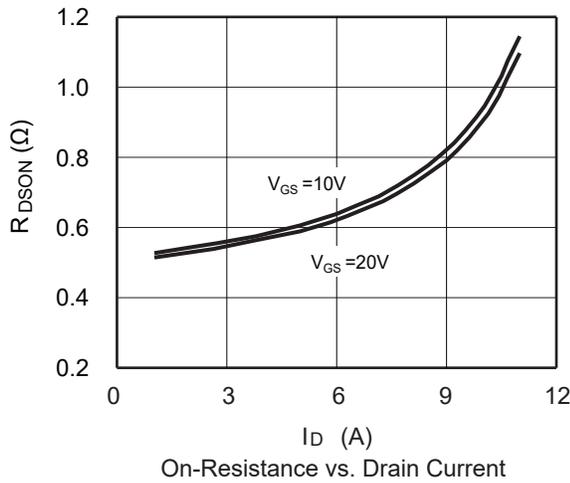
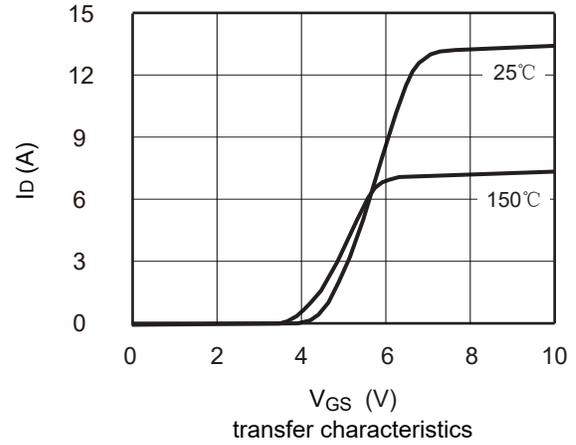
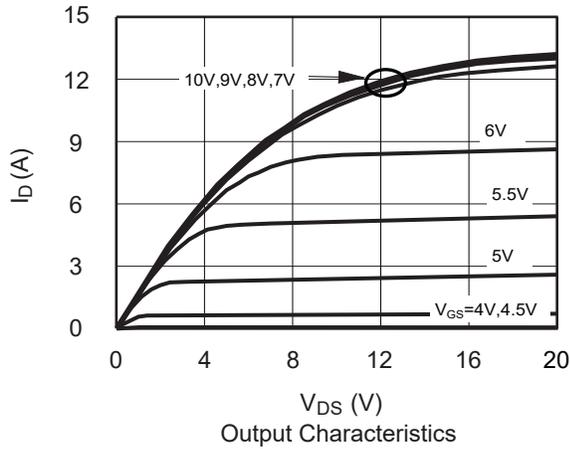
1.The EAS data shows Max. rating . The test condition is V_{DD}=100V, V_{GS}=10V, L=30mH, I_{AS}=3.5A.

This product has been designed and qualified for the consumer market.

Cmos assumes no liability for customers' product design or applications.

Cmos reserves the right to improve product design, functions and reliability without notice. Please refer to the latest version of specification.

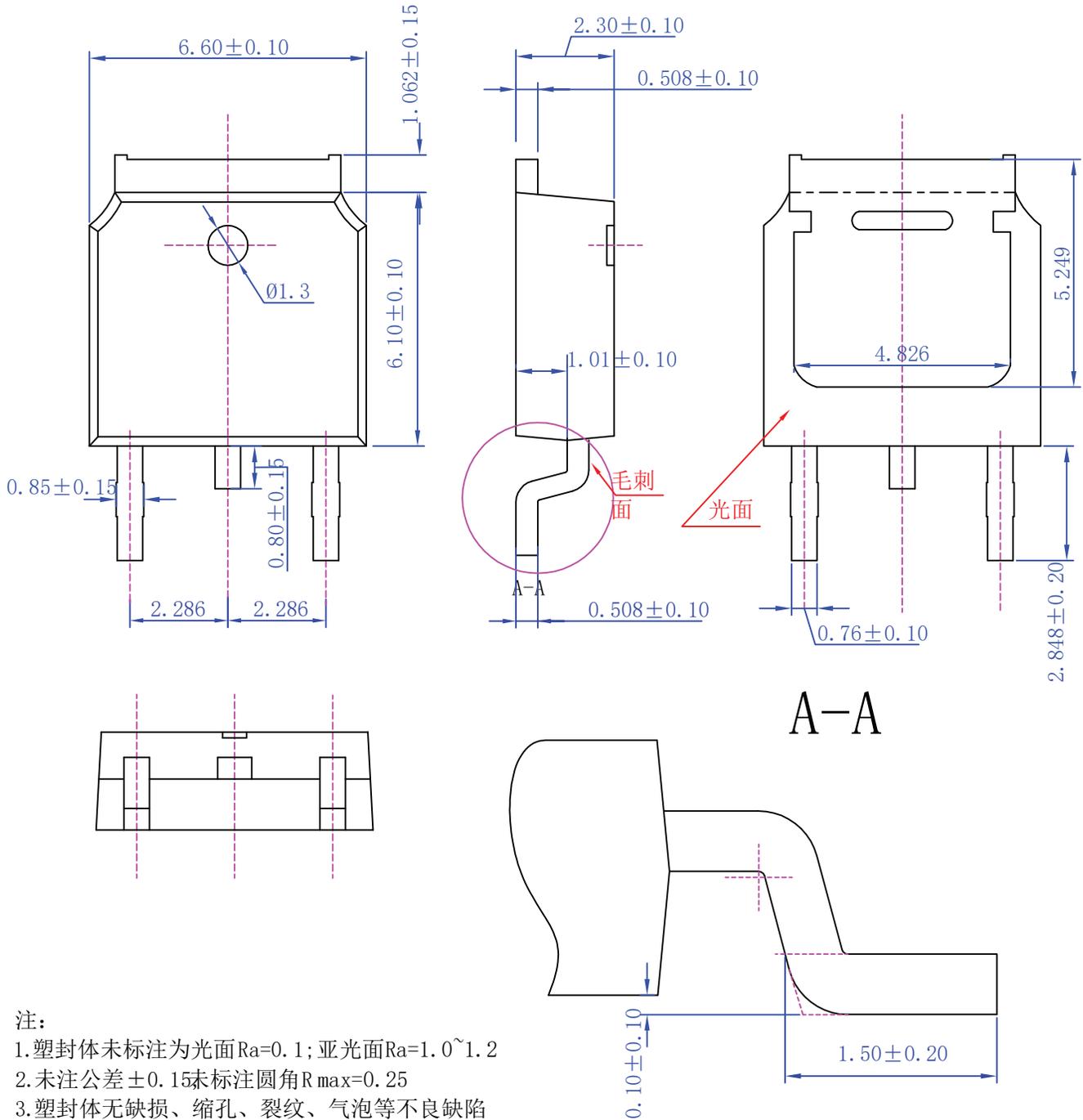
Typical Characteristics



Package Dimension

TO-252

Unit :mm



注:

1. 塑封体未标注为光面Ra=0.1; 亚光面Ra=1.0~1.2
2. 未注公差±0.15未标注圆角R max=0.25
3. 塑封体无缺损、缩孔、裂纹、气泡等不良缺陷
4. 标注单位mm
5. 顶针孔不允许凸出塑封体表面

CMD60R650D/CMU60R650D



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Package Dimension

TO-251A

Unit :mm

