Application Note: SYV939C

High Efficiency, 38V Maximum Input Single Inductor Synchronous Step Up/Down Regulator

General Description

The SYV939C is a high voltage synchronous Buck-Boost converter. The device operates over a wide input voltage range from 4V to 28V with 10A maximum average inductor current capability. The four-integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The SYV939C includes full protection features, such as output over current/short circuit protection, over voltage protection and thermal shutdown for reliable operating.

The device is available in compact QFN4×4-32 package.

Features

- 4V to 28V Operating Input Voltage Range
- 38V Absolute Maximum Input Voltage
- Low $R_{DS(ON)}$ for Internal Switches: 25mΩ
- Internal Soft-start Limits the Inrush Current
- Hiccup Mode for Output Over Current, Short-Circuit and Over Voltage Protection
- Thermal Shutdown with Auto Recovery
- 250kHz/500kHz Selectable Switching Frequency
- 6A/10A Selectable Average Inductor Current Limitation
- 1.0V ±1.5% Reference Voltage Accuracy
- Programmable Output Current Limitation with External Sensing Resistor
- Compact package: QFN4×4-32

Ordering Information

SYV939 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SYV939CQFC	QFN4×4-32	

Applications

- Docking Station
- Laptop
- High-end Power Bank
- Monitor
- Car Charger
- USB PD

Typical Application

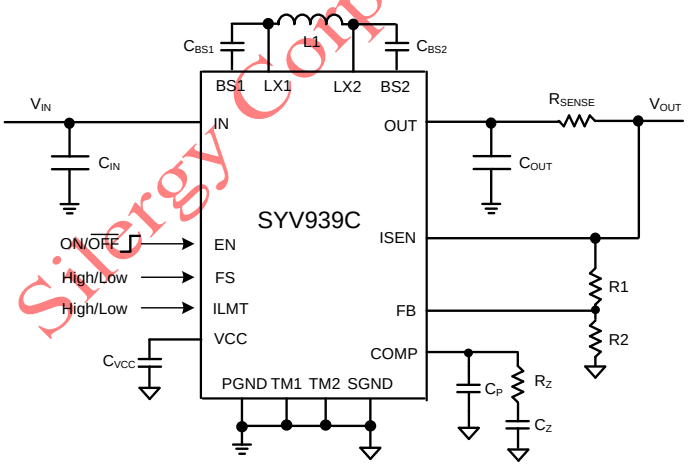


Fig.1 Typical Schematic Diagram

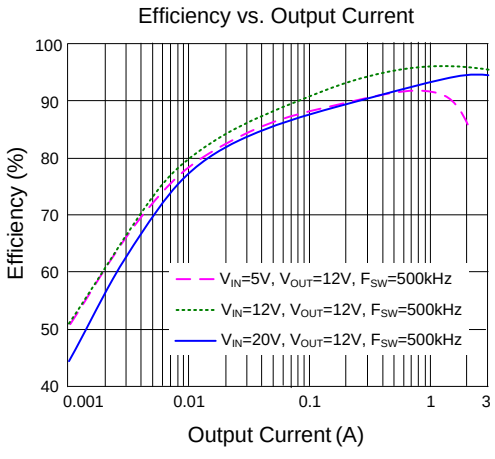
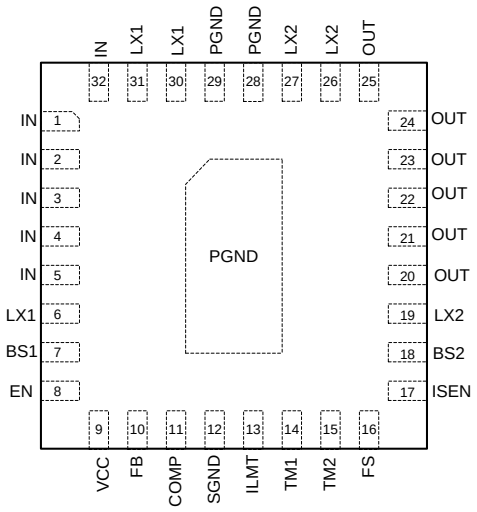


Fig.2 Efficiency vs. Output Current

Pinout (Top View)



(QFN4×4-32)

Top Mark: BXX***xyz*** **(**Device code: BXX; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Description
IN	1,2,3,4,5,32	Power input pin, decouple this pin to PGND with at least a 10μF ceramic capacitor.
LX1	6,30,31	Switching node 1.
BS1	7	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS1 and the LX1 pin.
EN	8	IC enable control pin, logic high enable. This pin is internally pulled high by 400nA pull-up current.
VCC	9	3.3V LDO output, power supply for internal driver and control circuits. Decouple this pin to SGND with a minimum of 2.2μF ceramic capacitor.
FB	10	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT}=1V\times(R_1+R_2)/R_2$.
COMP	11	Compensation pin. Connect the RC network between this pin and the ground.
SGND	12	Signal ground.
ILMT	13	Average inductor current limitation threshold select pin. Connect this pin to VCC for 10A threshold, and connect this pin to SGND for 6A threshold.
TM1	14	Test pin. For factory use only. Connect this pin to SGND in application.
TM2	15	Test pin. For factory use only. Connect this pin to SGND in application.
FS	16	Switching frequency select pin. Connect this pin to VCC for 500kHz switching frequency, and connect this pin to SGND for 250kHz switching frequency.
ISEN	17	Current sense pin. Connect a resistor R_{SENSE} between OUT and ISEN to set the output current limitation threshold. $I_{OUT,LMT}$ = 30m/R_{SENSE}.
BS2	18	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS2 and the LX2 pin.
LX2	19,26,27	Switching node 2.
PGND	28,29, Exposed Pad	Power ground.
OUT	20,21,22,23, 24,25	Power output pin, decouple this pin to PGND with at least a 10μF ceramic capacitor.

Block Diagram

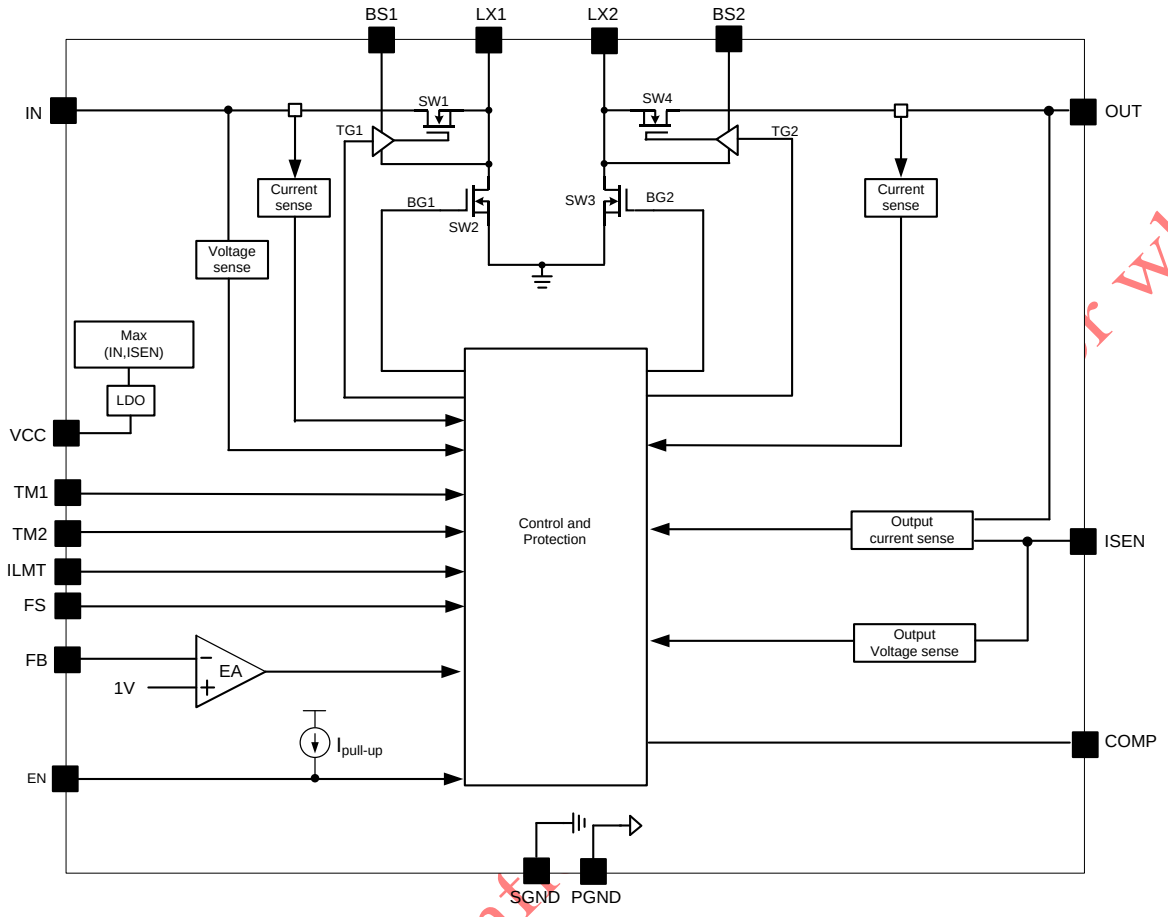


Fig.3 Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX1, LX2, OUT, ISEN, EN, FB, COMP ---------- -0.3V to 38V
BS-LX, VCC ---------- -0.3V to 4V
FS, ILMT ---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25℃ QFN4×4-32 ---------- 4W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 28℃/W
θ_{JC} ---------- 2.8℃/W
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

Input Voltage Range ---------- 4V to 28V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 12V, V_{OUT}=12V, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		28	V
Input UVLO Threshold	$V_{IN,UVLO}$		2.9		3.5	V
UVLO Hysteresis	$V_{UVLO,HYS}$			0.2		V
VCC LDO Voltage	VCC	I_{LDO}=10mA	3.09	3.26	3.44	V
Quiescent Current	I_Q	EN=High, No switching			300	μA
Shutdown Current	I_{SD}	EN=Low			11.5	μA
Feedback Reference Voltage	V_{REF}		0.985	1	1.015	V
FB Input Current	I_{FB}		-50		50	nA
Output OVP Threshold	$V_{FB,OVP}$	FB voltage rising		120		% V_{REF}
Output OVP Delay Time	$t_{OVP,DLY}$			10		μs
Output UVP Threshold	$V_{FB,UVP}$	FB voltage falling		50		% V_{REF}
Output UVP Delay Time	$t_{UVP,DLY}$			200		μs
Internal Power MOSFET $R_{DS(ON)}$	$R_{DS(ON)}$			25		mΩ
Inductor Average Current Limit	I_{AVG}	ILMT connect to SGND		6		A
		ILMT connect to VCC		10		A
Inductor Peak Current Limit	I_{PK}	ILMT connect to SGND	6.4	8.4	10.5	A
		ILMT connect to VCC	9.2	13	16.5	A
EN Input Logic High	V_{ENH}		1.5			V
EN Input Logic Low	V_{ENL}				0.5	V
Output Current Limit Voltage Threshold	$V_{IOUT,LIM}$		33	37	41	mV
Oscillator Frequency	f_{OSC}	FS connect to VCC	425	500	575	kHz
		FS connect to GND	190	250	320	kHz
Min On Time	t_{ON_MIN}			150		ns
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃
Soft-start Time	t_{ss}			1.5		ms

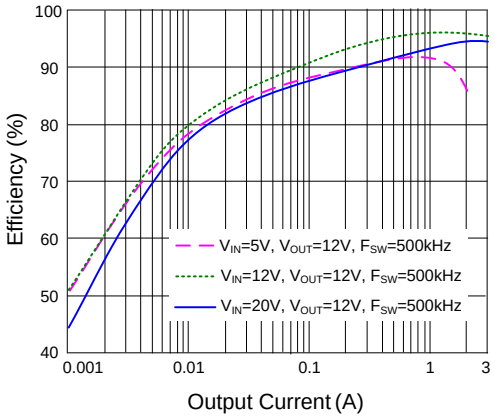
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

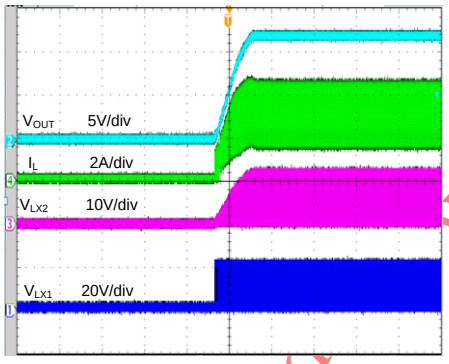
Typical Performance Characteristics

Efficiency vs. Output Current



Regulator Enable

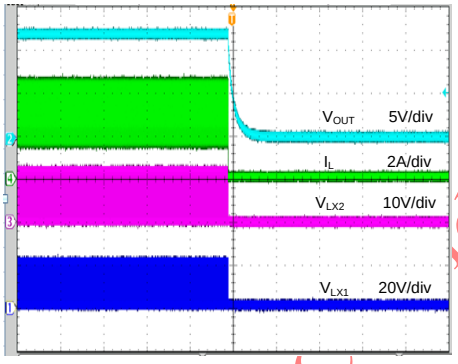
(V_{IN}=20V,V_{OUT}=12V,R_{LOAD}=4Ω)



Time (2ms/div)

Regulator Disable

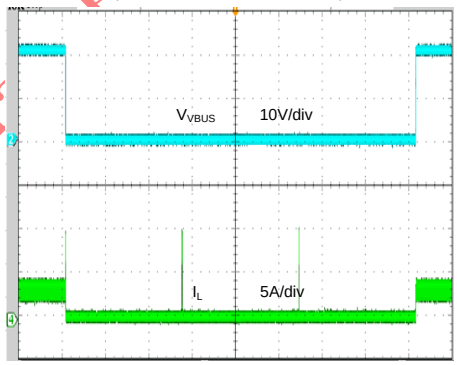
(V_{IN}=20V,V_{OUT}=12V,R_{LOAD}=4Ω)



Time (2ms/div)

Short Circuit Test

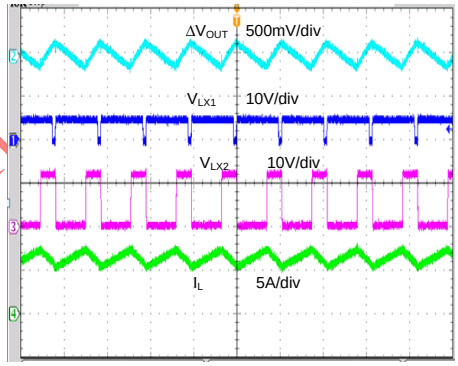
(V_{IN}=20V,V_{OUT}=20V,R_{LOAD}=6.7Ω)



Time (1s/div)

Output Ripple

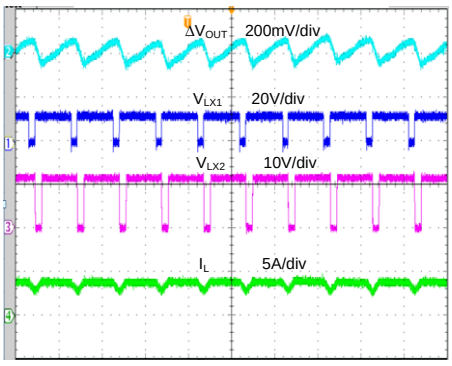
(V_{IN}=5V,V_{OUT}=12V,I_{LOAD}=2A)



Time (2μs/div)

Output Ripple

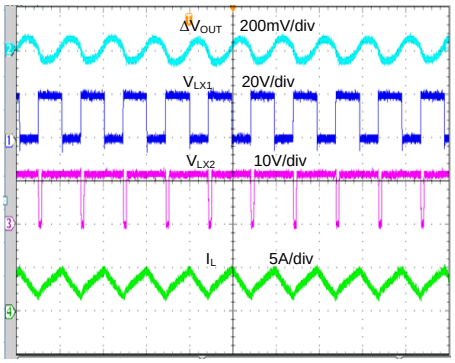
(V_{IN}=12V,V_{OUT}=12V,I_{LOAD}=3A)



Time (2μs/div)

Output Ripple

(V_{IN}=20V,V_{OUT}=12V,I_{LOAD}=3A)



Time (2μs/div)

Application Information

Input Under-voltage Lock-out

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches may be sufficiently enhanced, the IC incorporates input under-voltage lock-out (UVLO) protection. The device remains in a low current state and all switching is inhibited until V_{IN} exceeds the input UVLO (rising) threshold. At that time, if EN is enabled, the IC will start-up by initiating a soft-start ramp. If V_{IN} falls below the input UVLO (falling) threshold, switching will be suppressed again.

Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven above 1.5V normal device operation will be enabled. When driven < 0.5V the device will be shut down, reducing input current to < 11.5μA. EN is internally pulled high by 400nA pull-up current. In applications where EN is pulled high to the power input V_{IN}, a 10kΩ to 100kΩ resistor should be added between power input and EN.

Soft-start

The SYV939C incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1.5ms, which avoids high current flow and transients during startup.

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 100nF low ESR ceramic capacitor to be connected between BS1 and LX1, BS2 and LX2. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel power MOSFET switch.

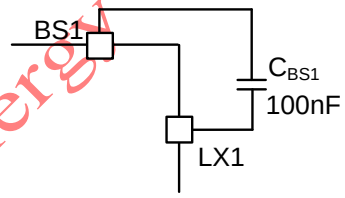


Fig. 4 External Bootstrap Capacitor Connection

VCC Linear Regulator

An internal linear regulator (VCC) produces a 3.3V supply from VIN which powers the internal gate drivers, PWM logic, analog circuitry and other blocks. Connect a 2.2μF low ESR ceramic capacitor from VCC to GND.

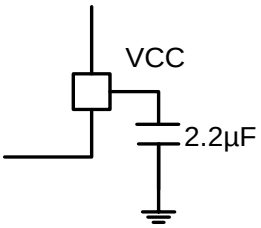


Fig. 5 VCC Regulator

Fault Protection Modes

1. Average Inductor Current Limit

The device incorporates an average inductor limit. When the average inductor current is greater than the threshold, the internal control loop will regulate the average inductor current by decreasing duty cycle. The IC resumes normal operation when the fault condition is removed. The average inductor current limit threshold is selectable by pulling ILMT pin low or to VCC.

2. Peak Inductor Current Limit

The device also incorporates a cycle-by-cycle "peak" current limit. Inductor current is measured in SW1 when it is on. If the current exceeds the current limit, both SW1 and SW3 turn off, and SW2 and SW4 turn on. The peak current limit threshold is selectable by pulling ILMT pin low or to VCC.

3. Short-circuit Protection

If V_{OUT} < ~50% of the set point and the device is in current limit (average or peak inductor current) continuously for approximately 200μs, the short-circuit protection mode will be initiated, and the device will shut down for approximately 2.6s. The device will then restart with a complete soft-start cycle. If the short circuit condition remains another 'hiccup' cycle of shutdown and restart will continue indefinitely unless the UVP threshold is reached.

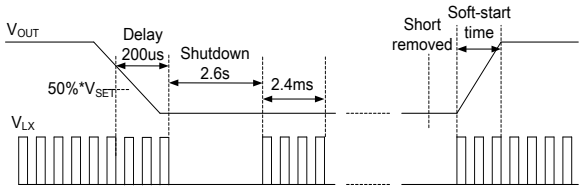


Fig. 6 Description of Short-circuit Protection

4. Output Over-voltage Protection (OVP)

This device includes output over-voltage protection (OVP). If the output voltage rises above the feedback regulation level, SW1 and SW3 turn off and the synchronous rectifier turns on. If the output voltage remains high, the SW2 and SW4 remain on until the inductor current reaches zero. If the output voltage continues to rise and exceeds the output over-voltage

threshold for more than 10μs, the output over-voltage protection mode is triggered. The device resumes regulation once the overvoltage condition is removed.

5. Over-temperature Protection (OTP)

SYV939C includes over-temperature protection (OTP) circuitry to prevent over heating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 150℃. Once the junction temperature cools down by approximately 15℃, the IC will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Feedback Resistor Selection

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 100kΩ is highly recommended for both resistors. The output voltage V_{OUT} is programmed by external voltage divider with the 1V internal voltage reference as given in equation (1).

$$V_{OUT} = 1V \times \frac{R_1 + R_2}{R_2} \quad (1)$$

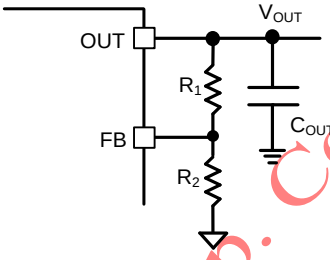


Fig.7 V_{OUT} Programming

Output Current Limit

The SYV939C provides a function for output current limit by sensing the voltage drop between the OUT pin and the ISEN pin (as shown in fig.7). Once the differential voltage on R_{SENSE} exceeds the voltage threshold, the internal current control loop will regulate the output current by decreasing duty cycle until UVP or OTP is triggered. Noticing that the effects of RPIN and RWIRE cannot be ignored, the actual limit current ILIMIT can be calculated as given in Equation (2):

$$I_{LIMIT} = \frac{V_{OUT} - V_{ISEN}}{R_{SENSE} + R_{PIN} + R_{WRIE}} \quad (2)$$

where R_{PIN}≈1.65mΩ.

R_{WIRE} depends on PCB layout.

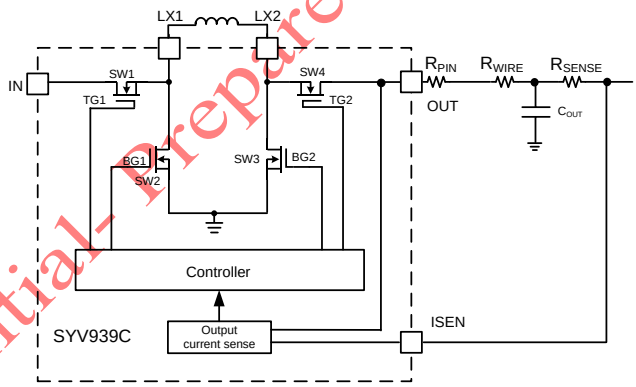
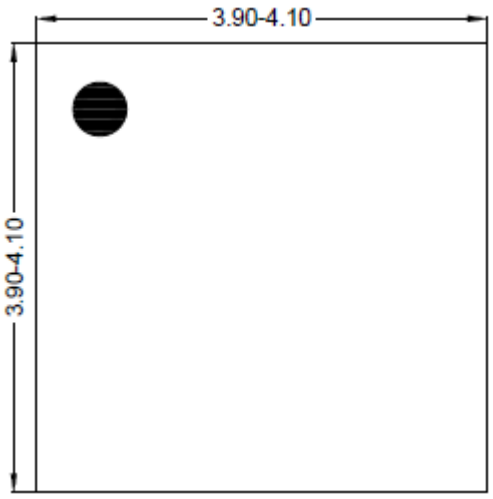
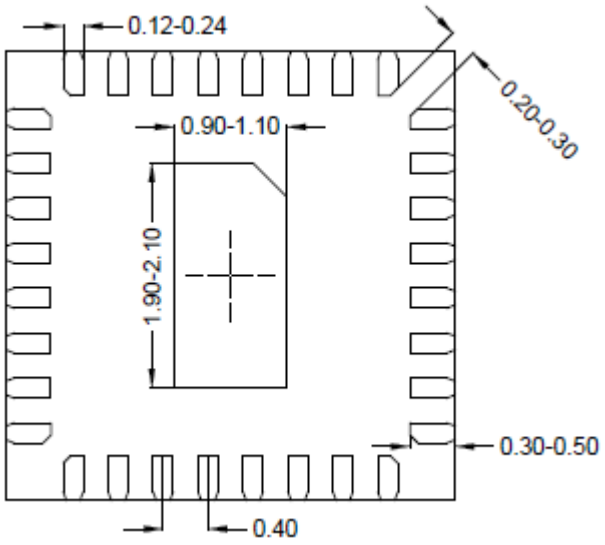


Fig.8 Description of Output Current Limit

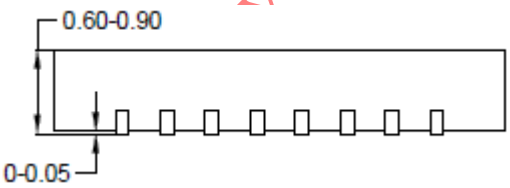
QFN4×4-32 Package Outline Drawing



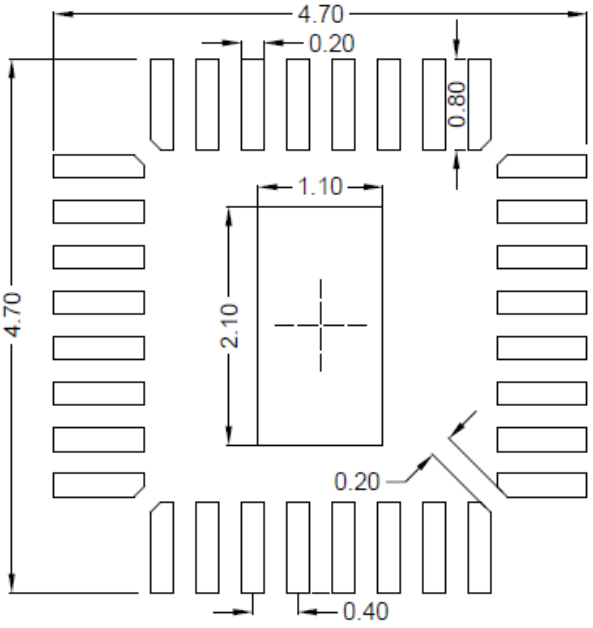
Top View



Bottom View



Side View



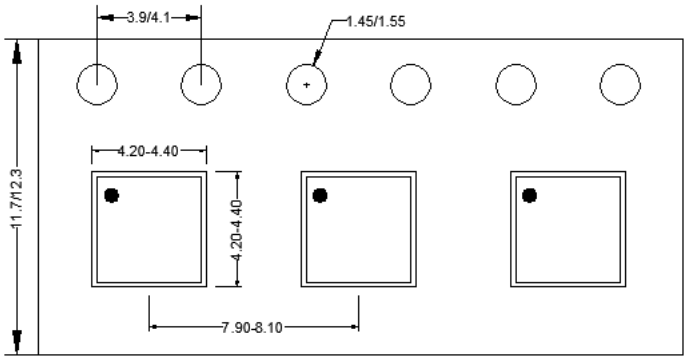
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

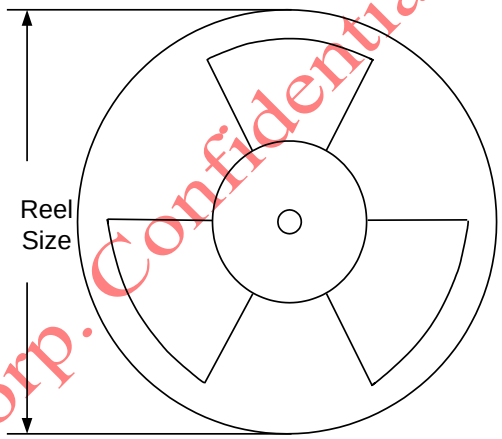
1. Taping orientation

QFN4×4



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN4×4	12	8	13"	400	400	5000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov.19, 2018	Revision 0.9B	Update in Features: 1: change "4V to 28V Input Voltage Range" to " 4V to 28V **Operating** Input Voltage Range"; 2: Add "38V Absolute Maximum Input Voltage" in Feature. Change "28V Input" to "38V Maximum Input" in the header.
Oct. 24, 2018	Revision 0.9A	change the Absolute Maximum Rating of IN, LX1, LX2, OUT, ISEN, EN, FB, COMP from "-0.3V to 30V" to "-0.3V to 38V"
July 10, 2018	Revision 0.9	Initial Release

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