



钛迪半导体  
Tudi Semiconductor

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## Product Specification

TUDI-ADM3483

3.3 V Slew Rate Limited, Half- and Full-Duplex,  
RS-485/RS-422 Transceivers

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## FEATURES

- 3.3V power operation
- Co-existence with 5V logic
- Compliant with EIA RS-422 and RS-48 standards, common mode range
- Data rate 250Kbps
- Low EMI (electromagnetic interference) reduction rise rate
- Low supply current in shutdown mode
- Up to 32 transceivers on the bus
- - 7 V to 12 V bus common mode range

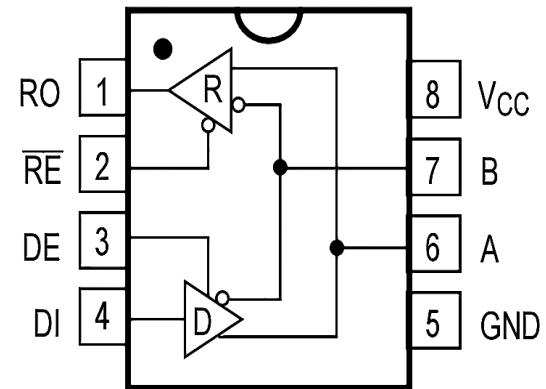


Figure 1. Pin Diagram

## Description

The ADM3483 is a low-power, differential line transceiver designed to operate from a single 3.3V power supply. The low power consumption, plus a shutdown mode, make it ideal for applications where power conservation is critical. The ADM3483 is designed for half-duplex communication.

The ADM3483 features a limited-slope driver that significantly reduces EMI and reflections caused by improper cable termination, thus allowing error-free data transmission at data rates up to 250kbps.

The receiver input impedance is 12k $\Omega$ , allowing up to 32 transceivers to be connected to the bus. A thermal shutdown circuit prevents excessive power dissipation due to bus contention or output short circuit. The thermal shutdown circuit will drive the driver output into a high-impedance state if a temperature rise is detected in the internal driver circuit under fault conditions. If the input is not connected (floating), the receiver contains a fault-safe feature that results in a high output state. These devices are fully specified in the commercial and industrial temperature ranges. The ADM3483 is available in an 8-pin SOIC DIP package.

## Applications

- Low power RS-485/RS-422
- applications Telecom
- Industrial process control
- HVAC



## Pin description

Pin Number	Pin Name	FUNCTION
1	RO	Receiver Output. When enabled, if $A-B \geq -10mV$ , then $RO=high$ . If $A-B \leq -200 mV$ , then $RO=low$
2	/RE	Receiver Output Enable. A low level enables the RO; a high level places it in a high impedance state.
3	DE	Driver Output Enable. A high level enables the driver differential outputs, Pin A and Pin B; a low level places the driver in a high impedance state.
4	DI	Driver Input. When the driver is enabled, a logic low on DI forces Pin A low and Pin B high; a logic high on DI forces Pin A high and Pin B low.
5	GND	Ground Connection (0V).
6	A	No inverting Receiver Input A/Driver Output A
7	B	Inverting Receiver Input B/Driver Output B.
8	VCC	Power Supply

## Parameter limit

PARAMETER	Symbol	Value	Unit
CTR Port	/RE,DE,DI	-0.3~VCC+0.3	V
Driver Output Voltage	A、B	-7~13	V
Receiver Output Voltage	RO	-0.3~VCC+0.3	V
Supply Voltage	VCC	+7	V
Continuous Power Dissipation	MSOP8.SOP8.DIP8	830	mW
Soldering Temperature (reflow)		300	°C
Storage Temperature Range		-60~150	°C
Temperature Range		-40~85	°C

Stresses beyond those listed under "Parameter limit" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability



### Receiver Switching Characteristics

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Propagation delay from receiver input to output, from low to high	tRPLH	CL=15pF See Figures 7 and 8		80	150	ns
The propagation delay from receiver input to output is from high to low	tRPHL			80	150	ns
tRPLH-tRPHL	tRPDS			7	10	ns
Enable low time out	tRPZL	CL=15pF See Figures 7 and 8		20	50	ns
Enable to output high time	tRPZH	CL=15pF See Figures 7 and 8		20	50	ns
Time from output low to disable	tpRLZ	CL=15pF See Figures 7 and 8		20	45	ns
Time from output high to disable	tpRHZ	CL=15pF See Figures 7 and 8		20	45	ns
Off stateEnable to output high time	tRPSH	CL=15pF See Figures 7 and 8		200	1400	ns
Off stateEnable low time out	tRPSL	CL=15pF See Figures 7 and 8		200	1400	ns
Time to turn off	tsHDN	NOTE	80		300	ns

NOTE: When /RE=1 and DE=0, the device will not enter shutdown mode if the duration is less than 80ns; however, it will definitely enter shutdown mode if the duration exceeds 300ns



supply current

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Supply current	$I_{CC1}$	/RE=0V,DE=0V		520	800	uA
	$I_{CC2}$	/RE=VCC,DE=VCC		540	700	uA
Turn-off current	$I_{sHDN}$	/RE=VCC,DE=0V		0.5	10	uA

Drive Switch Characteristics

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Driver differential output delay	$t_{DD}$	$R_{DIFF}=60\Omega$ , $CL_1=CL_2=100\text{pF}$ (see Figure 3 and Figure 4)		10	35	ns
Drive differential output transition time	$t_{TD}$			12	25	ns
Drive propagation delay from low to high	$t_{PLH}$	$R_{DIFE}=27\Omega$ (see Figure 3 and Figure 4)		8	35	ns
Drive propagation delay from high to low	$t_{PHL}$			8	35	ns
$ t_{PLH}-t_{PHL} $	$t_{PDS}$			1	8	ns
Enable to output high	$t_{pZH}$	$RL=110\Omega$ (see Figure 5 and 6)		20	90	ns
Enable to output low	$t_{pzL}$			20	90	ns
Input low to disable	$t_{PLZ}$	$RL=110\Omega$ (see Figure 5 and 6)		20	80	ns
Enable high input	$t_{PHZ}$			20	80	ns
Enable high output under off condition	$t_{DSH}$	$R=110\Omega$ (see Figure 5 and 6)		500	900	ns
Enable low output under shutdown conditions	$t_{DSL}$	$RL=110\Omega$ (see Figure 5 and 6)		500	900	ns



DC electrical characteristics of the driver

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Driver differential output (non-loaded)	VoD <sub>1</sub>			3.3		V
Drive differential output	VoD <sub>2</sub>	graph 2,RL=54	1.5		VCC	V
		graph 2,RL=100	2		VCC	
Variation in the amplitude of the output voltage (NOTE1)	VoD	graph 2,RL=54			0.2	V
Output common mode voltage	Voc	graph 2,RL=54			3	V
Amplitude Variation of Common Mode Output Voltage (NOTE1)	Voc	graph 2,RL=54			0.2	V
High-level input	VH	DE,DI,/RE	2.0			V
Low level input	V	DE,DI,/RE			0.8	V
Logic input current	IN1	DE,DI,/RE	-2		2	uA
Output the current during a short circuit, with high short-circuit	IosD <sub>1</sub>	Short circuit to 0V~12V			250	mA
Output the current during a short circuit, down to low	IosD <sub>2</sub>	Short circuit to -7V~0V	-250			mA
Overtemperature shutdown threshold temperature				140		
Overtemperature turn-off hysteresis temperature				20		



DC Electrical Characteristics of the Receiver

Parameter	symbol	Test condition	Minimum	Typical case	Maximum	Unit
Input current(A,B)	IN2	DE=0V,VCC=0 or 3.3V VIn=12V			125	uA
		DE=0V,VCC=0 or 3.3V VIn=-7V	-100			uA
Forward input threshold voltage	VIT+	-7V Vcm 12V			+200	mV
Reverse input threshold voltage	VIT-	-7V Vcm 12V	-200			mV
Input hysteresis voltage	Vhys	-7V Vcm 12V	10	30		mV
High level output voltage	VoH	IoUT=-2.5mA,VID =+200 mV	VCC-1.5			V
Low level output voltage	VoL	IoUT=+2.5mA,VD =-200 mV			0.4	V
Three-state input leakage current	IoZR	0.4V<Vo<2.4V			±1	uA
Input resistance of receiver	RIn	-7V Vcm 12V	96			k
Receiver short circuit current	IosR	0V Vo VCC	±8		±60	mA



## FUNCTION TABLES

TRANSMITTING						RECEIVING			
CTR	/RE	X	X	0	1	0	0	0	1
	DE	1	1	0	0	X	X	X	X
INPUTS	DI	1	0	X	X				
	A-B					$\geq -10\text{mV}$	$\leq -200\text{mV}$	Open/shorted	X
OUTPUTS	A	H	L	Z					
	B	L	H	Z					
	RO					H	L	H	Z

X:Don't care;Z:high impedance.

## TEST CIRCUIT

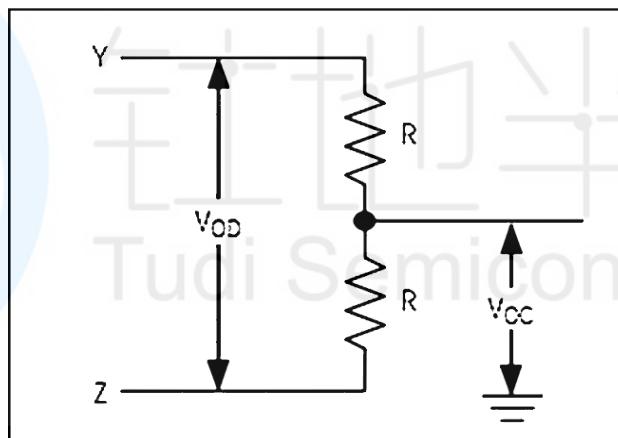


Figure 2 DC test load of the driver

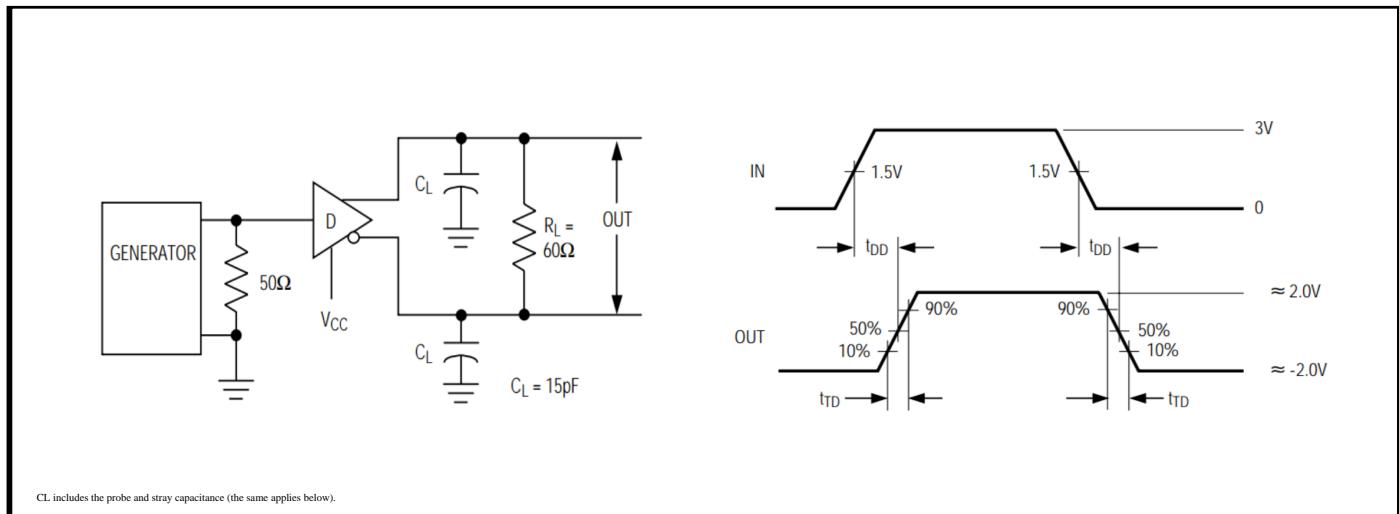


Figure 3 Differential delay and transit time of driver

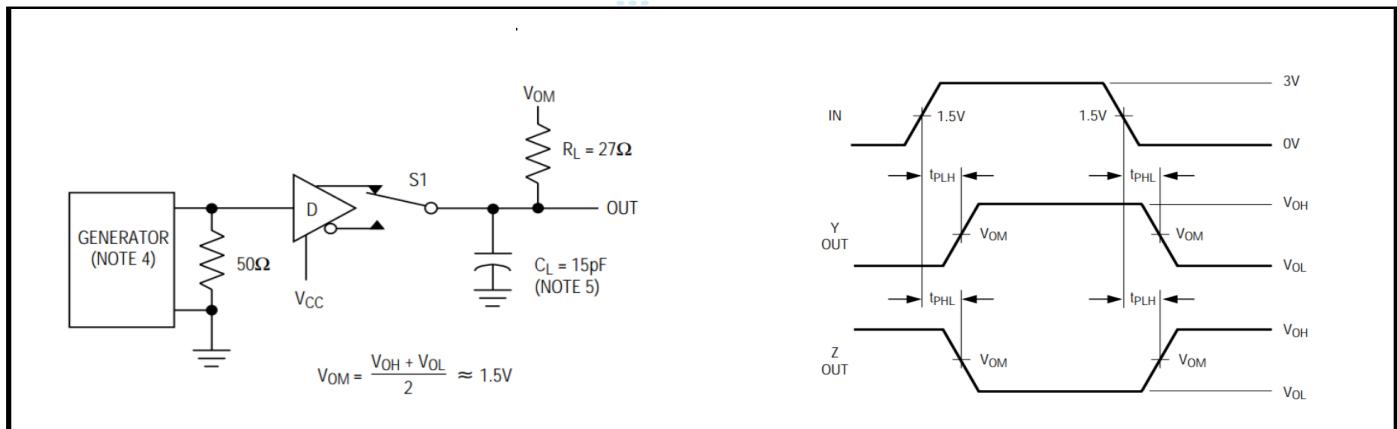


Figure 4 Propagation Delay of Driver

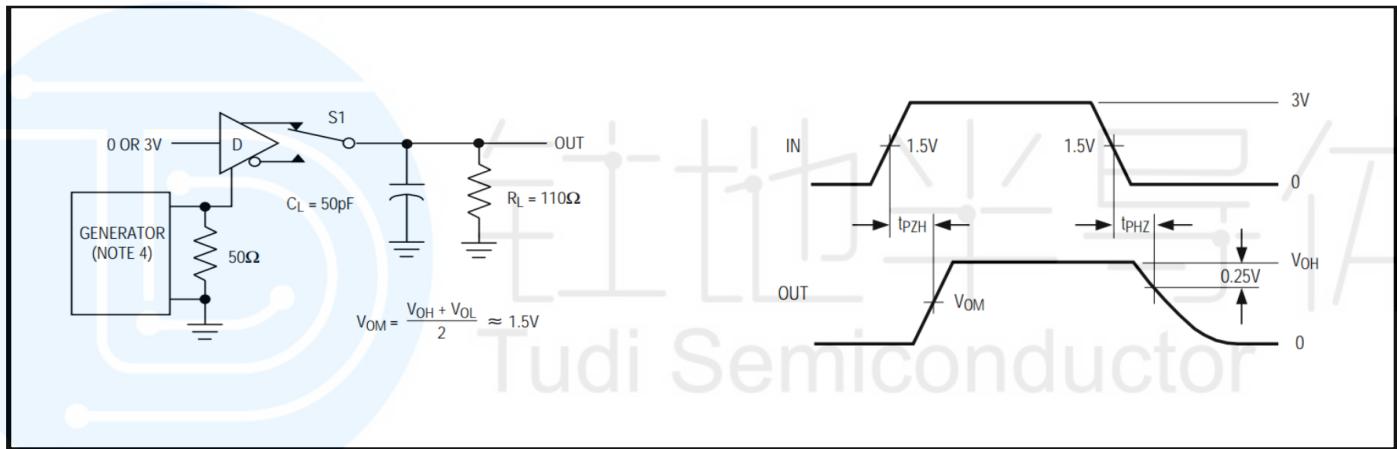


Figure 5 Driver enable and disable time

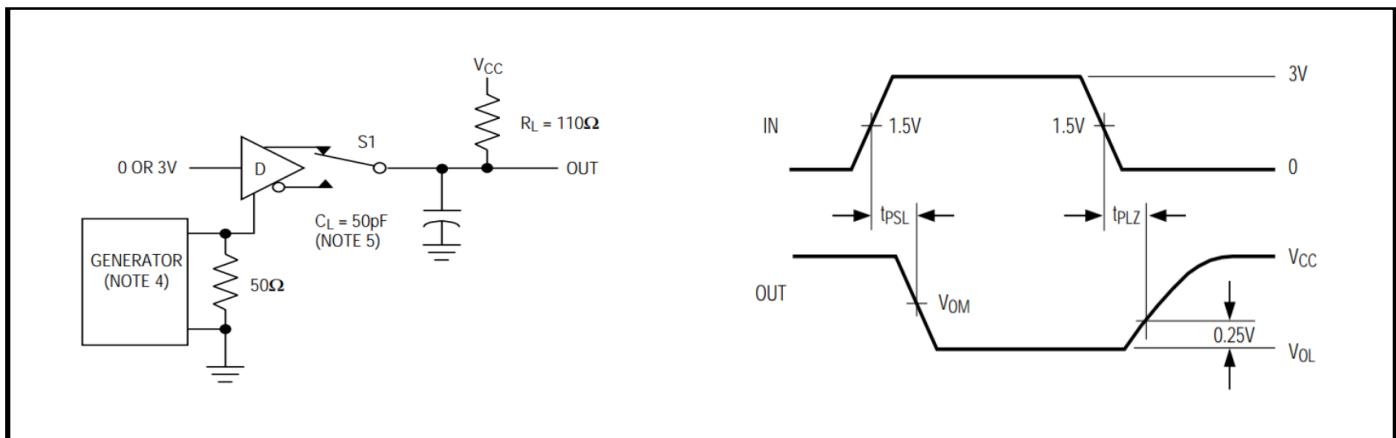


Figure 6 Driver enable and disable time

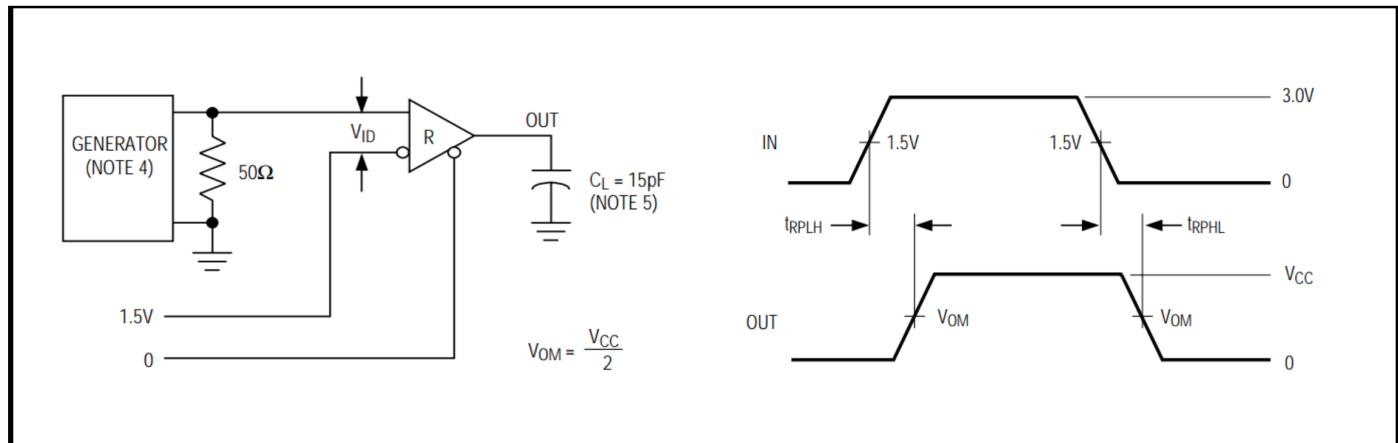


Figure 7 Receiver propagation delay test circuit

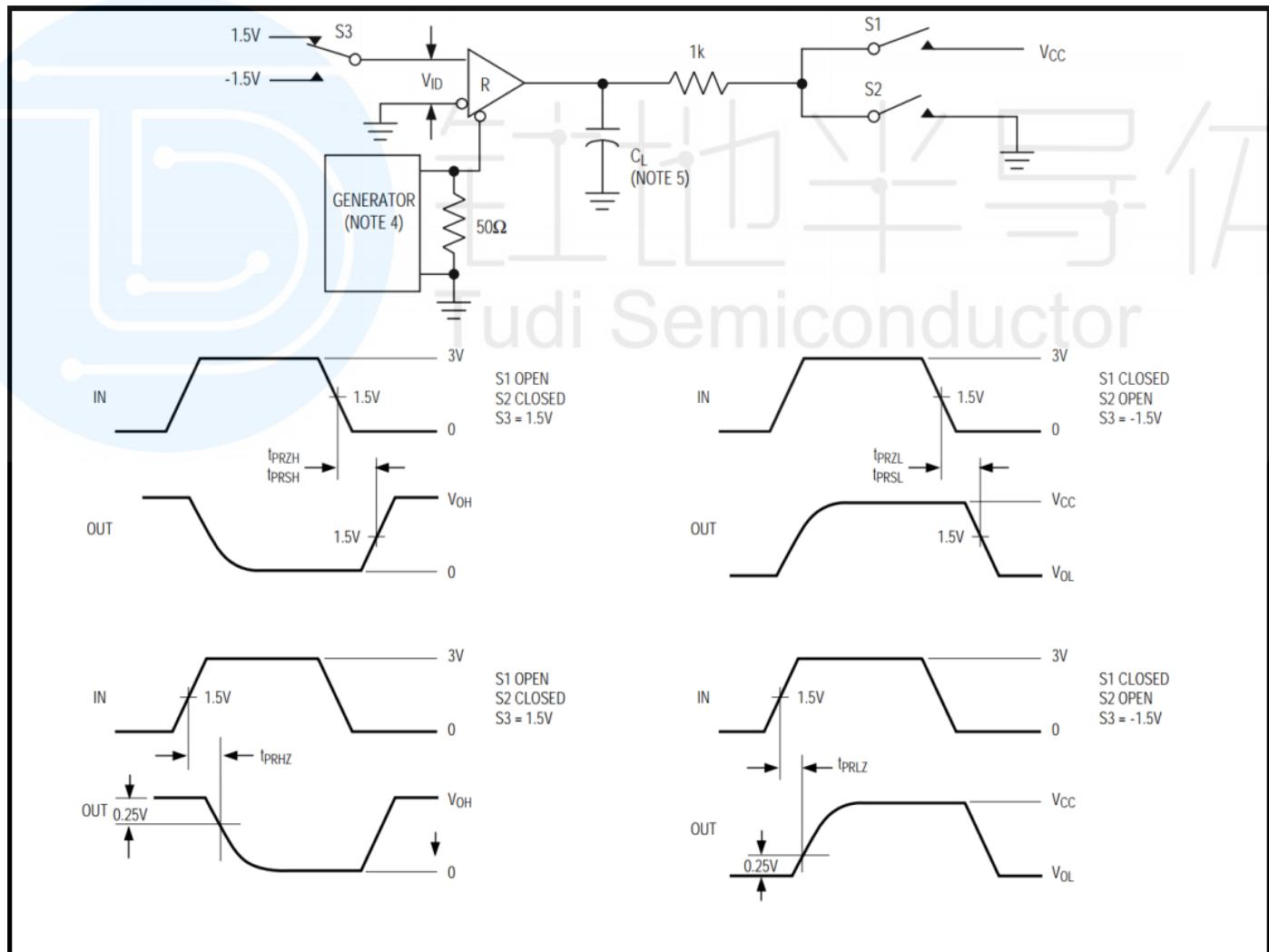


Figure 8 Receiver Enable and Disable Time

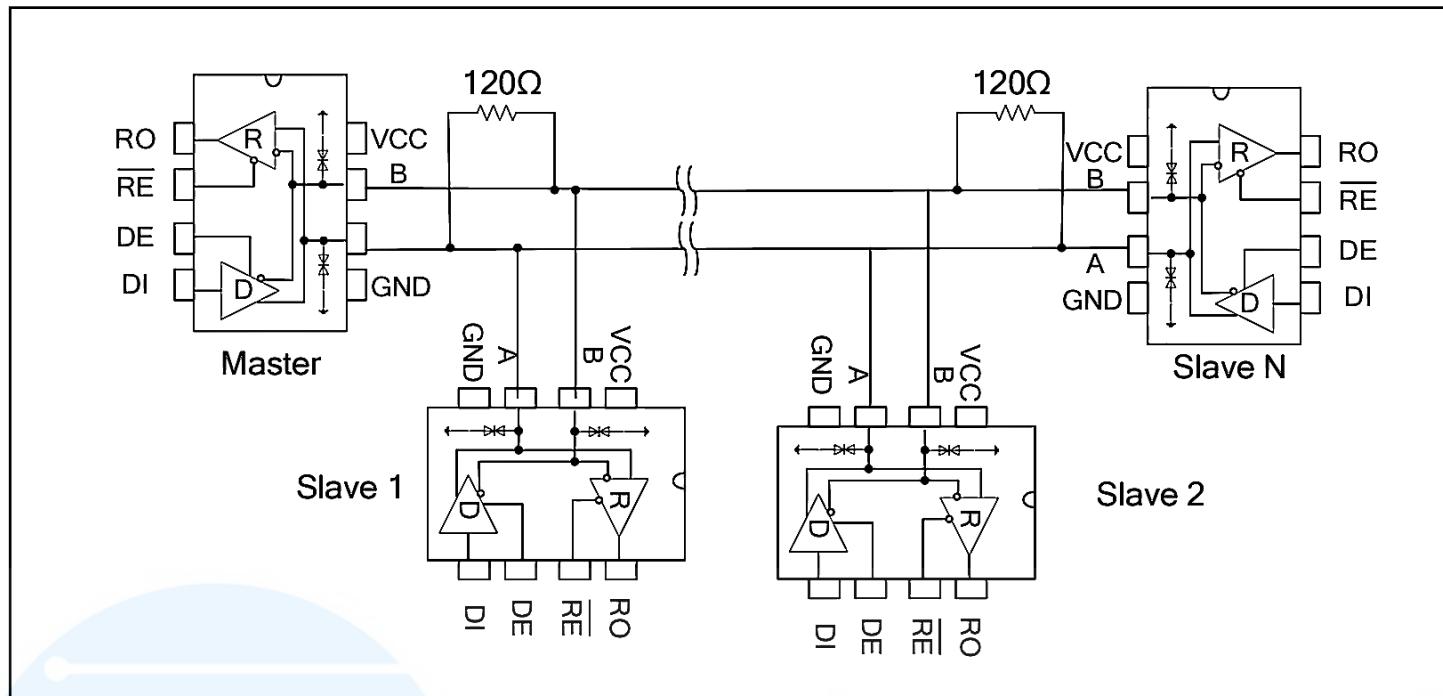


Fig11 Backbone cable type RS485 communications network

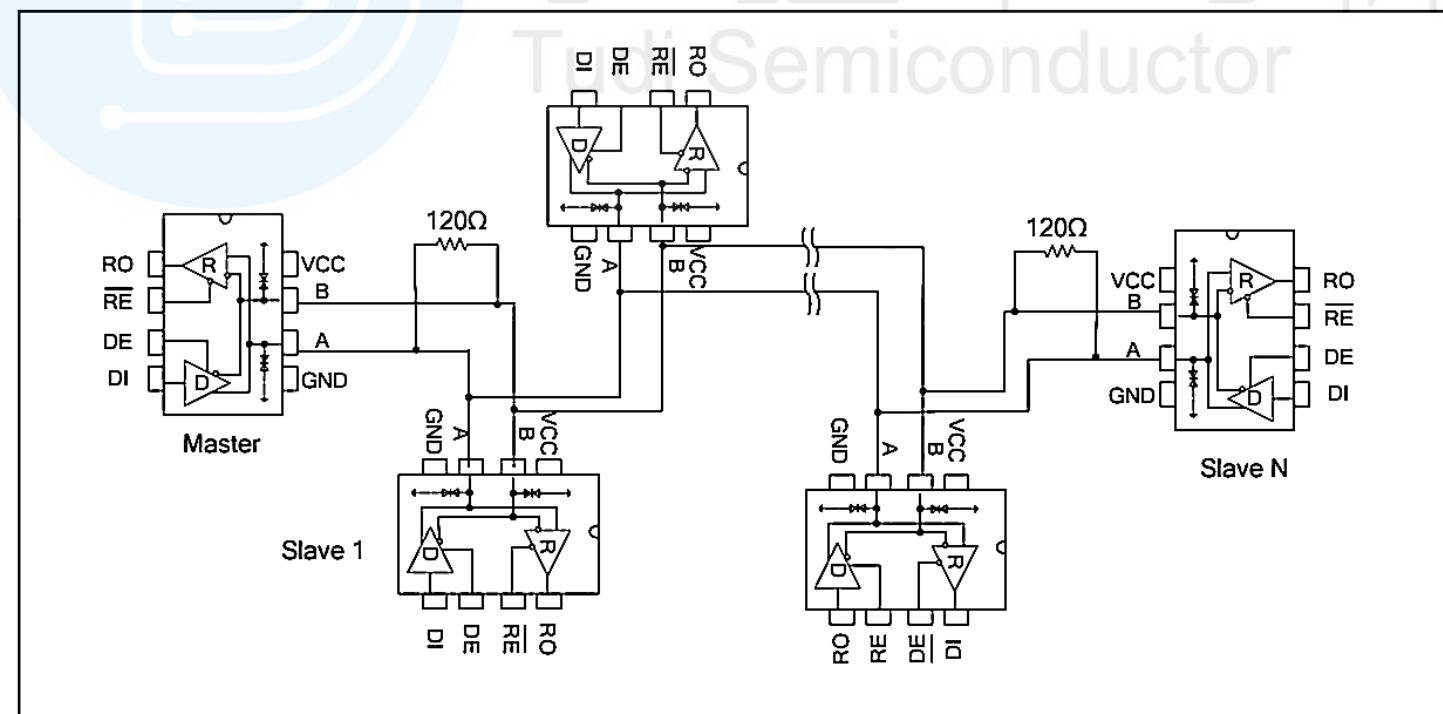


Fig12 Daisy chain topology type RS485 communications network

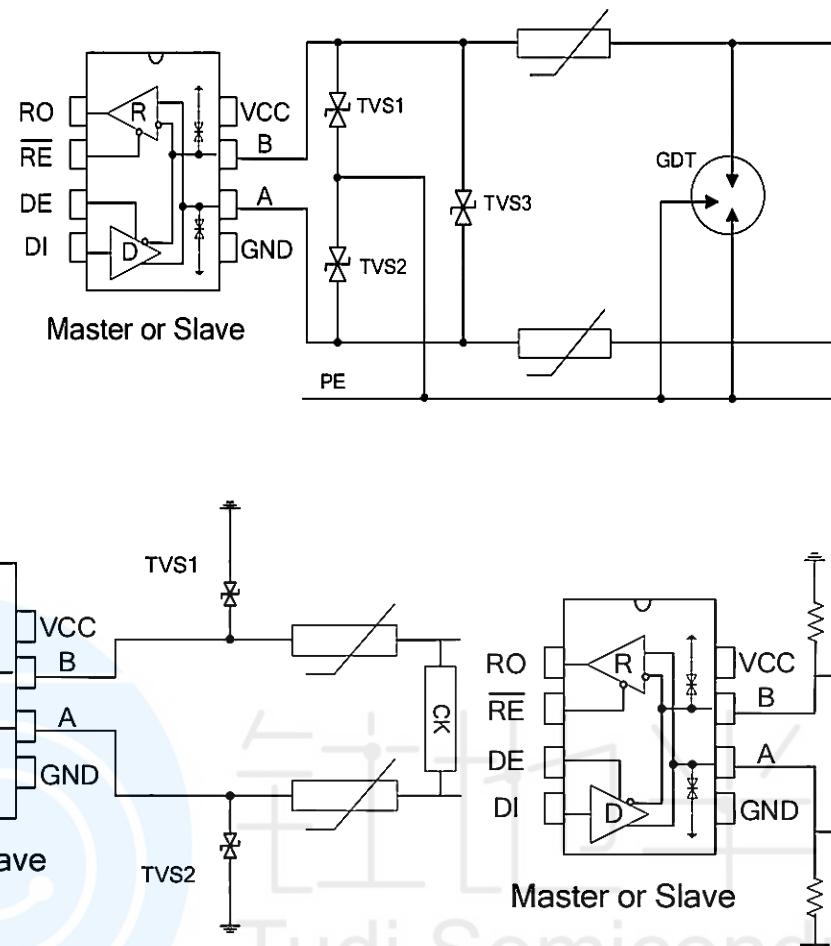


Fig13 RS485 bus ports Protection configuration

## Order information

Order Number	Package	Package Quantity	Marking On The park	Temperature
ADM3483ARZ-REEL-TUDI	SOP8	Tape,Reel,2500	ADM3483ARZ	- 40°C to 85°C
ADM3483ANZ-TUDI	DIP8	Tube,50,A box of 2000	ADM3483ANZ	



## Additional description

### Description

3483, including a driver and a receiver, is a half-duplex high-speed transceivers for RS-485 / RS-422 communications. 3483 features fail-safe, overvoltage protection, overcurrent protection, thermal protection, and allows / RE, DE hot-swappable. The 3483 allows an error-free data transmission up to 250Kbps.

### Typical Application

Backbone cable type: 3483 transceiver is designed for multi-point bi-directional data communication bus transmission lines. Figure 11 shows a typical network application circuit. These devices can also be used as a cable longer than 4,000 feet of line repeater, to reduce the reflection, the transmission line should be in its ends terminated in its characteristic impedance, and stub lengths off the main line should be as short as possible. Hand in hand type: Also known as daisy chain topology, is the prior RS485 bus topology recommended by the TIA organization. The routing method is the master device and a number of slave devices connected in hand-hand configuration, as shown in Figure 12. It should be noted at that hand in handle means no branch line. This kind of topology has the advantages of small reflection and high rate of success communication. The bus port protection : In harsh environments, RS485 communication ports are usually done with static protection, lightning surge protection, and other additional protection, even prepared to prevent 380V electricity access by mistake. To avoid the destruction of intelligent instruments and industrial control host, figure 13 demonstrates three general kinds of RS485 bus port protection configuration.

### Connecting 32 Transceivers on one Bus

The standard 3483 receiver input impedance is guaranteed  $>12k\Omega$ , the standard driver can drive up to 32 unit loads. These devices can be any combination, or in combination with other RS-485 transceiver combination, as long as the total load does not load more than 32 units, can be connected on the same bus.

### Drive Output Protection

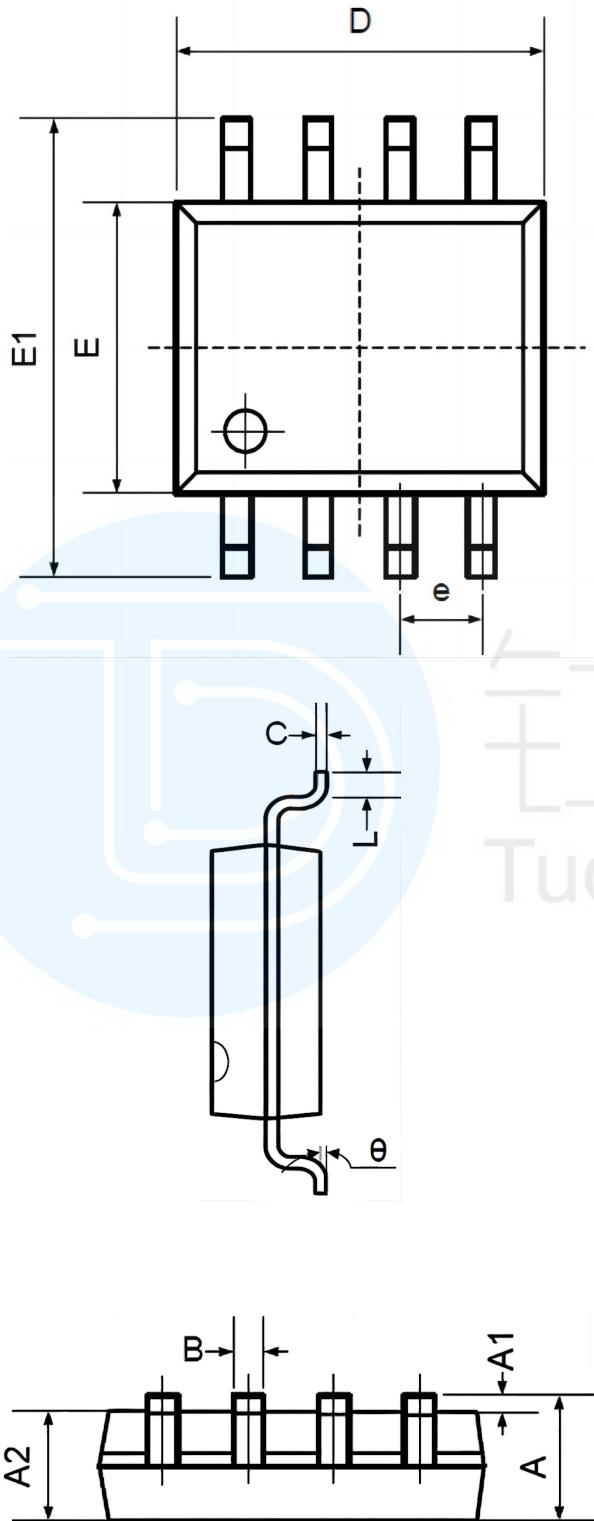
Through two mechanisms to avoid failure or a bus contention causes power consumption is too high. First, in the entire common Mode voltage range, overcurrent protection circuit provides a fast short protection. Second, when the die temperature exceeds  $150^{\circ}\text{C}$ , driver output is forced into a high impedance state by the thermal shutdown circuit.

### Fail Safe

When the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled, 3483 guarantees a logic-high receiver output. This is done by the receiver input thresholds are set between  $-10\text{mV}$  and  $-200\text{mV}$ . If the differential receiver input voltage  $(A-B) \geq -10\text{mV}$ , RO is logic high; if the voltage  $(A-B) \leq -200\text{mV}$ , RO is logic low. When attached to the terminal all transmitters on the bus are disabled, the receiver differential input voltage is pulled to  $0\text{V}$  by the termination resistor. With the receiver threshold of the 3483, this results in a logic-high with a  $10\text{mV}$  minimum noise margin. The  $-10\text{mV}$  to  $-200\text{mV}$  threshold complies with the  $\pm 200\text{mV}$  EIA/TIA-485 standard.



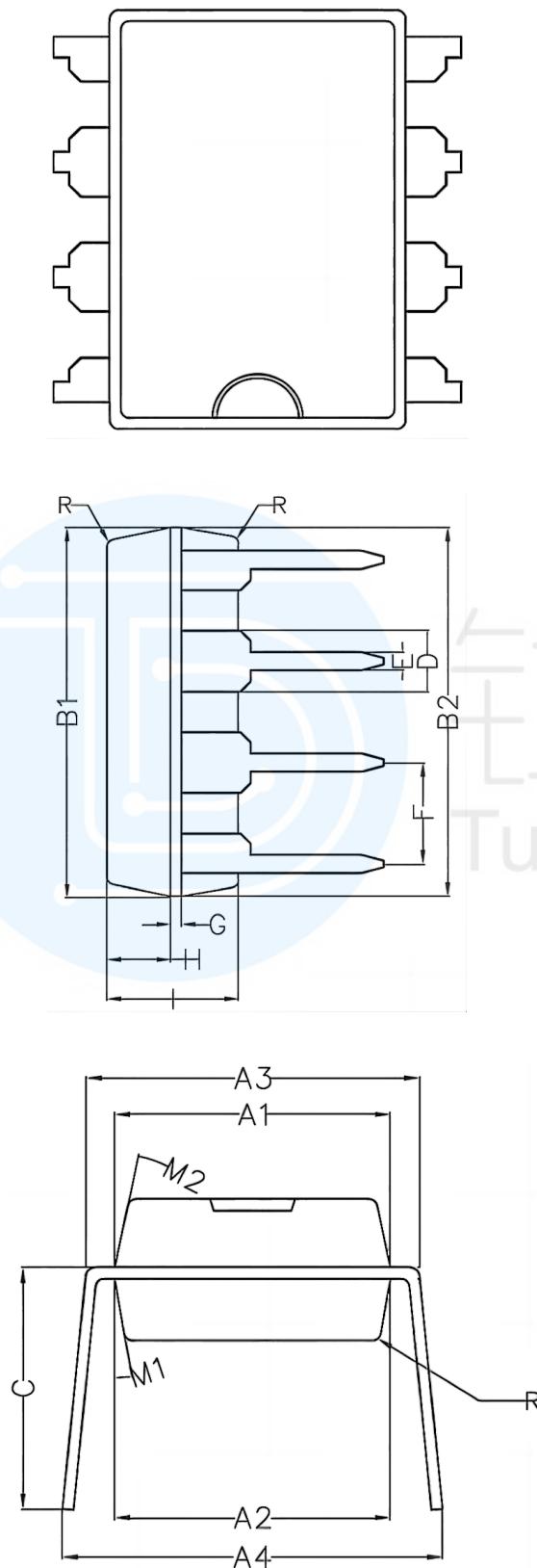
## Package SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



## Package DIP8



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
工	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°



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