General description

The LMX960D80 high-side N_FET driver works with an internal MOSFET and acts as hot swap circuit with power limiting function. The LMX960D80 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other hot power source, thereby limiting the voltage sag on the backplane's supply voltage and the dv/dt of the voltage applied to the load.

The current limit in the external series pass N-Channel MOSFET is programmable. The input undervoltage and overvoltage lockout levels are programmable by resistance divider networks. The LMX960D80 automatically restarts at a fixed duty cycle programmed by the Timer capacitor.

LMX960D80 is available in 10-pin DFN3*3 package.

Features

- ♦ Wide operating range: 9V to 40V
- ♦ Adjustable current limit
- ♦ Circuit breaker function for severe overcurrent events
- ♦ Internal high side charge pump and gate driver for N-channel MOSFET
- ♦ Adjustable undervoltage lockout (UVLO)
- ♦ Adjustable overvoltage lockout (OVP)
- ♦ Available with automatic restart
- ♦ 10-Pin DFN package

Applications

- ♦ Server backplane systems
- ♦ Base station power distribution systems
- ♦ 12-24V and 36V Industrial systems
- ♦ Programmable logic circuit
- ♦ Solid state circuit breaker

General information

Ordering information

Part Number	Description
LMX960D80	DFN33-10L
MPQ	3000pcs

Package dissipation rating

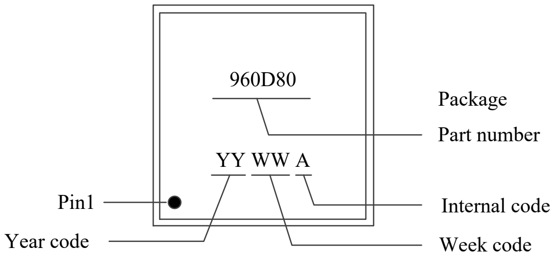
Package	RθJA（℃/W）
DFN3*3-10L	50

Absolute maximum ratings

Parameter	Value
VIN to GND	-0.3 to 60V
SENSE, OUT to GND	-0.3 to 60V
OUT to GND (1ms transient)	-0.3 to 60V
OVP, PWR, Timer to GND	-0.3 to 7V
VIN to SENSE	-0.3 to 0.3V
Maximum junction temperature, T_{JMAX}	150℃
Storage temperature, T_{stg}	-65 to 150℃

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

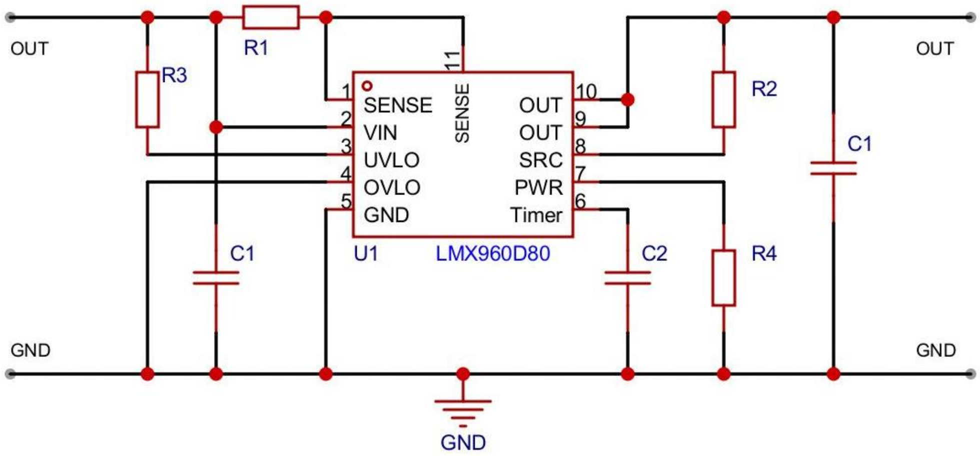
Marking information



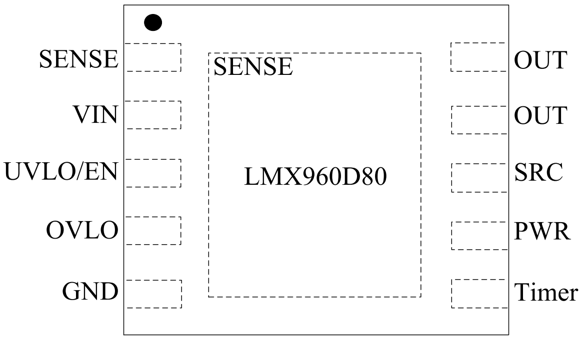
Recommended operating condition

Symbol	Range
Supply voltage	9 to 48V
OVP, PWR, Timer voltage	0 to 5V
Junction temperature	-40 to 125℃

Typical application

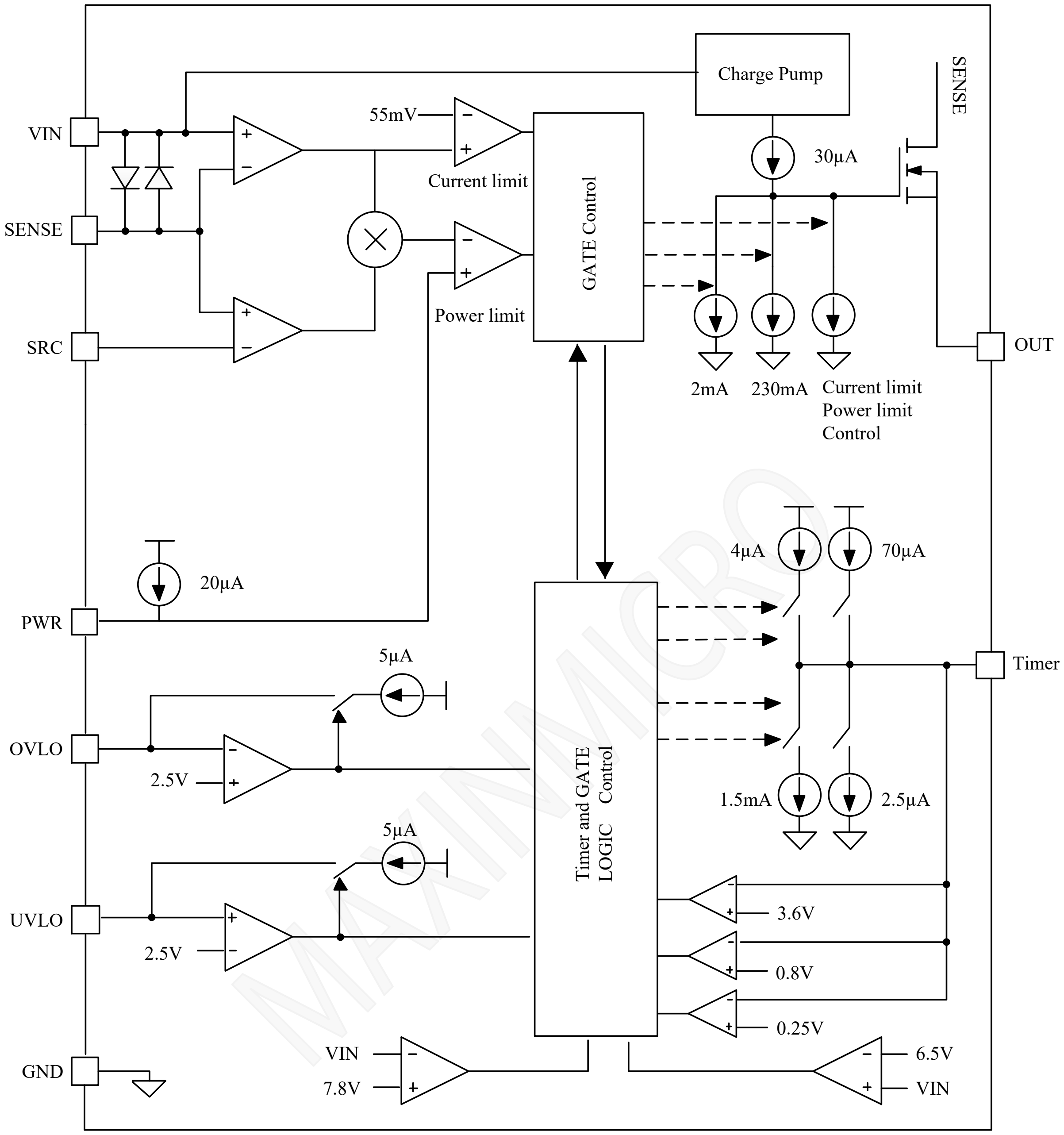


Terminal assignments



PIN num	PIN name	Description
1/11	**SENSE**	Current sense input: The voltage across the current sense resistor (R1) is measured from VIN to this pin. If the voltage across the R1 reaches 55mV the load current is limited and the fault timer activates.
2	**VIN**	Positive supply input: A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off.
3	**UVLO/EN**	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
4	**OVLO**	Overvoltage lockout: An external resistor divider from the system input voltage sets the overvoltage turnoff threshold. An internal 18µA current source provides hysteresis. The disable threshold at the pin is 2.5V typical.
5	**GND**	Circuit ground
6	**Timer**	Timing capacitor: An external capacitor connected to this pin sets the insertion time delay and the fault timeout period. The capacitor also sets the restart timing.
7	**PWR**	Current limit set: An external resistor connected to this pin, in conjunction with the current sense resistor, sets the maximum power dissipation allowed in the external series pass MOSFET.
8	**SRC**	Output feedback: Connect to the output rail (internal MOSFET source). Internally used to determine the MOSFET VDS voltage for power limiting. Connect this pin to OUT across a resistor, and a 100R is recommended.
9/10	**OUT**	System OUT pin.

Block diagram

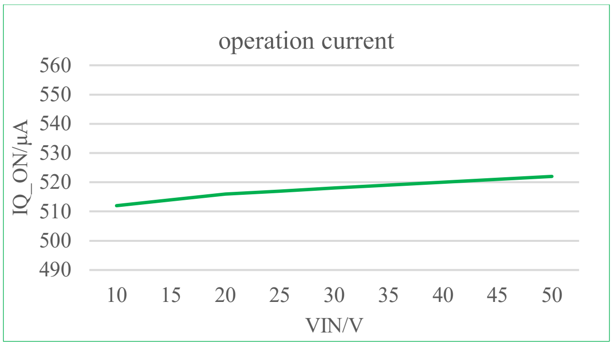


Electrical characteristics

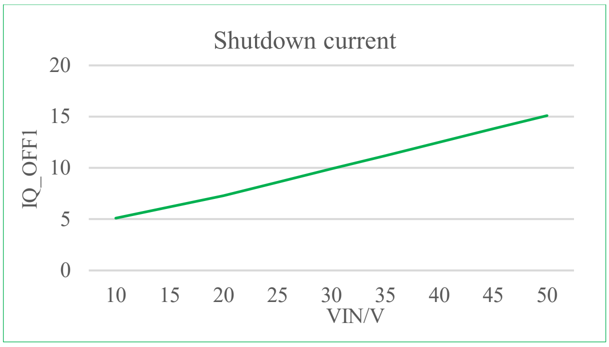
VIN = 12-36V, T_J = 25°C, unless otherwise noted.

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
INPUT (VIN PIN)						
VIN			9		48	V
IQ_{ON}	Supply current	UVLO/EN>2.5V and OVLO<2.5V		450		μA
IQ_{OFF}		VENH<EN/UVLO<VUVLOL	100		300	μA
IQ_{OFF1}		VENH<EN/UVLO<VUVLOL	0		25	μA
V_{INSERT}			5.5	6.5	7.5	V
V_{INEN}			6.8		8.5	V
UVLO/EN						
V_{UVLOL}	UVLO Threshold voltage	falling	2.25	2.5	2.75	V
$UVLO_{HYS}$	UVLO hysteresis current	UVLO/EN=1V	2	5	10	μA
$UVLO_{BIAS}$	UVLO bias current	UVLO/EN=48V			1	μA
V_{ENH}	EN Threshold voltage	rising	1.3	1.53	1.7	V
V_{ENL}	EN Threshold voltage	falling	0.5	0.68	0.9	V
OVLO						
V_{OVLOR}	OVLO Threshold voltage	Rising	2.25	2.5	2.75	V
$OVLO_{HYS}$	OVLO hysteresis current	OVLO=3V	2	5	10	μA
$OVLO_{BIAS}$	OVLO bias current	OVLO=2V			1	μA
OUT PIN						
I_{OUT_DIS}	OUT bias current, disabled	Disabled, OUT = 0V, SENSE = VIN		10		μA
I_{OUT_EN}	OUT bias current, enabled	Enabled, OUT=VIN		11		μA
PWR						
PWR_{ILM-1}	Power limit sense voltage (VIN-SENSE)	SEN-OUT=48V，RPWR=150kΩ	19	25	31	mV
PWR_{ILM-2}		SENSE-OUT=24V，RPWR=75 kΩ		25		mV
I_{PWR}	Power pin current	PWR=2.5V	17	20	23	μA
CURRENT LIMIT						
V_{CL}	Over current threshold	VIN-VSENSE	47	55	65	mV
I_{SENSE}	SENSE input current	Enable, OUT=SENSE		8		μA
		Disable, OUT=0V		10		μA
TIMER						
V_{TMRH}	Upper threshold	End of insertion time	3.2	3.6	4.0	V
V_{TMRL}	Lower threshold	Restart cycles	0.5	0.8	1.1	V
		End of 8th cycles		0.25		V
I_{TIMER}	Insertion time current	VIN=V_{INSERT}	2	4	6	μA
	Sink current, end of insertion time	Timer=2V	0.7		2	mA
	Fault detection current		45	70	95	μA
	Fault sink current		1.25	2.5	3.75	μA
DT_{FAULT}	Fault restart duty cycle			0.5		%
MOSFET						
VDS	Drain to Source voltage		60			V
Ron	On resistance	Vgs=10V		80		mR

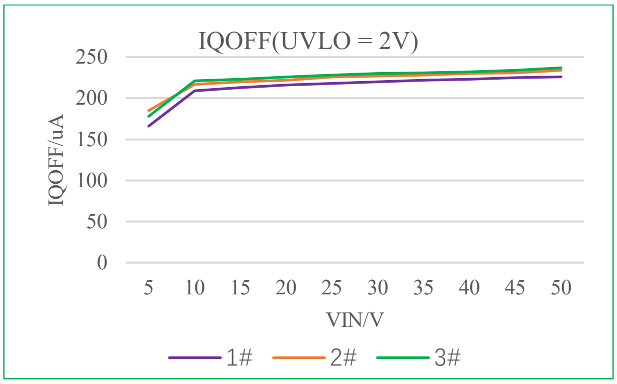
Characteristic plot (12-48V typical)



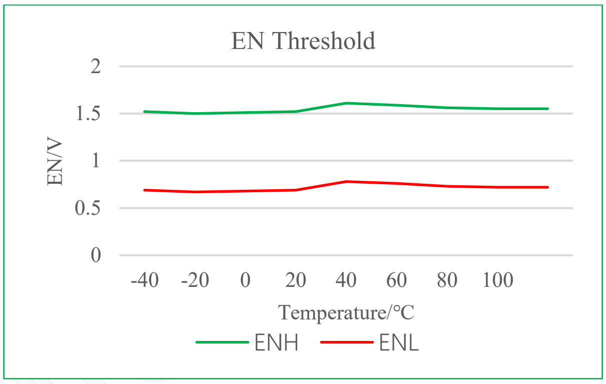
The operation current vs input voltage



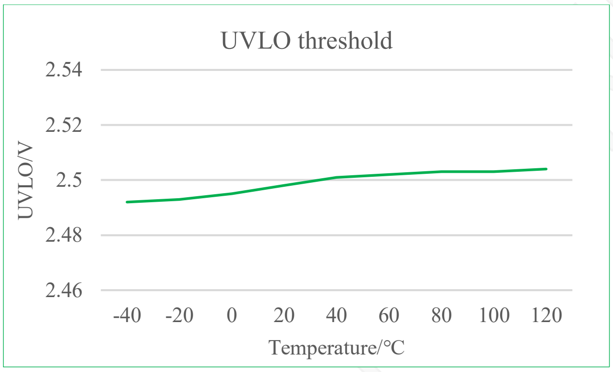
The shotdown current vs input voltage



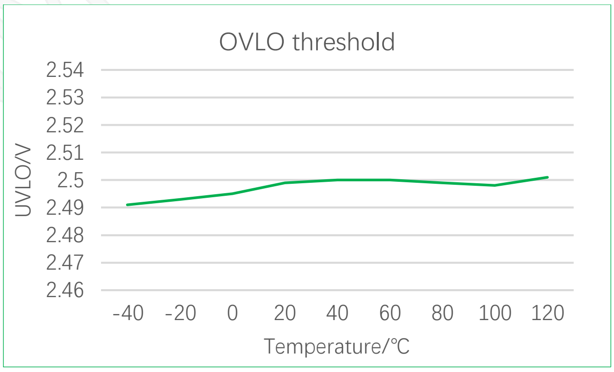
The UVLO current vs input voltage



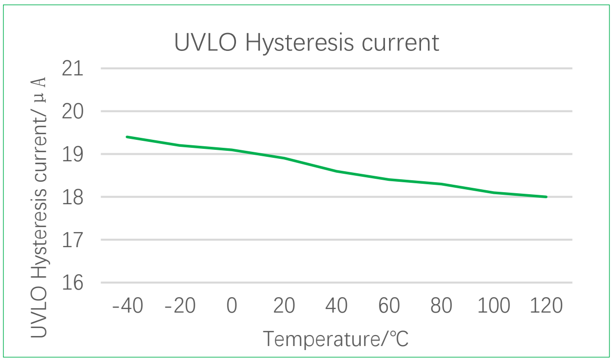
EN threshold vs temperature



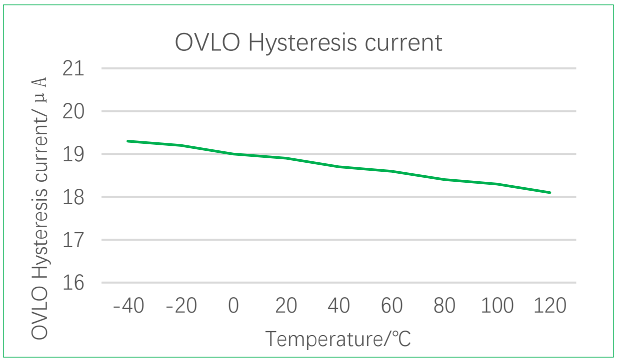
UVLO threshold vs temperature



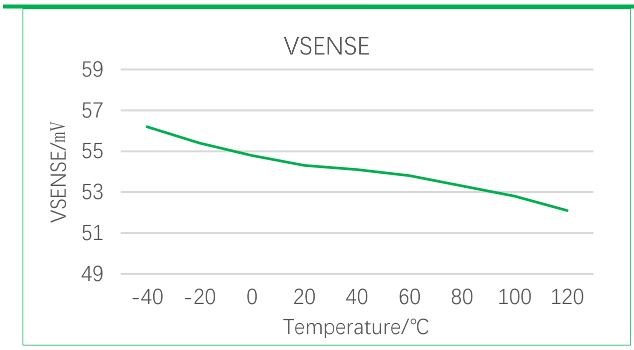
OVLO threshold vs temperature



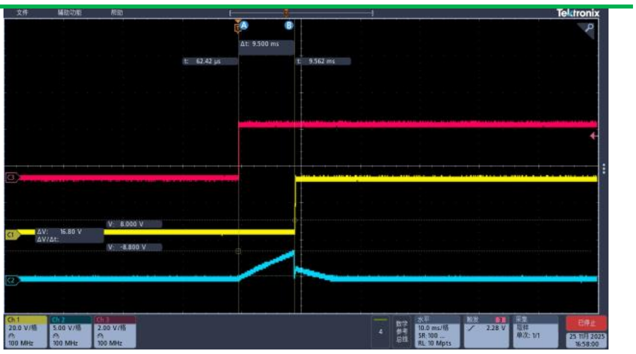
UVLO hysteresis current vs temperature



OVLO hysteresis current vs temperature

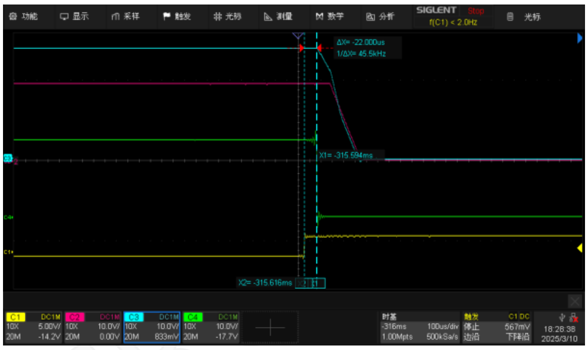


Current limit sense voltage vs temperature



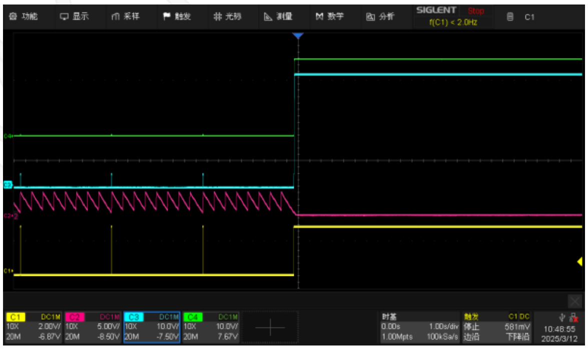
EN on

UVLO protection



OVLO protection

Over current protection



Over current release

Short circuit protection

Continues repeated switch on an off with 1A load

Detailed description

Overview

LMX960D80 have programmable current limit, current limiting for an extended period results in the shutdown of the series pass device. In this event, the LMX960D80 retries an infinite number of times to recover after the fault is removed. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition. Programmable undervoltage lockout (UVLO) and overvoltage lockout (OVP) circuits shut down the LMX960D80 when the system input voltage is outside the desired operating range.

In addition to a programmable current limit, the LMX960D80 monitors and limits the maximum power dissipation in the series pass device to maintain operation within the device Safe Operation Area. Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the LMX960D80 retries an infinite number of times to recover after the fault is removed. The circuit breaker function quickly switches off the series pass device upon detection of a severe overcurrent condition.

Undervoltage Lockout (UVLO)

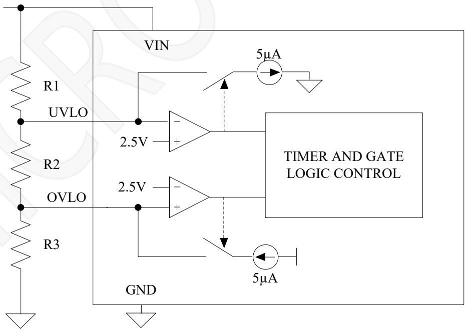
The series pass MOSFET is enabled when the input supply voltage is within the operating range defined by the programmable undervoltage lockout and overvoltage lockout levels. Typically, the UVLO level at VIN is set with a resistor divider as shown in the figure below. When VIN is below the UVLO level, the internal 5µA current source at UVLO is enabled, the current source at OVLO is off, and OUT is broken off. As VIN increases, raising the voltage at UVLO above 2.5V, the 5µA current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO pin above 2.5V, OUT is switched on by 30µA current source at the GATE pin if the insertion time delay has expired. The minimum possible UVLO level at VIN can be set by connecting the UVLO pin to VIN. In this case OUT is enabled when the VIN voltage reaches the V_{INEN} threshold.

By programming the UVLO and OVLO threshold the LMX960D80 enables the pass series MOSFET when the input supply voltage is within the desired operational range. If VIN is below the UVLO threshold, or above the OVLO threshold, OUT is switched off, denying power to the load. Hysteresis is provided for each threshold.

There are four methods to configure UVLO and OVLO to set the hysteresis threshold.

Option A

The configuration shown in the following figure requires three resistors (R1-R3) to set the threshold.



The procedure to calculate the resistor values is as follows：

1. Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL}).
2. Choose the upper OVLO threshold (V_{OVH}).
3. The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case but is determined after the values for R1-R3 are determined.

The resistors are calculated with Equation1, Equation2 and Equation3.

$$R1=\frac{V_{UVH}-V_{UVL}}{5\mu A}=\frac{V_{UV(HYS)}}{5\mu A} \qquad (1)$$

$$R3=\frac{2.5\times R1\times V_{UVL}}{V_{OVH}\times(V_{UVL}-2.5V)} \qquad (2)$$

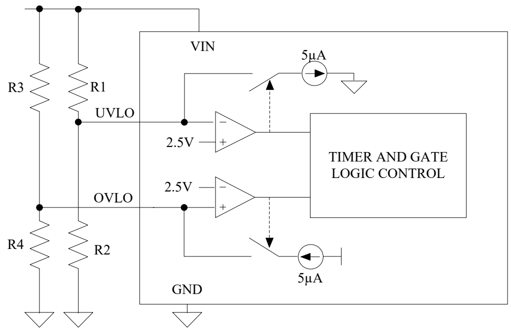
$$R2=\frac{2.5V\times R1}{V_{UVL}-2.5V}-R3 \qquad (3)$$

The lower OVLO threshold is calculated from Equation4.

$$V_{OVL} = \left[(R1 + R2) \times \left(\frac{2.5V}{R3} - 5\mu A\right)\right] + 2.5V \qquad (4)$$

Option B

If all four thresholds must be accurately defined, the following figure can be used.



The four resistor values are calculated as follows:

1. Choose the upper UVLO threshold (V_{UVH}) and lower UVLO threshold (V_{UVL}) with Equation5 and Equation6.

$$R1 = \frac{V_{UVH} - V_{UVL}}{5\mu A} = \frac{V_{UV(HYS)}}{5\mu A} \qquad (5)$$

$$R2 = \frac{2.5V \times R1}{V_{UVL} - 2.5V} \qquad (6)$$

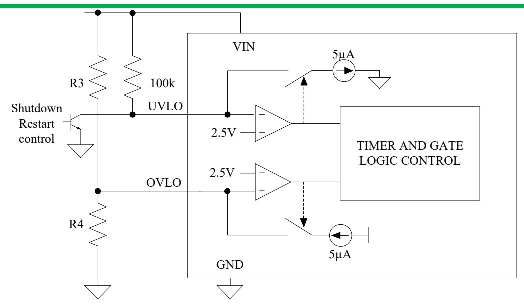
2. Choose the upper OVLO threshold (V_{OVH}) and lower OVLO threshold (V_{OVL}) with Equation7 and Equation8.

$$R3 = \frac{V_{OVH} - V_{OVL}}{5\mu A} = \frac{V_{OV(HYS)}}{5\mu A} \qquad (7)$$

$$R4 = \frac{2.5V \times R3}{V_{OVH} - 2.5V} \qquad (8)$$

Option C

The minimum UVLO level is obtained by connecting the UVLO pin to VIN as shown in the following figure. Q1 is switched on when the VIN voltage reaches V_{INEN} threshold. An external transistor can be connected to UVLO to provide remote shutdown control. The OVLO threshold is set using R3, R4. Their values are calculated using the method in Option B.



Option D

The OVLO function can be disabled by grounding the OVLO pin. The UVLO thresholds are set as described in Option B and Option C.

Overvoltage Lockout (OVLO)

The series pass MOSFET is enabled when the input supply voltage is within the operating range defined by the programmable undervoltage lockout and overvoltage lockout level. If VIN raises the OVLO pin voltage above 2.5V, the LMX960D80 denying power to the load. When the OVLO pin is above 2.5V, the OUT is switched on.

Power up sequence

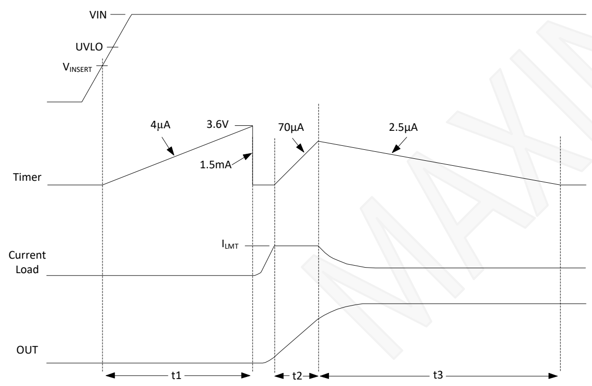
The VIN operating range of the LMX960D80 is 9V to 48V. As the VIN initially increases, the internal NMOSFET is held off an 230mA pulldown current at the internal GATE. The strong pulldown current at the GATE pin prevents an inadvertent turn on as the MOSFET's gate to drain capacitance is charged. Additionally, the Timer pin is initially held at ground. When the VIN voltage reaches the VINSERT threshold the insertion time begins. During the insertion time, the capacitor at the Timer pin is charged by a 4µA current source, and internal MOS is held off by a 2mA pulldown current at the internal GATE regardless of the VIN voltage. The insertion time delay allows ringing and transient at VIN to settle before MOS can be enabled.

The insertion time ends when the Timer pin voltage reaches 3.6V. The capacitor is the quickly discharged by an internal 1.5mA pulldown current. After the insertion time, the LMX960D80 control circuity is enabled when VIN reaches the

VINEN threshold. The internal power pass is switched on when VIN exceeds the UVLO threshold. If VIN is above the UVLO threshold at the end of the insertion time, OUT switches on at that time.

As the voltage at the OUT pin increases, the LMX960D80 monitors the drain current and power dissipation of MOSFET. In rush current limiting and power limiting circuits actively control the current delivered to the load. During the in rush limiting interval an internal 70μA fault timer current source charges the timer capacitor. If the power dissipation and the input current reduce below their respective limiting threshold before the Timer pin reaches 3.6V, the current 70μA source is switched off, and the capacitor is discharged by the internal 2.5μA current sink.

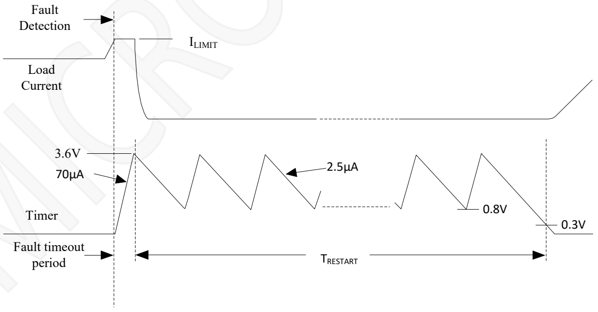
The Timer pin voltage 3.6V before in rush current limiting or power limiting ceases, a fault is declared and OUT is turned off.



Fault timer and restart

When the current limit or power limit threshold is reached during turn on or as result of a fault condition, the internal gate to source voltage is modulated to regulate the load current and power dissipation. When either function is activated, an 70μA fault timer current source charged the external capacitor at the Timer pin. If the fault condition subsides during the fault timeout period before the Timer pin reaches 3.6V, the LMX960D80 returns to the normal operating mode, and the Timer capacitor is discharged by the 2.5μA current sink. If the Timer pin reaches 3.6V during the fault timeout period, OUT will be switched off.

The LMX960D80 provides an automatic restart sequence which consists of the Timer pin cycling between 3.6V and 0.8V seven times after the fault timeout period as shown in the following figure. The period of each cycle is determined by the 70μA charging current, and the 2.5μA discharging current, and the value of the capacitor at Timer pin. When the Timer pin reaches 0.3V during the eight high to low ramp, the OUT will be switched on. If the fault condition is still present, the fault timeout period and the restart cycle repeat.



The fault timer runs when the hot swap is in power limit or current limit, which is the case during start up. Thus the timer has to be sized large enough to prevent a time out during start up. If the part starts directly into current limit the maximum start time can be computed with Equation9.

$$t_{start,max} = \frac{C_{OUT} \times V_{INMAX}}{I_{LIM}} \qquad (9)$$

For most designs, $I_{LIM} \times V_{DS} > P_{LIM}$, so the hot swap starts in power limit and transition into current limit. In that case, the estimated start time can be computed with Equation10.

$$t_{start} = \frac{C_{OUT}}{2} \times \left(\frac{V_{INMAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2}\right) \qquad (10)$$

Note that the above start time assumes constant, typical current limit and power limit values. The actual start up time is slightly longer, as the power limit is a function of VDS and decreases as the output voltage increases. To ensure that the timer never times out during start up, we recommend setting the minimum fault time to be greater than the startup time by adding an additional 50% of the fault time. This accounts for the variation in power limit, timer current and timer capacitance. Thus the charge time can be computed with Equation11.

$$t_{FLT} = \frac{C_{Timer}\times 3.6V(typ)}{70\mu A(typ)} \qquad (11)$$

Current Limit

The current limit threshold reached when the voltage across the sense resistor R_S (VIN to SENSE) reaches 55mV. In the current limiting condition, the internal GATE voltage is controlled to limit the current in pass MOSFET. While the current limit circuit is active, the fault SST is active. If the load current falls below the current limit threshold before the end of the fault timeout period. For proper operation, the RS resistor value must be no larger than 100mΩ.

When VIN=36V, the Timer capacitor and PWR resistor can reference the following table.

Rsense=50mΩ		
Iocp=1.1A		
Timer	Debounce time	PWR
100nF	6.3ms	≤51kΩ
10nF	0.9ms	≤100kΩ
1nF	78us	≤820kΩ

Input and Output Protection

Proper operation of the LMX960D80 hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Typical application. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shuts off. The TVS must be chosen to have minimal leakage current at V_{INMAX} and to clamp the voltage to under 30V during hot-short events. A 100~200ohm resistor should be placed between OUT pin and Source of external MOSFET to prevent damage from surge voltage, as the R_{SOURCE} shown in the Typical application.

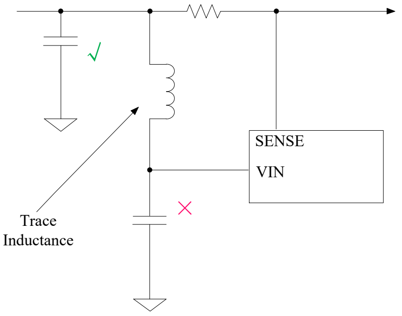
Power Supply Recommendations

In general, the LMX960D80 behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, Maxin recommends placing a 1μF ceramic capacitor to ground close to the drain of the hot swap MOSFET. This reduces the common mode voltage seen by VIN and SENSE. Additional filtering may be necessary to avoid nuisance trips.

Layout Guidelines

The following guidelines must be followed when designing the PC board for the LMX960D80:

- Note that special care must be taken when placing the bypass capacitor for the VIN pin. During hot shorts, there is a very large dv/dt on input voltage after the internal MOSFET turns off. If the bypass capacitor is placed right next to the pin and the trace from R_{SENSE} to the pin is long, an LC filter is formed. As a result, a large differential voltage can develop between VIN and SENSE. To avoid this, place the bypass capacitor close to R_{SENSE} instead of the VIN pin.



Layout Trace Inductance

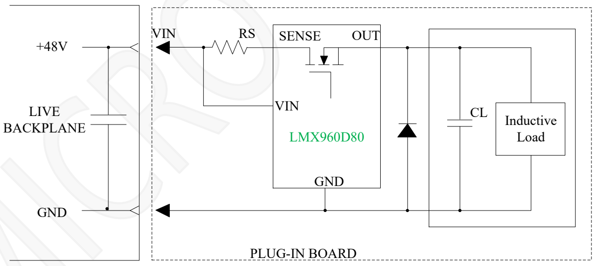
- The sense resistor (R_S) must be close to the LMX960D80, and connected to it using the Kelvin techniques.

- The ground connection for the various components around the LMX960D80 must be connected directly to each other, and to the LMX960D80's GND pin, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- The board's edge connector can be designed to shut off the LMX960D80 as the board is removed, before the supply voltage is disconnected from the LMX960D80. When the board is inserted into the edge connector, the system voltage is applied to the LMX960D80's VIN pin before the UVLO voltage is taken high.

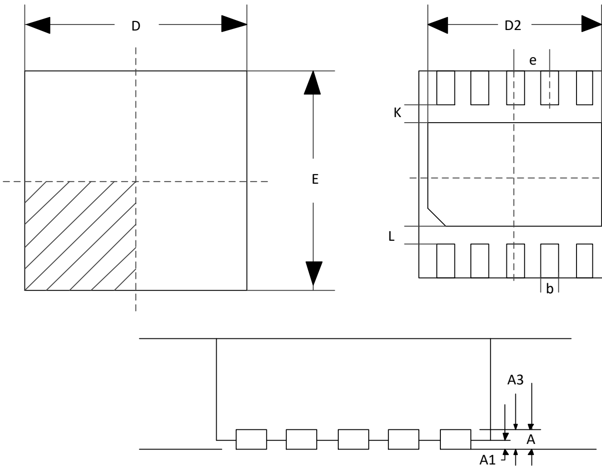
System Considerations

A) Continued proper operation of the LMX960D80 hot swap circuit requires capacitance be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in the following figure. The capacitor in the Live Backplane section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines generates a transient voltage at shut-off which can exceed the absolute maximum rating of the LMX960D80, resulting in its destruction.

B) If the load powered via the LMX960D80 hot swap circuit has inductive characteristics, a diode is required across the LMX960D80's output. The diode provides a recirculating path for the load's current when the LMX960D80 shuts off that current. Adding the diode prevents possible damage to the LMX960D80 as the OUT pin is taken below ground by the inductive load at shutoff.



Package information DFN3*3-10L



DFN3*3-10L for LMX960D80DL

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0.00	0.03	0.05	0.00	0.0012	0.0020
A3	0.20BSC			0.008BSC		
b	0.18	0.24	0.30	0.007	0.009	0.011
D	3.00BSC			0.12BSC		
D2	2.45	2.50	2.55	0.096	0.098	0.100
E	3.00BSC			0.12BSC		
E2	1.75	1.80	1.85	0.069	0.071	0.073
e	0.50BSC			0.02BSC		
K	0.19TYP			0.0075BSC		
θ	0.35	0.40	0.45	0.014	0.016	0.018

Restrictions on Product Use

- MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

- In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

- The information contained herein is subject to change without notice.

Version update record:

V10 The original version

V11 Official release version