UMW NTD2955T4G

-60V P-Channel MOSFET

1.Description

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low−voltage, high speed switching applications in power supplies, converters, and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer an additional safety margin against unexpected voltage transients.

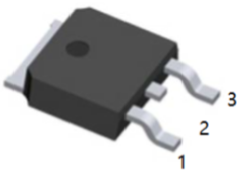
2.Features

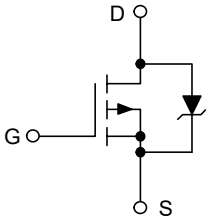
- $V_{DS\ (V)}$=-60V
- I_D=-20A
- $R_{DS(ON)}$=53mΩ
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(ON)}$ Specified at Elevated Temperature
- Designed for Low−Voltage, High−Speed Switching Applications and to Withstand High Energy in the Avalanche and Commutation Modes

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_C= 25°C

Parameter	Symbol	Rating	Units
Drain-to-Source Voltage	V_{DSS}	-60	V_{dc}
Gate-to-Source Voltage-Continuous	V_{GS}	±20	V_{dc}
-Non-repetitive (t_P≤ 10 ms)	V_{GSM}	±25	V_{pk}
Drain Current-Continuous @T_A= 25°C	I_D	-12	A_{dc}
-Single Pulse (t,≤ 10 ms)	I_{DM}	-36	A_{pk}
Total Power Dissipation @T_A= 25°C	P_D	55	W
Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C

Single Pulse Drain-to-Source Avalanche Energy-Starting Tj= 25°C (V_{DD}=25Vdc, V_{GS}=10Vdc, Peak I_L=12Apk,L=3.0 mH, R_G=25Ω)	E_{AS}	216	mJ
Thermal Resistance-Junction-to-Case	$R_{\theta JC}$	2.73	°C/W
-Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	°C/W
-Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	°C/W
Maximum Lead Temperature for SolderingPurposes, 1/8 in. from case for10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in pad size (Cu area = 1.127 in^2).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu area = 0.412 in^2)

5.Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

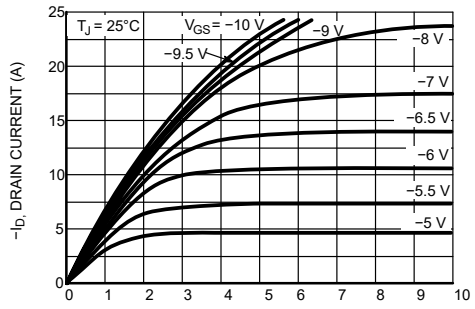
Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0Vdc, I_D=-0.25mA	-60			Vdc
(Positive Temperature Coefficient) (Note 3)				67		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0Vdc, V_{DS}=-60V, T_J=25°C			-10	μAdc
		V_{GS}=0Vdc,V_{DS}=-60V,T_J=150°C			-100	μAdc
Gate−Body Leakage Current	I_{GSS}	V_{GS}=±20Vdc, V_{DS}=0Vdc			±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Negative Temperature Coefficient)	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μAdc	-1.1	-2	-3	V
Static Drain−Source On−State Resistance	$R_{DS(ON)}$	V_{GS}=-10Vdc, I_D=-6Adc		150	170	mΩ
Drain−to−Source On−Voltage	$V_{DS(ON)}$	V_{GS}=-10Vdc,I_D=-12Adc		-1.86	-2.6	Vdc
		V_{GS}=-10Vdc,I_D=-6Adc,T_J=150°C			-2	Vdc
Forward Transconductance	g_{FS}	V_{DS}=10Vdc, I_D=6Adc		8		Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{DS}=-25Vdc, V_{GS}=0Vdc f=1MHz		500	750	pF
Output Capacitance	C_{oss}			150	250	pF
Reverse Transfer Capacitance	C_{rss}			50	100	pF
SWITCHING CHARACTERISTICS (Notes 3 and 4)						
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=-30Vdc, I_D=-12A V_{GS}=-10V, R_G=9.1Ω		10	20	ns
Rise Time	t_r			45	85	ns
Turn-Off Delay Time	$t_{D(off)}$			26	40	ns
Fall Time	t_f			48	90	ns
Gate Charge	Q_T	V_{DS}=-48Vdc, V_{GS}=-10Vdc I_D=-12A		15	30	nC
	Q_{GS}			4		nC
	Q_{GD}			7		nC

DRAIN−SOURCE DIODE CHARACTERISTICS (Note 3)						
Reverse Recovery Time	V_{SD}	I_S=12Adc, V_{GS}=0V		-1.6	-2.5	Vdc
		I_S=12Adc, V_{GS}=0V, T_J=150°C		-1.3		Vdc
Reverse Recovery Time	t_{rr}	I_S=12A, dI_S/dt=100 A/μs V_{GS}=0 V		50		ns
	t_a			40		ns
	t_b			10		ns
Reverse Recovery Stored Charge	Q_{rr}			0.1		μC

3. Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

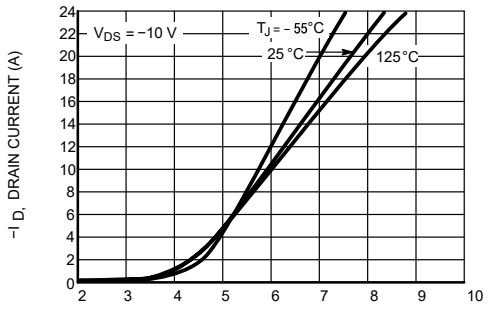
4. Switching characteristics are independent of operating junction temperature.

6.1Typical Characterisitics



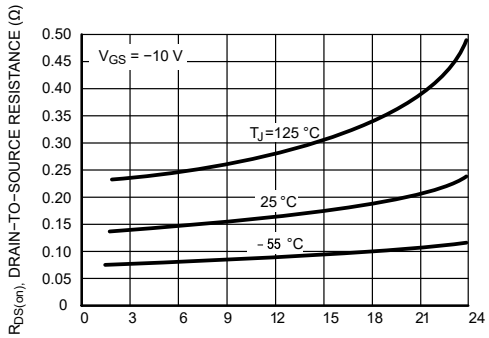
$-V_{DS}$, DRAIN−TO−SOURCE VOLTAGE (VOLTS)

Figure 1: On−Region Characteristics



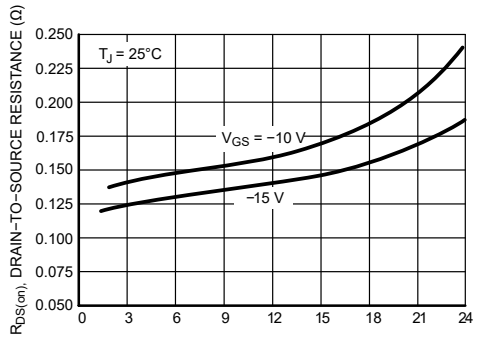
$-V_{GS}$, GATE−TO−SOURCE VOLTAGE (VOLTS)

Figure 2: Transfer Characteristics



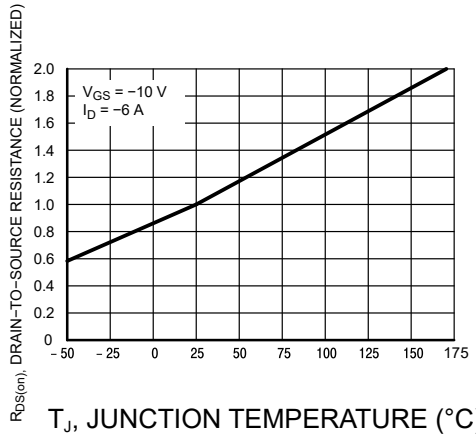
$-I_D$, DRAIN CURRENT (AMPS)

Figure 3: On−Resistance versus Drain Current and Temperature



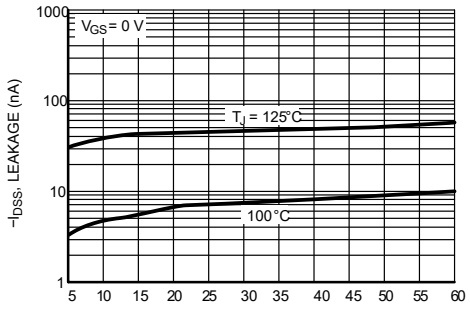
-I_D, DRAIN CURRENT (AMPS)

Figure 4: On−Resistance versus Drain Current and Gate Voltage



T_J, JUNCTION TEMPERATURE (°C)

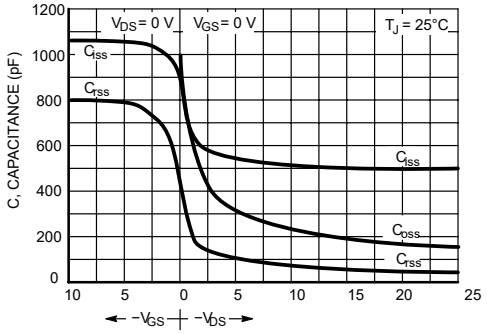
Figure 5: On−Resistance Variation with Temperature



$-V_{DS}$, DRAIN−TO−SOURCE VOLTAGE (VOLTS)

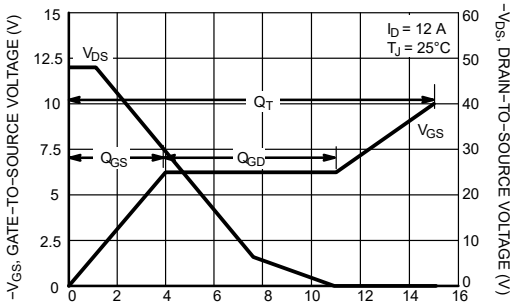
Figure 6: . Drain−To−Source Leakage Current versus Voltage

6.2Typical Characterisitics



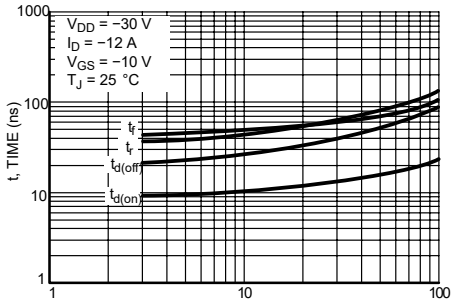
GATE−TO−SOURCE OR DRAIN−TO−SOURCE VOLTAGE (V)

Figure 7: Capacitance Variation



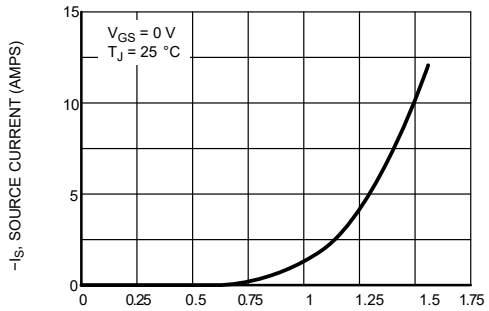
Q_T, TOTAL GATE CHARGE (nC)

Figure 8: Gate−To−Source and Drain−To−Source Voltage versus Total Charge



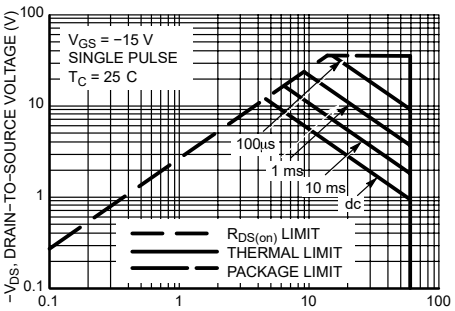
R_G, GATE RESIRTANCE (Ω)

Figure 9: Resistive Switching Time Variation versus Gate Resistance



$-V_{SD}$, SOURCE−TO−DRAIN VOLTAGE (V)

Figure 10: Diode Forward Voltage versus Current



$-V_{DS}$, DRAIN−TO−SOURCE VOLTAGE (V)

Figure 11: Maximum Rated Forward Biased Safe Operating Area

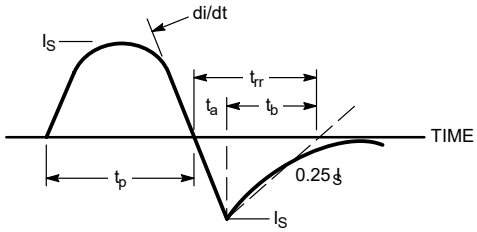


Figure 12: Diode Reverse Recovery Waveform

6.3Typical Characterisitics

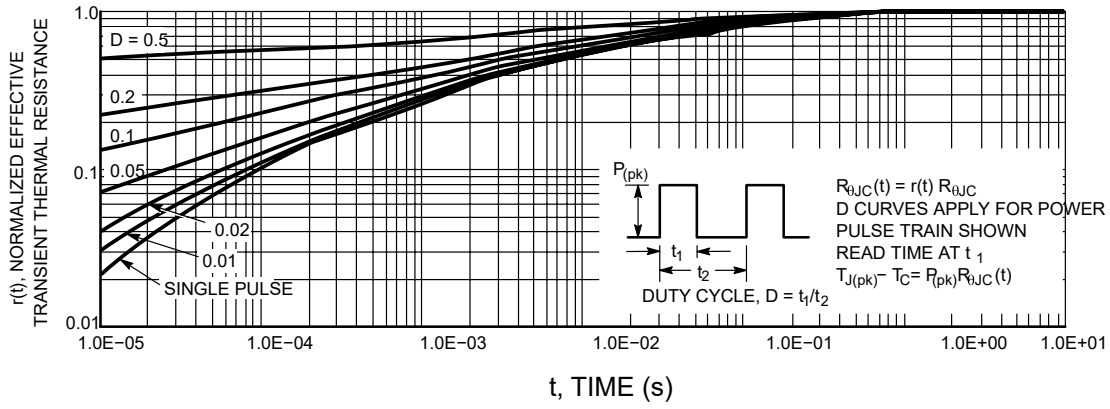
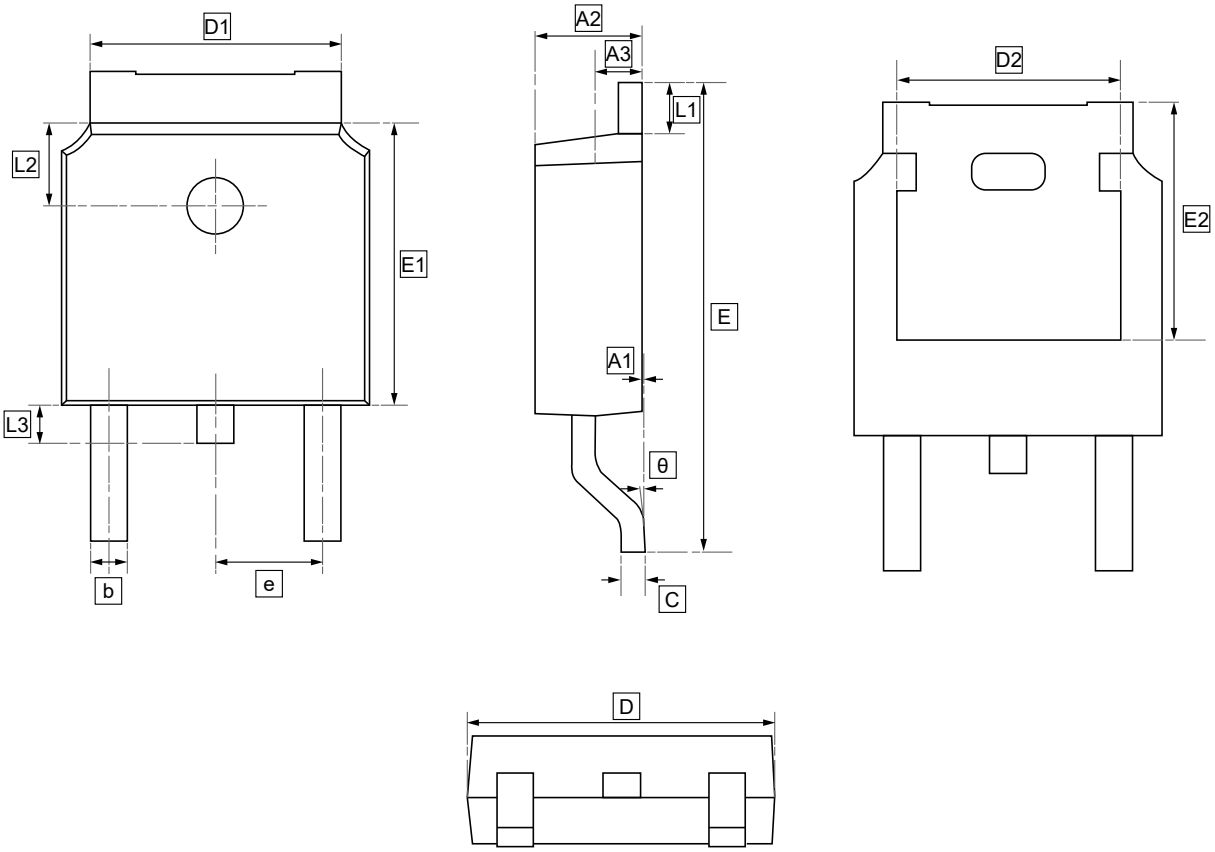


Fig 13: Thermal Response

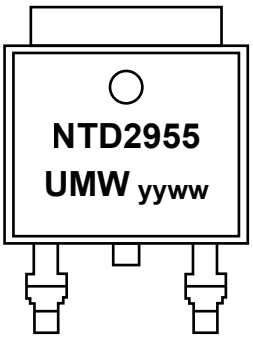
7.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NTD2955T4G	TO-252	2500	Tape and reel

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