UMW FDD6637

-30V P-Channel MOSFET

1.Features

- V_{DSS}=-30V
- $R_{DS(ON)}$<11.6mΩ(V_{GS}=-10V)
- $R_{DS(ON)}$<18mΩ(V_{GS}=-4.5V)
- RoHS Compliant
- High performance trench technology
- for extremely low $R_{DS(ON)}$

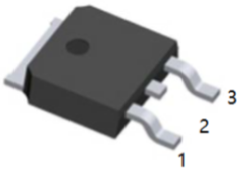
2.Applications

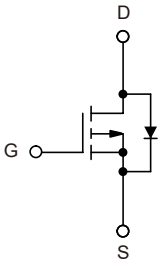
- Inverter
- Power Supplies

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_A= 25°C

Parameter			Symbol	Rating	Units
Drain-Source Voltage			V_{DSS}	-30	V
Drain-Source Avalanche Voltage (maximum)		(Note 4)	$V_{DS(Avalanche)}$	-40	V
Gate-Source Voltage			V_{GSS}	±25	V
Continuous Drain Current	@T_C=25°C	(Note 3)	I_D	-55	A
	@T_A=25°C	(Note 1a)		-13	A
	Pulsed	(Note 1a)		-100	A
Power Dissipation	@T_C=25°C	(Note 3)	P_D	57	W
	@T_A=25°C	(Note 1a)		3.1	W
	@T_A=25°C	(Note 1b)		1.3	W
Operating and Storage Junction Temperature Range			T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	2.2	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1b)	$R_{\theta JA}$	96	°C/W

6.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Energy (Single Pulse)	E_{AS}	V_{DD}=-35V, I_D=-11A, L=1mH		61		mJ
Drain-Source Avalanche Current	I_{AS}			-14		A
Drain–Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-28V, V_{GS}=0V			-1	μA
Gate–Body Leakage	I_{GSS}	V_{GS}=±25V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1	1.6	-3	V
Static Drain–Source On–Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-14A		9.7	11.6	mΩ
		V_{GS}=-4.5V, I_D=-11A		14.4	18	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-14A		35		S
Input Capacitance	C_{iss}	V_{DS}=-20V, V_{GS}=0V f=1MHz		2370		pF
Output Capacitance	C_{oss}			470		pF
Reverse Transfer Capacitance	C_{rss}			250		pF
Gate Resistance	R_g	f=1MHz		3.6		Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=-20V, I_D=-1A V_{GS}=-10V, R_{GEN}=6Ω		18	32	ns
Turn–On Rise Time	t_r			10	20	ns
Turn-Off DelayTime	$t_{D(off)}$			62	100	ns
Turn–Off Fall Time	t_f			36	58	ns
Total Gate Charge, VGS = –10V	Q_g	V_{DS}=-20V, I_D=-14A		45	63	nC
Total Gate Charge, VGS = –5V	Q_g			25	35	nC
Gate–Source Charge	Q_{gs}			7		nC
Gate–Drain Charge	Q_{gd}			10		nC
Drain–Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-14A (Note 2)		-0.8	-1.2	V
Diode Reverse Recovery Time	t_{rr}	I_F=-14A, di/dt=100A/μs		28		ns
Diode Reverse Recovery Charge	Q_{rr}			15		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$=40°C/W when mounted on a 1in ^{2} pad of 2oz copper.

b) $R_{\theta JA}$= 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at T_C=25°C and $R_{DS(ON)}$ is at $T_{J(max)}$ and V_{GS}=10V. Package current limitation is 21A

4. $BV_{(avalanche)}$ Single-Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.

7.1Typical characteristic

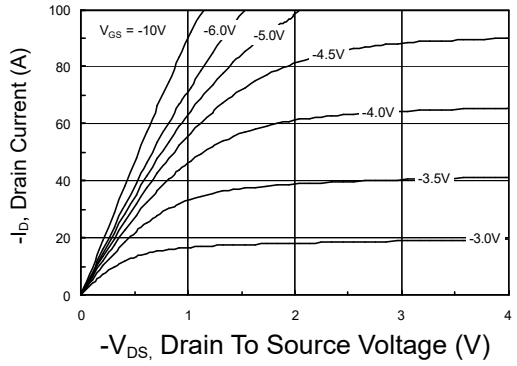


Figure 1: On-Region Characteristics

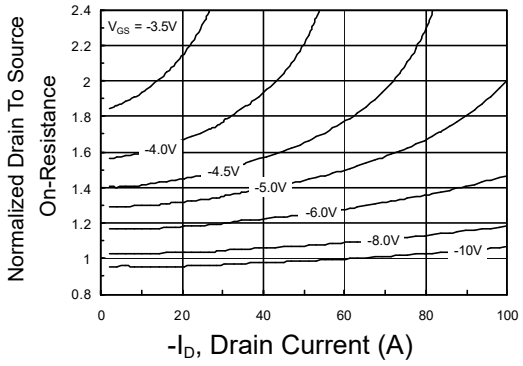


Figure 2: Normalized On-Resistance vs Drain Current and Gate Voltage

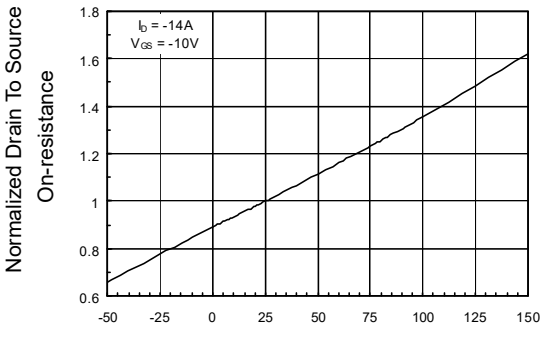


Figure 3: Normalized On Resistance vs Junction Temperature

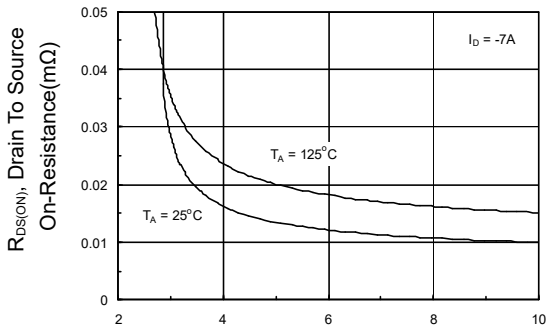


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

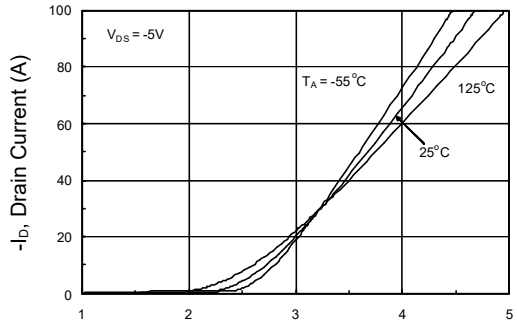


Figure 5: Transfer Characteristics

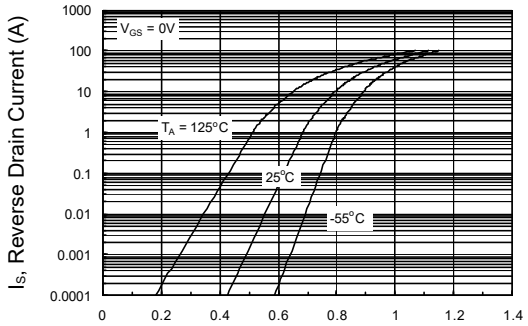
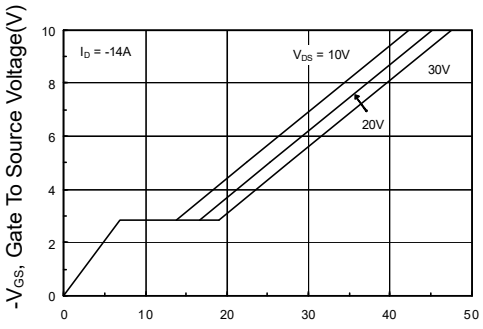


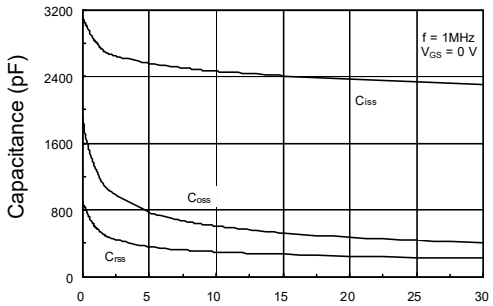
Figure 6: Source to Drain Diode Forward Voltage vs Source Current

7.2Typical characteristic



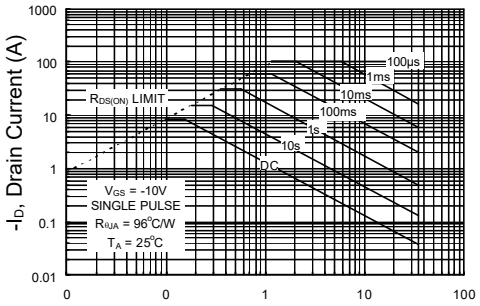
Q_g, Gate Charge (nC)

Figure 7: Gate Charge Characteristics



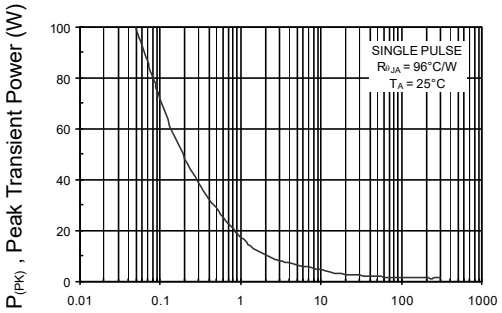
$V_{DS,}$ Drain To Source Voltage (V)

Figure 8: Capacitance vs Drain to Source Voltage



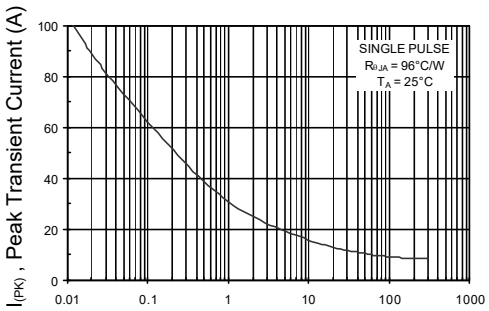
$-V_{DS}$, Drain To Source Voltage (V)

Figure 9: Maximum Safe Operating Area



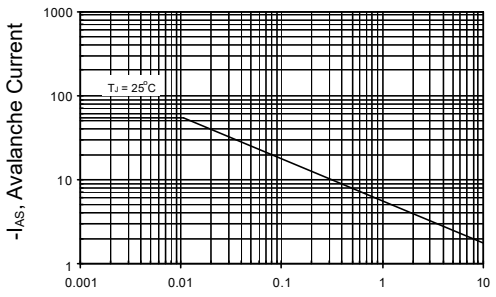
t_1, TIME (sec)

Figure 10: Single Pulse Maximum Power Dissipation



t_1, TIME (sec)

Figure 11: Single Pulse Maximum Peak Current



t_{AV}, Time In Avanche(ms)

Figure 12: Unclamped Inductive Switching Capability

7.3Typical characteristic

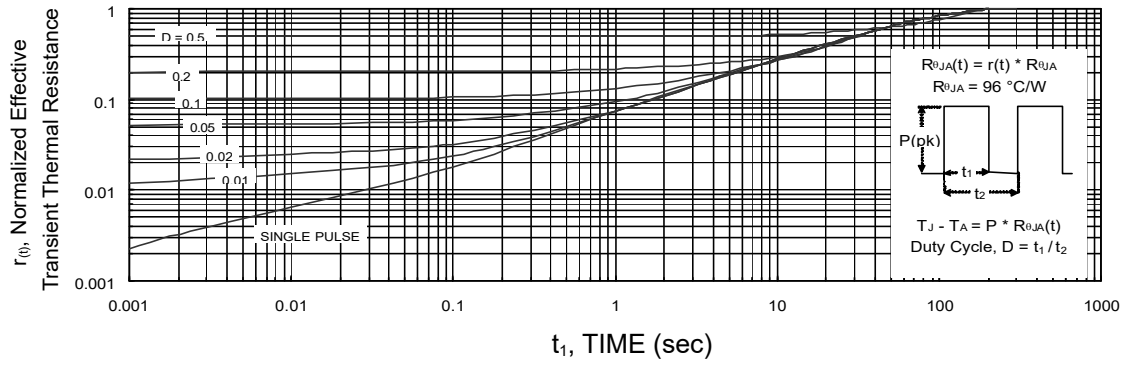


Figure 13: Transient Thermal Response Curve

8.Test Circuits and Waveforms

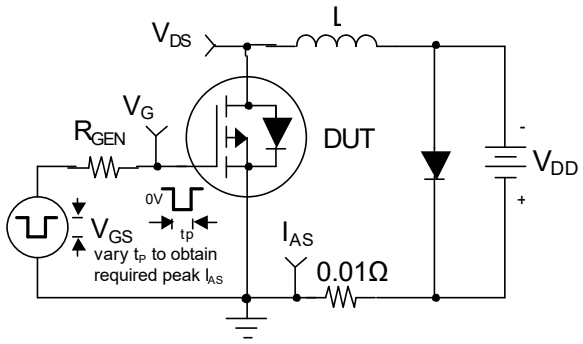


Figure 14. Unclamped Inductive Load Test Circuit

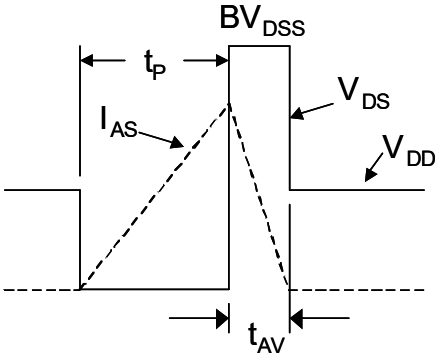


Figure 15. Unclamped Inductive Waveforms

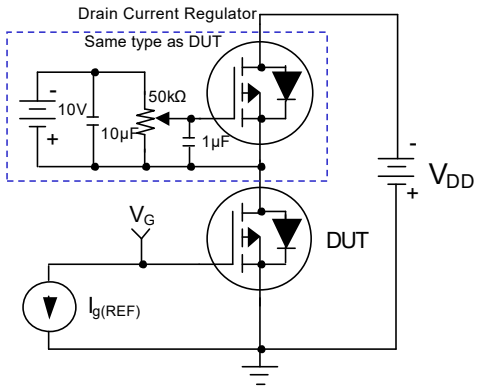


Figure 16. Gate Charge Test Circuit

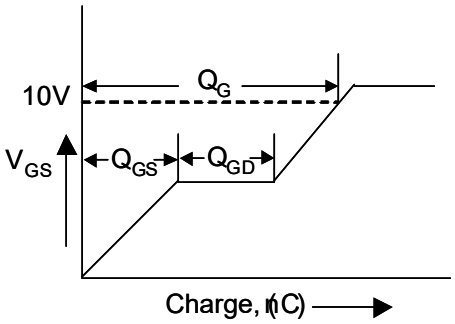


Figure 17. Gate Charge Waveform

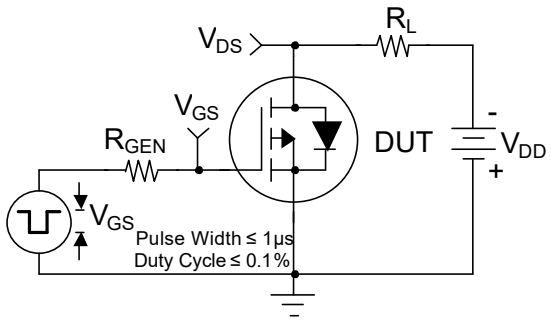


Figure 18. Switching Time Test Circuit

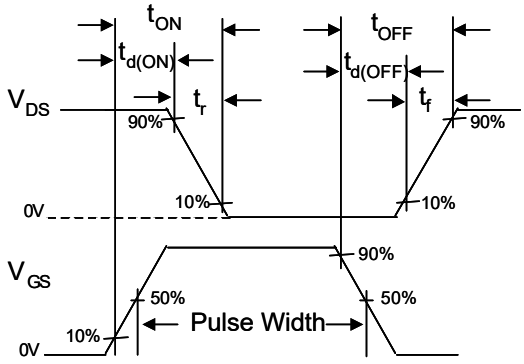
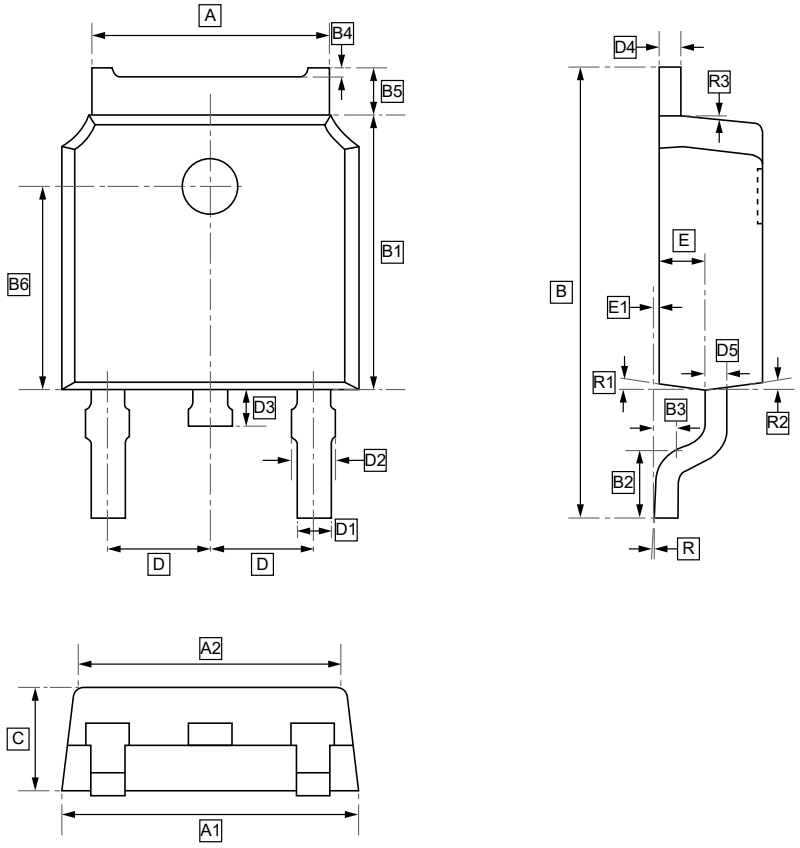


Figure 19. Switching Time Waveforms

9.TO-252 Package Outline Dimensions

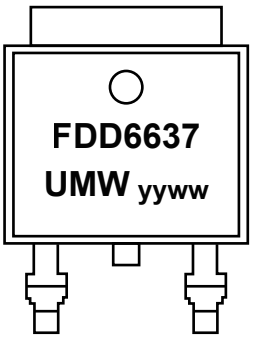


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	B	B1	B2	B3	B4	B5	B6	C	D
Min	5.1	6.4	5.6	9.5	5.9	1.35	0.4	0.1	0.85	4.35	2.15	2.286
Max	5.5	6.8	6.0	10.3	6.3	1.65	0.6	(typ.)	1.05	4.65	2.45	(typ.)

Symbol	D1	D2	D3	D4	D5	E	E1	R	R1	R2	R3
Min	0.66	0.81	0.65	0.42	0.42	0.86	0.05	0°	7°	7°	7°
Max	0.86	1.01	0.95	0.58	0.58	1.16	0.05	6°	(typ.)	(typ.)	(typ.)

10.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD6637	TO-252	2500	Tape and reel

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