CMOS IC – 3.5 – DIGIT A/D CONVERTER

1. DESCRIPTION

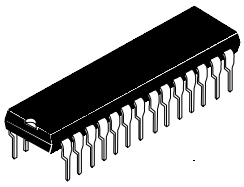
The HT7316A is high performance, low power 3 1/2 - digit A/D converter. All the necessary active devices are contained in a single CMOS IC, including seven-segment decoder, display driver, voltage reference and clock. HT7316A is designed to interface with a liquid crystal display (LCD). High accuracy 10μV for 200.0mV full-scale measurement, input bias current of 10pA max, and rollover of less than one count.

The HOLD pin makes hold or “freeze” a reading.

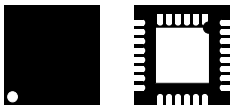
2. FUNCTIONS

- True polarity indication for precision null detection
- Low noise – Less than 15μ Vp-p
- Low power operation – 0.3 mW
- High Impedance CMOS differential inputs 10^{12} Ω
- True differential input and reference
- Low operating voltage: 2.5V ~ 5.2V
- Direct display drive for LCD
- No additional active components required
- Low linearity error: guaranteed less than 1 count
- Internal reference with low temperature drift
- Applications: digital panel meters, digital multimeters, thermometers, capacitance meters, PH meters, photometers etc.

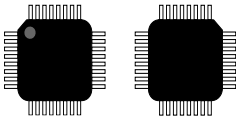
ORDERING INFORMATION



DIP40（52*14）
N SUFFIX
HT7316ANZ



QFN44（8*8）
RN SUFFIX
HT7316ARNZ

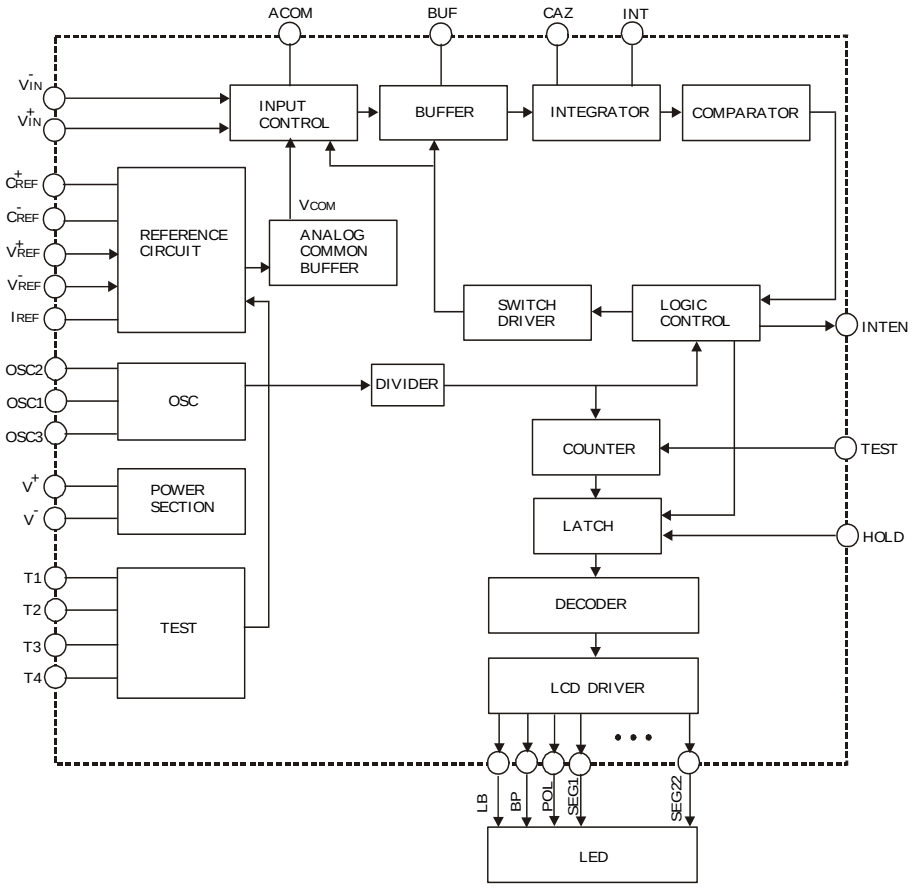


LQFP44（10*10）
RQ SUFFIX
HT7316ARQZ

&HT7316	= Specific Device Code
&A	= Version
&N, RN,RQ	= Packaging
&Z	= Pb−Free Package
&#	=Date Code

T_A = -40° to 125°C for all packages

3. BLOCK DIAGRAM



4. ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage (V^+ to V^-)		6	V
Analog Input Voltage (either input)		V+ to V^-	V
Reference Input Voltage (either input)		V+ to V^-	V
Digital Inputs		V^- to V+	V
Operating Temperature	T_{opr}	-40 ~ +125	°C
Storage and Junction Temperature	T_{stg}	-55 ~ +150	°C

5. DC ELECTRICAL CHARACTERISTICS

V_{supply} (V^+ to V^-) = 3.0V, T_A = 25°C, f_{clock} = 48KHz, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V^+, V^-		2.5	3.0	5.2	V
Supply Current	I_{DD}	V_{IN} = 0		200		μA
Leakage Current Input	I_{LEAK}	V_{IN} = 0		1	10	pA
Segment and Back Plane Drive Voltage	V_{LCD}			3.0		V
Analog Common Voltage (With Respect to Negative Supply)	V_{ANACOM}			1.5		V
Noise (Pk-Pk Value Not exceeded 95% of Time)	V_N	V_{IN} = 0 Full Scale 200.0mV	-	15	-	μV
Zero Input Reading		V_{IN} = 0 Full Scale 200.0mV	-000.0	± 000.0	± 3	Digital Reading
Ratiometric Reading		V_{IN} = V_{REF} =100.0mV	999	999/1000	1000	Digital Reading
Linearity (Max. Deviation From Best Strait Line Fit)		Full Scale 200.0mV	-1	± 0.2	+1	Counts
Scale Factor Temp Coeff. (Advanced)		V_{IN} = 199.0mV 0 °C < T_A < 70 °C		± 5		ppm/°C
Rollover Error		V^-_{IN}= V^+_{IN} =200.0mV	-1	± 0.2	+1	Counts
Reference Current	I_{REF}		18.6	19	19.4	μA
Reference Current Supply Voltage Ratio	$\Delta I_{REF}/\Delta V$	V = (V+ - V^-)		0.1		μA/V
Low Battery Detection Voltage	V_{LV}			2.5		V

6. FUNCTIONAL DESCRIPTION

An input signal to be measured is applied to the integrating capacitance for a fixed time as determined by a clock counter. The accumulated charge will be proportional to the input signal, for a fixed clock rate and constant current. The resulting integral is returned to zero by integrating a reference signal of polarity opposite that of the input signal. The length of time required for the integrator to return to zero, as measured with the clock counter to display at output, is proportional to the average magnitude of the input signal over the integration period

6.1. Analog Selection

Fig.1 shows the block diagram of the Analog Section for HT7316A. Each measurement cycle is divided into three parts.

They are:

(1) Signal integrated [INT]

(2) Deintegrated [DE]

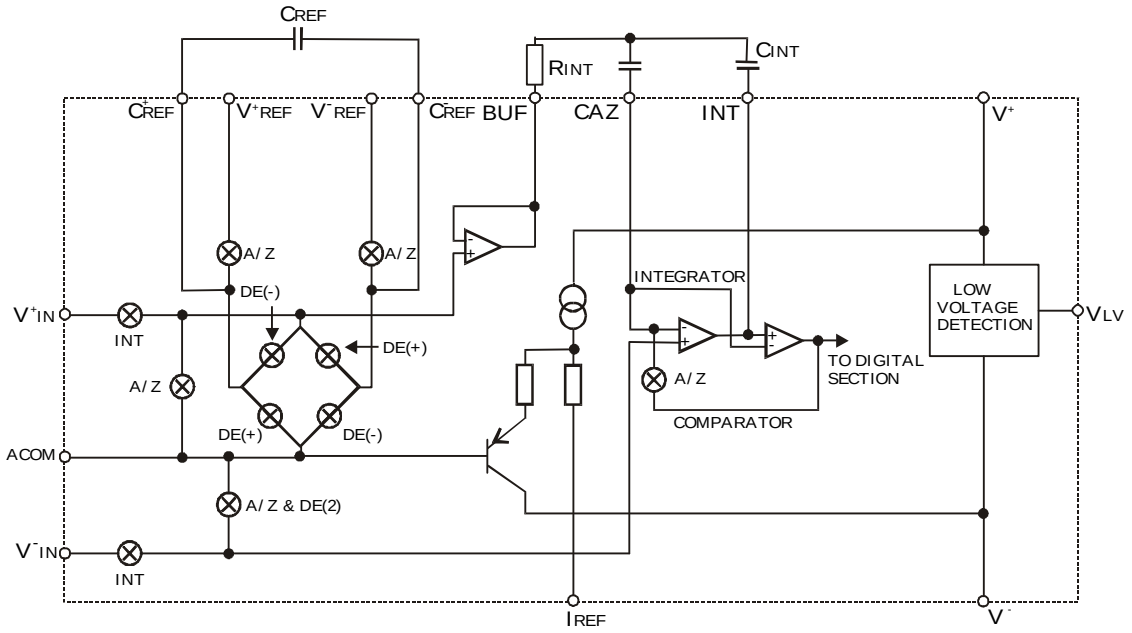


Fig.1 HT7316A Analog Section

a. Type Phase

During type phase, three things happen:

(1) Input high and low are disconnected from PIN and shorted to analog COMMON.

(2) The reference capacitor is charged to the reference voltage.

A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator and comparator.

b. Signal Integrate Phase

During signal integrate, the type phase loop is opened, the internal short is removed, and the internal inputs high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time (1000 counts). At the end of this phase, the polarity of the integrated signal is determined.

c. De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to Analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to type phase. The time required to return to type phase is proportional to the input signal. Specifically, the digital reading displayed is 1000

b. Digital Selection

Fig.2 show the digital section for the HT7316A. The internal digital ground is equal with V^- voltage. The BP frequency

is the clock frequency divided by 800. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible DC voltage exists across the segments.

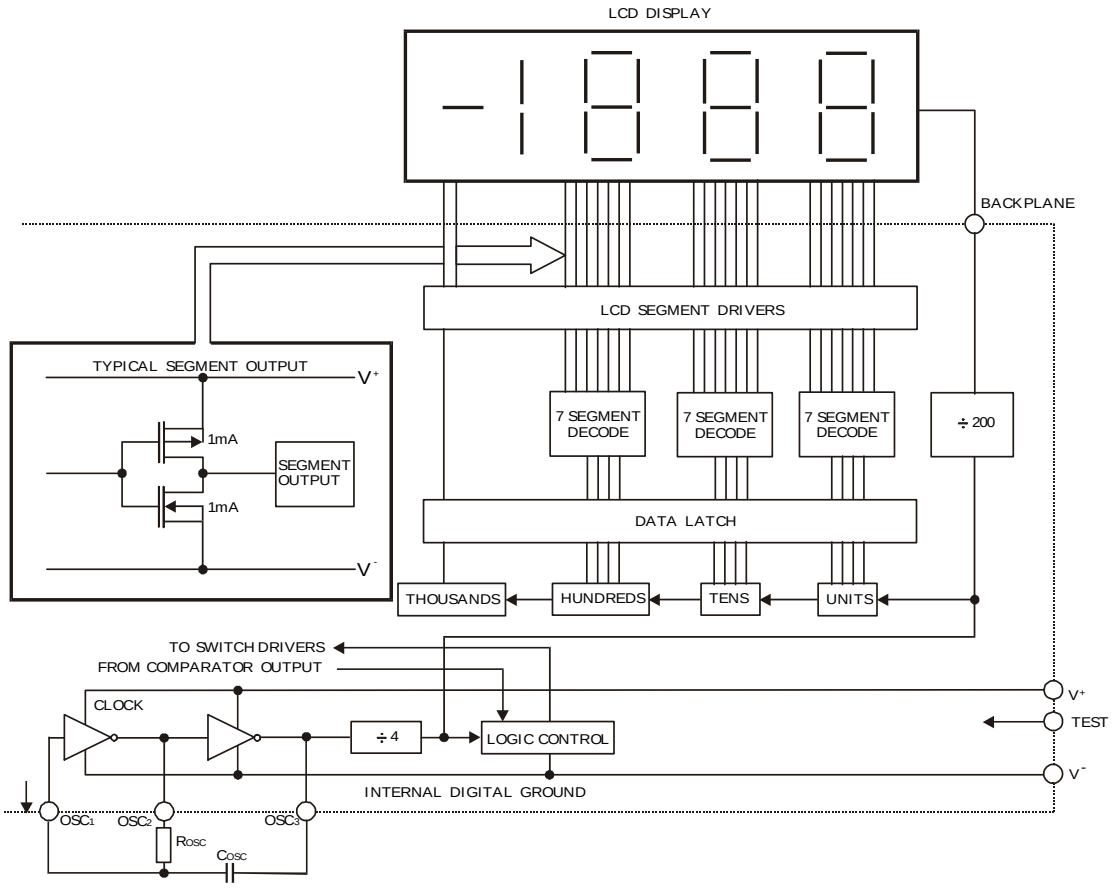
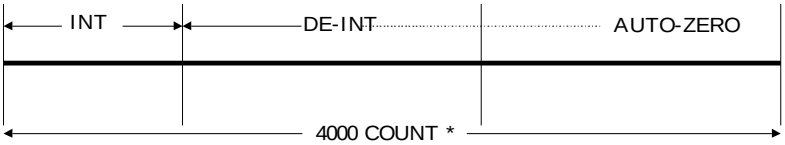


Fig.2 HT7316A Digital Section

6.2 System Timing

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phase. These are: signal integrated (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes complete measure cycles of 4000 (16000 clock pulses) independent of input voltage.



* as a matter of fact, the total measurement cycle is 4001 counts for measured values less than 2000 counts The measurement cycle becomes 4000 counts for overflow measurement

6.3 Clock Circuit:

HT7316A may use the following clocking methods:

1. An external oscillator connected to OSC_1.
2. An RC oscillator using OSC_1, OSC_2 and OSC_3.

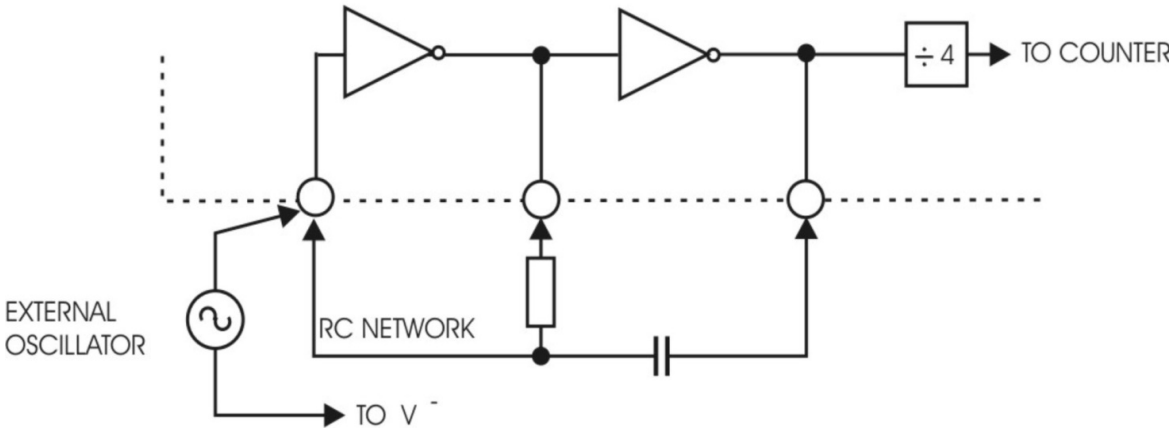


Fig.3 Clock Circuit

6.4 Integrating Resistor (R_{INT}) :

The buffer amplifier and integrator are designed with class A output stages with 10μA of quiescent current each. They can supply 10μA drive current with negligible linearity errors. R_{INT} should be large enough to remain in linear region but small enough to reduce the leakage current on the PC board. For 200mv full scale, R_{INT} is 200KΩ.

6.5 Oscillator Components (R_{OSC}, C_{OSC}) :

While using RC oscillator, the R_{OSC} (between OSC_1 and OSC_2) should be 100KΩ and C_{OSC} is selected from the following equation:

$$F_{osc} = \frac{0.45}{R_{osc} \bullet C_{osc}}$$

(R_{OSC} in MΩ, C_{OSC} in μF)

6.6 Integrating Capacitor (C_{INT}) :

C_{INT} should be chosen to give the maximum voltage swing without causing the saturation of integrator output swing. An additional requirement of C_{INT} is that C_{INT} must have low dielectric absorption to minimize rollover error. Polypropylene capacitors give undetectable errors at reasonable cost

6.7 Reference Voltage Selection:

The analog input required to generate full scale output (2000 counts) is $V_{IN} = V_{REF}$, thus:

V_{REF} = 100mV for full scale voltage 200mV.

V^-_{IN} and the transducer output is connected between V^+_{IN} and analog common.

6.8 Reference Voltage Capacitor (C_{REF}):

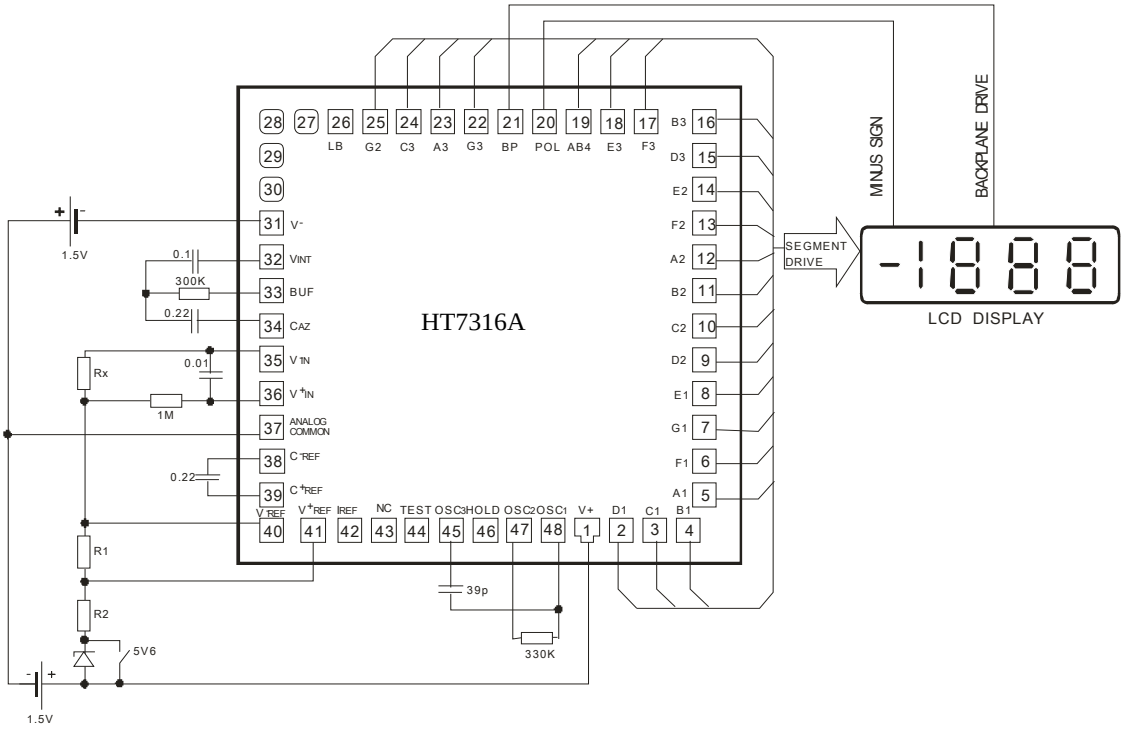
The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1μF capacitor gives good performance when V^-_{IN} is tied to analog common. If a large analog common voltage exists (V^-_{REF} unequal analog common) and a 200.0mV scale is used, a larger value is required to prevent rollover error. Generally 0.1μF will hold the rollover error to 0.5 count. In this case a mylar type dielectric capacitor is adequate

6.9 Reference Current (I_{REF}):

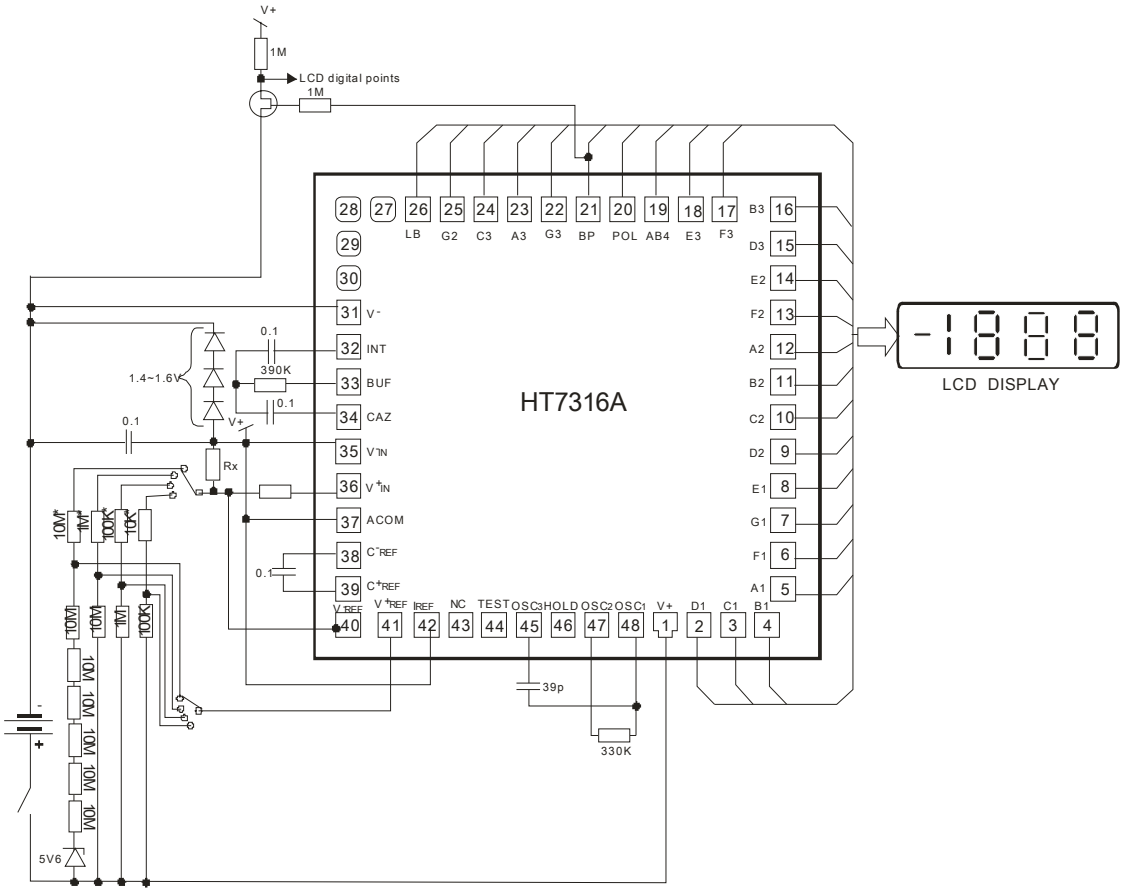
The 19μA reference current source is trimmed to 2.0% tolerance at T_A=25°C. It is intended to be used in conjunction with the external resistors to generate reference voltage

7. APPLICATION CIRCUITS

a. Resistance Meter (Two 1.5V batteries)



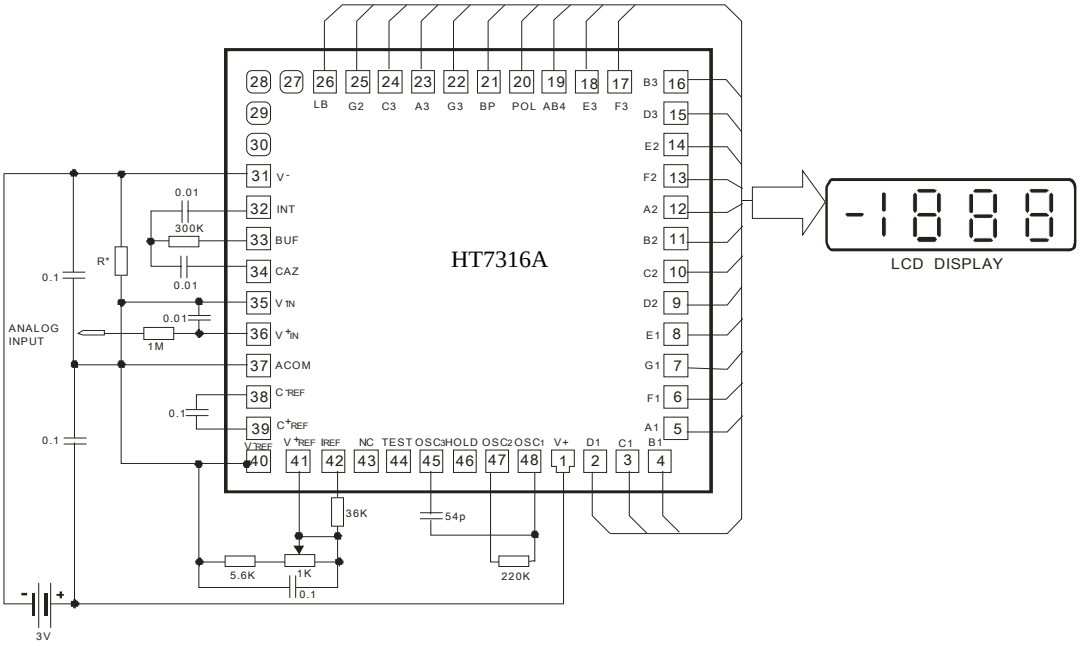
b. Resistance Meter (3V)



NOTE:

1. The chip substrate is electrically connected to V_{SS}.
2. R* - accuracy these resistors must be 1%.
3. $f_{OSC} \approx 32kHz$; $f_{LCD} = f_{OSC}/800$.

c. Voltmeter (3V battery)



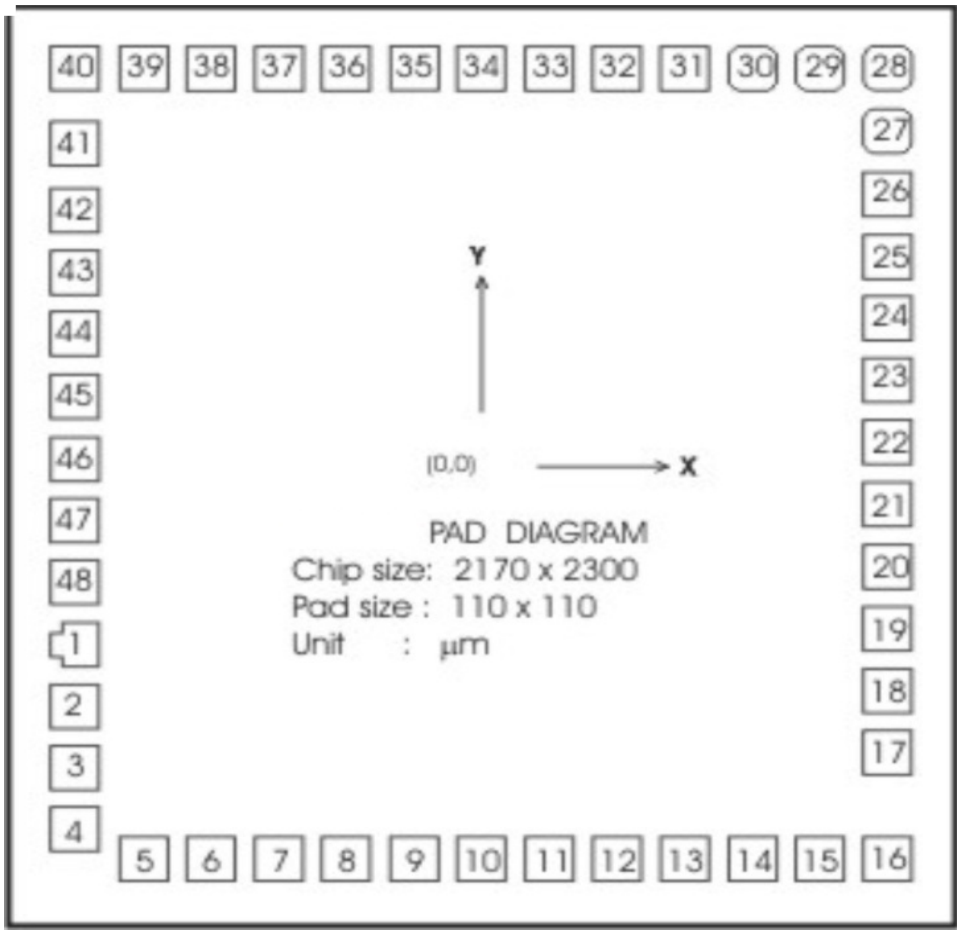
Notes: 1. The chip substrate is connected to Vss.

2. By R* = 75kΩ, the ACOM voltage is adjusted to min (V^+ - V^-)/2.

Resistor R* , which connects from V- to V-in, should be about 75kOhm, but correct value must be adjusted, - ACOM voltage is depended from this resistor and this resistor must be selected to adjust ACOM voltage (see Note 2).

(To simplify possible procedure we can recommend reserve two places for this resistor, as from sum of two resistors can be easy receive good result. Evidently maybe one resistor can be enough

8. PAD DIAGRAM

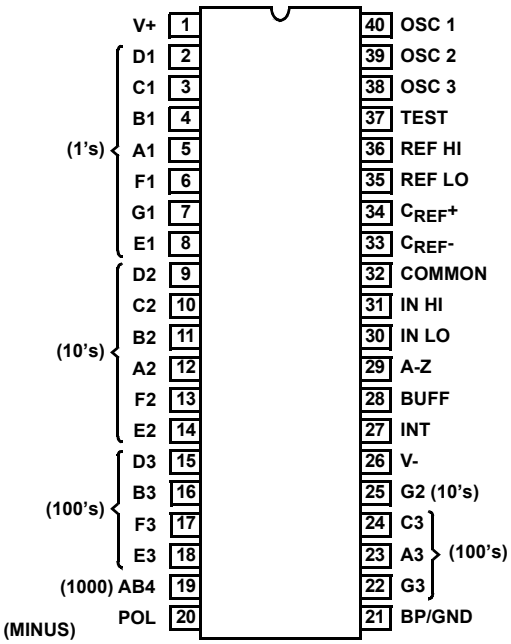


9. PAD DESCRIPTION

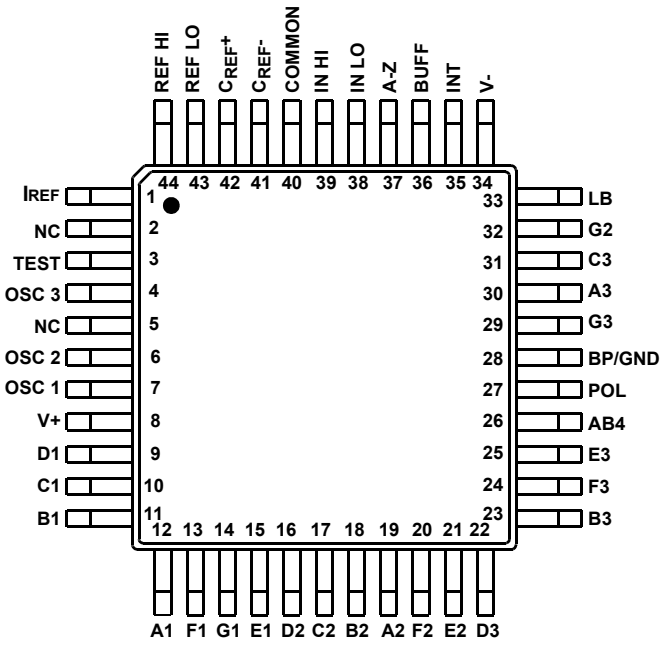
Pad No.	Pad Name	Description
1	V^+	Positive supply voltage.
2	D1	Activates the D section of the units display.
3	C1	Activates the C section of the units display.
4	B1	Activates the B section of the units display.
5	A1	Activates the A section of the units display.
6	F1	Activates the F section of the units display.
7	G1	Activates the G section of the units display.
8	E1	Activates the E section of the units display.
9	D2	Activates the D section of the tens display.
10	C2	Activates the C section of the tens display.
11	B2	Activates the B section of the tens display.
12	A2	Activates the A section of the tens display.
13	F2	Activates the F section of the tens display.
14	E2	Activates the E section of the tens display.
15	D3	Activates the D section of the hundreds display
16	B3	Activates the B section of the hundreds display
17	F3	Activates the F section of the hundreds display.
18	E3	Activates the E section of the hundreds display.
19	AB4	Activates both halves of the 1 in the thousands display.
20	POL	Activates the negative polarity display.
21	BP	LCD Backplane drive output.
22	G3	Activates the G section of the hundreds display.
23	A3	Activates the A section of the hundreds display.
24	C3	Activates the C section of the hundreds display.
25	G2	Activates the G section of the tens display.
26	LB	Low – Battery flag segment driver.
27	T1	Test pad.
28	T2	Test pad.
29	T3	Test pad.
30	T4	Test pad.
31	V^-	Negative power supply voltage.
32	INT	Integrator output. Connection point for integration capacitor.
33	BUF	Integration resistor connection.
34	CAZ	Auto-zero capacitor connection point.
35	V^-_{IN}	The analog LOW input is connected to this pin.
36	V^+_{IN}	The analog HIGH input is connected to this pin.
37	ACOM	Analog common point.
38	C^-_{REF}	Reference capacitor, negative terminal.
39	C^+_{REF}	Reference capacitor, positive terminal. A 0.1μF capacitor is used in most applications.
40	V^-_{REF}	Analog reference input, negative terminal.
41	V^+_{REF}	Analog reference input, positive terminal.
42	I_{REF}	Reference Current Output.
43	NC	
44	TEST	LCD test. When TEST pulled to V^+, LCD should read – 1888.
45	OSC_3	See OSC_1
46	HOLD	Hold input. Logic 1 hold display.
47	OSC_2	See OSC_2
48	OSC_1	Pins OSC_1, OSC_2 and OSC_3 make up the oscillator section.

10. PACKAGE PIN INFORMATION

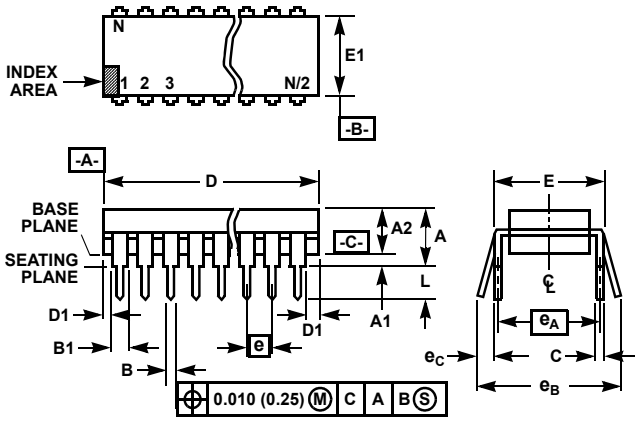
HT7316ANZ (PDIP)
TOP VIEW



HT7316ARQZ (QFP44)
HT7316ARNZ (QFN44)
TOP VIEW



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

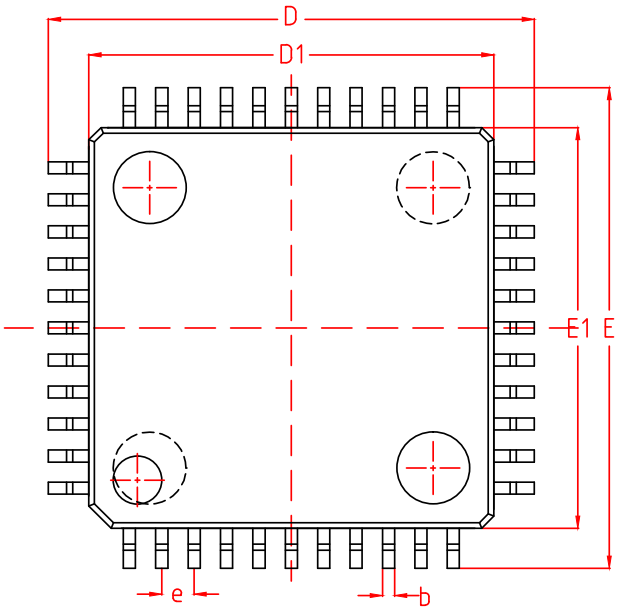
E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

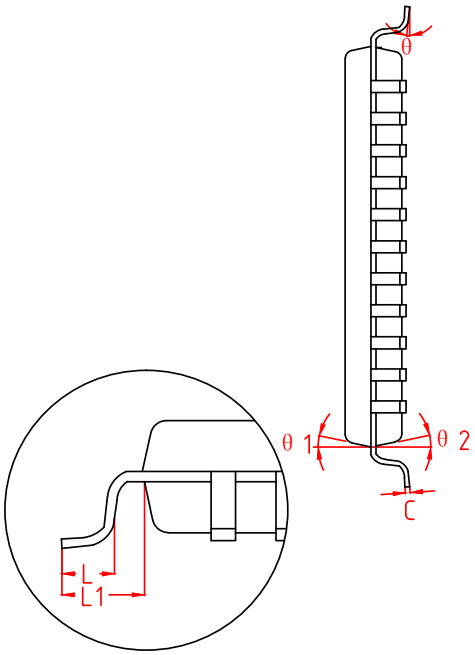
Rev. 0 12/93

LQFP44L(10X10X1.4-P0.8)

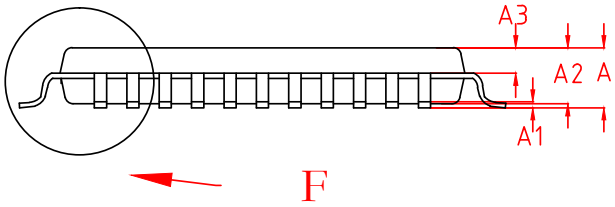
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图

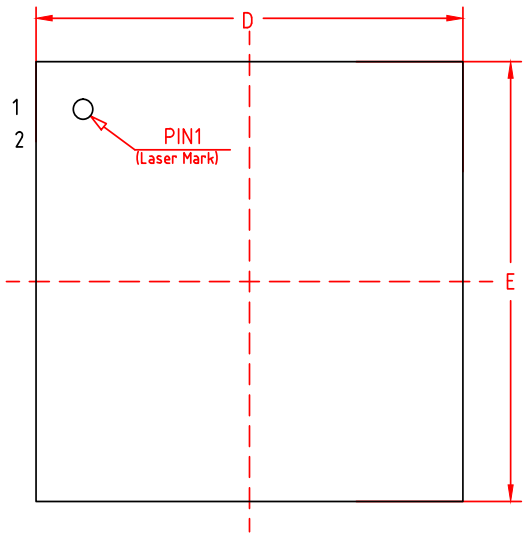


DETAIL:F

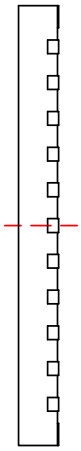
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.28	–	0.36
c	0.13	–	0.17
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80 BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

QFN44L(8×8×0.75-P0.65)

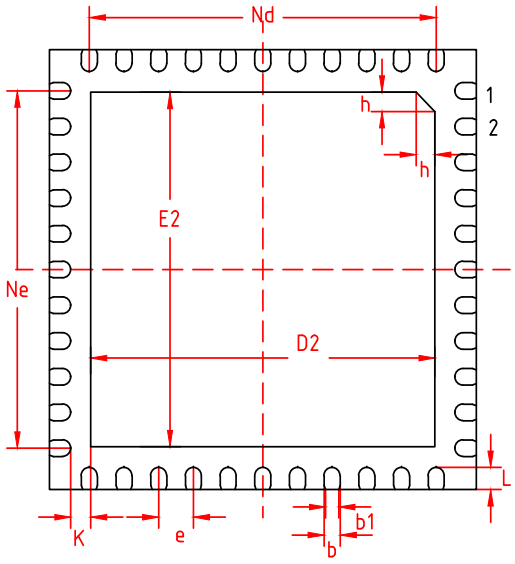
TOP VIEW
正视图



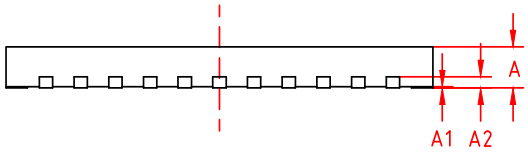
SIDE VIEW
侧视图



BOTTOM VIEW
背视图



SIDE VIEW
侧视图



机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.70	0.75	0.80
A1	–	0.02	0.05
A2	0.203 REF		
b	0.25	0.30	0.35
b1	0.20	0.25	0.30
D	7.90	8.00	8.10
D2	6.35	6.45	6.55
E	7.90	8.00	8.10
E2	6.35	6.45	6.55
e	0.65 BSC		
K	0.325	0.375	0.425
L	0.35	0.40	0.45
h	0.30	0.35	0.40
Ne	6.50 BSC		
Nd	6.50 BSC		

免责声明核心条款

本规格书所载信息由[深圳市海天芯微电子有限公司]（以下简称“海天芯”）提供，仅作为技术参考文档使用。本公司不对规格书中任何数据的准确性、完整性或适用性作出明示或暗示的保证，包括但不限于：

1.更新与终止：本公司保留随时修改、补充或终止本规格书的权利，恕不另行通知。

2.设计参数、性能指标及测试结果可能因实际应用环境、制造工艺或第三方组件差异而发生变化。

3.文档中引用的第三方技术或专利信息可能存在更新滞后，建议用户自行核实最新状态。

4.规格书不构成对产品功能、可靠性或安全性的承诺，实际表现需经用户独立验证。

5.因使用本规格书信息导致的直接、间接、特殊或衍生性损失（包括但不限于利润损失、生产中断或数据损坏）。

6.用户基于未经验证的设计参数实施工程决策所产生的后果。

7.第三方知识产权侵权索赔，除非该侵权由本公司故意行为直接导致。

8.在应用本规格书前，自行评估设计可行性并承担全部技术风险。

9.不将文档内容用于未经授权的商业目的或侵犯第三方权益。

10.发现信息矛盾或缺陷时，立即停止使用并通知本公司。