

1.Description

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

2.2Features

- High power and current handling capability.
- High performance trench technology for extremely low $R_{DS(ON)}$

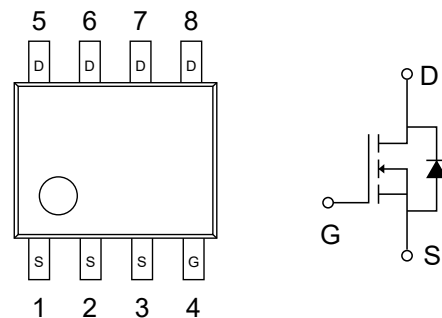
2.1Features

- $V_{DS(V)}=20V$
- $I_D=15A(V_{GS}=4.5V)$
- $R_{DS(ON)}<7.5m\Omega(V_{GS}=2.5V)$
- $R_{DS(ON)}<10m\Omega(V_{GS}=4.5V)$

3.Pinning information

Pin	Symbol	Description
4	G	GATE
1,2,3	S	SOURCE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	V_{GSS}	± 8	V
Drain Current – Continuous	I_D	15	A
– Pulsed (Note 1a)		50	
Power Dissipation for Single Operation (Note 1a)	P_D	2.5	W
		1.2	
		1	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}C$



5. Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	25	°C/W



6. Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

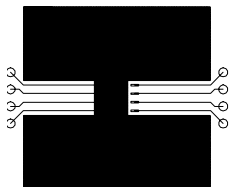
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	20			V
Breakdown Voltage Temperature Coefficient	$\frac{V_{\Delta BV_{DSS}}}{\Delta T_J}$	$I_D=250\mu A$ Referenced to 25°C		29		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=16V, V_{GS}=0V$			1	μA
Gate–Body Leakage, Forward	I_{GSSF}	$V_{DS}=0V, V_{GS}=8V$			100	nA
Gate–Body Leakage, Reverse	I_{GSSR}	$V_{DS}=0V, V_{GS}=-8V$			-100	nA
On Characteristics (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.2	1.4	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	$I_D=250\mu A$ Referenced to 25°C		-4		mV/°C
Static Drain–Source On–Resistance	$R_{DS(ON)}$	$V_{GS}=4.5V, I_D=15A$		6	7.5	mΩ
		$V_{GS}=2.5V, I_D=12A$		8	10	
On–State Drain Current	$I_{D(ON)}$	$V_{GS}=4.5V, V_{DS}=5V$	25			A
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=15A$		70		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, f=1MHz$		4700		pF
Output Capacitance	C_{oss}			850		pF
Reverse Transfer Capacitance	C_{rss}			310		pF
SWITCHING PARAMETERS (Note 2)						
Turn-On DelayTime	$t_{D(on)}$	$V_{DD}=10V, I_D=1A$ $V_{GS}=4.5V, R_{GEN}=6\Omega$		20	32	ns
Turn-On Rise Time	t_r			27	44	ns
Turn-Off DelayTime	$t_{D(off)}$			95	133	ns
Turn-Off Fall Time	t_f			35	56	ns
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=15A$ $V_{GS}=5V$		47	66	nC
Gate–Source Charge	Q_{gs}			7		nC
Gate–Drain Charge	Q_{gd}			10.5		nC



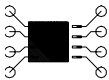
Drain-Source Diode Characteristics						
Maximum Continuous Drain-Source Diode Forward Current	I_S				2.1	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=2.1A(\text{Note } 2)$		0.65	1.2	V

Notes:

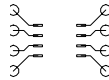
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 50° C/W when
mounted on a 0.5 in²
pad of 2 oz. copper.



b) 105° C/W when
mounted on a 0.02 in²
pad of 2 oz. copper.



c) 125° C/W when
mounted on a 0.003 in²
pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%



7.1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

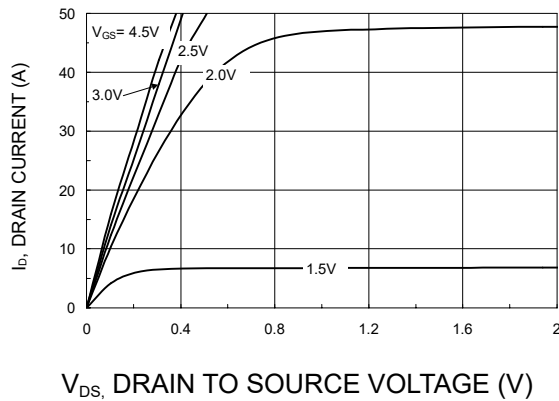


Fig 1: On-Region Characteristics.

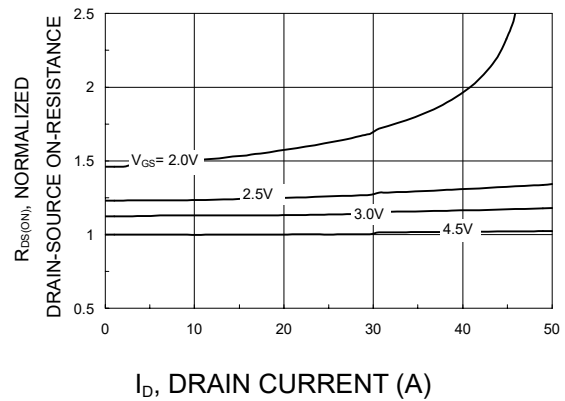


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage.

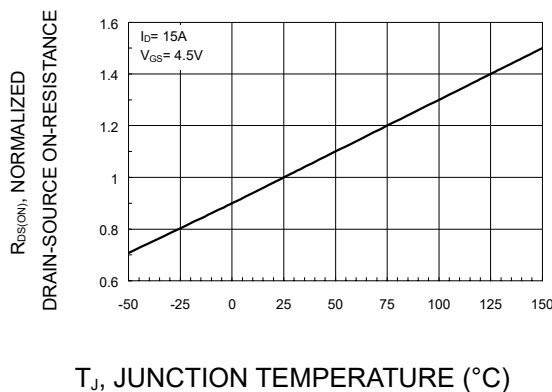


Figure 3: On-Resistance Variation with Temperature.

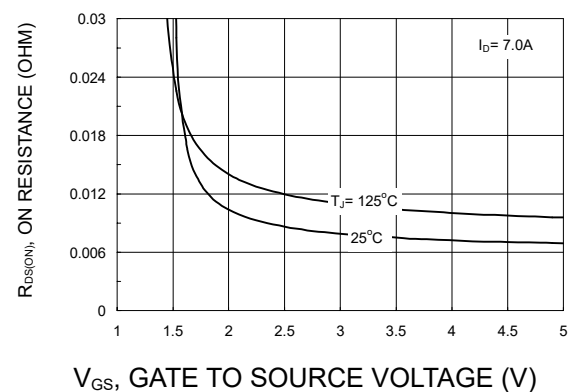


Figure 4: On-Resistance Variation with Gate-to-Source Voltage.

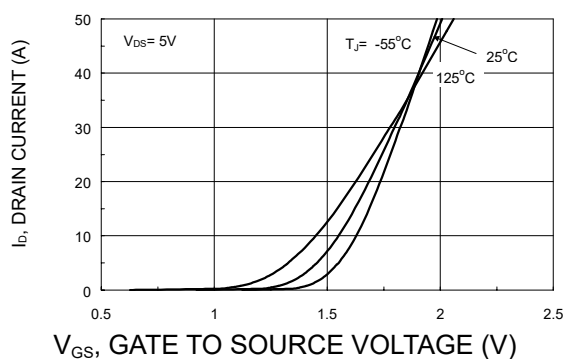


Figure 5: Transfer Characteristics.

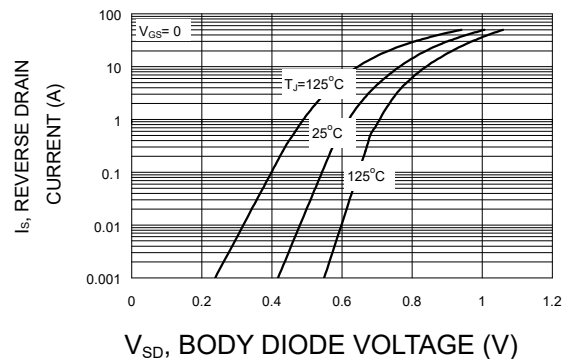


Figure 6: . Body Diode Forward Voltage Variation with Source Current and Temperature.



7.2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

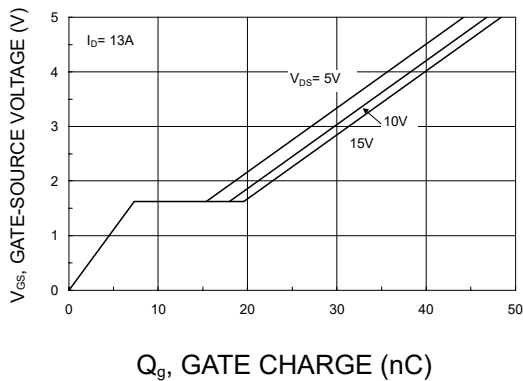


Figure 7: Gate-Charge Characteristics

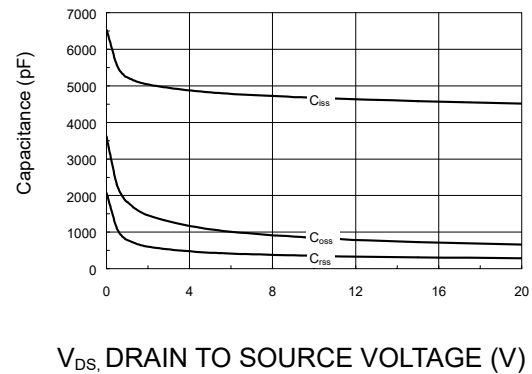


Figure 8: Capacitance Characteristics

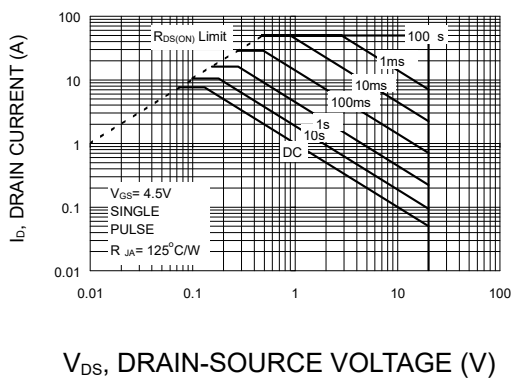


Figure 9: Maximum Safe Operating Area.

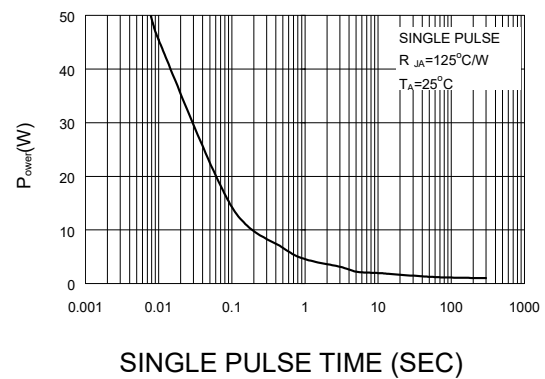


Figure 10: Single Pulse Maximum Power Dissipation.

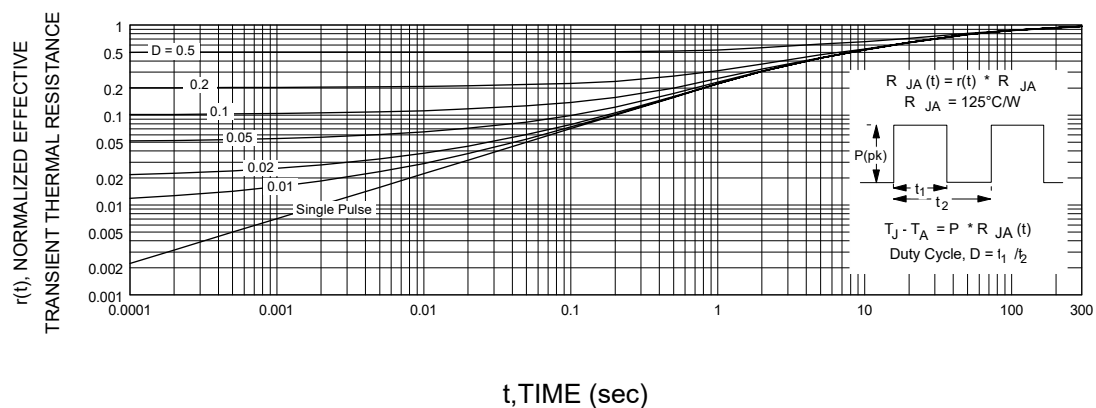
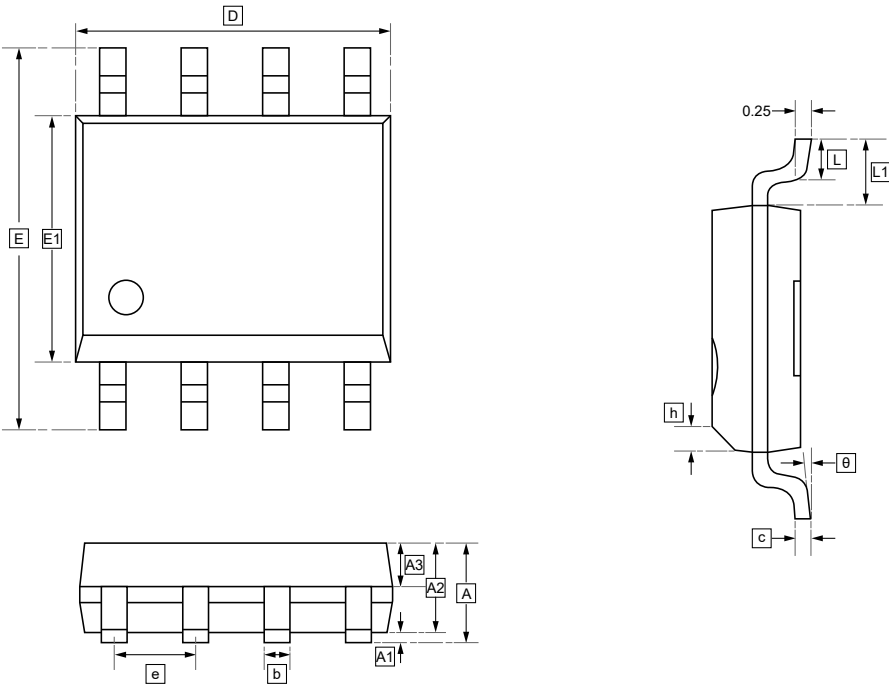


Figure 11: Transient Thermal Response Curve.



8.SOP-8 Package Outline Dimensions



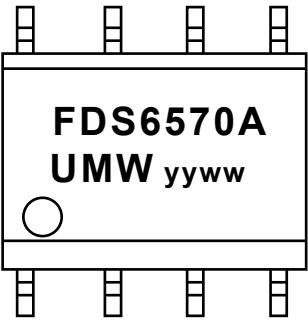
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.80	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.00	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°



9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS6570A	SOP-8	3000	Tape and reel



10.Disclaimer

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