Description

The LIS2DW12TR is an acceleration sensor IC, which features abundant functions, low power dissipation, small size, and precision measurement.

It communicates with MCU through I²C/SPI interface, the acceleration measurement data can be accessed in interrupt mode or inquiry mode. INT1 and INT2 provide many auto-detected interrupt signals which are suitable to many motion detection fields, interrupt source include data in position interrupt signal, FIFO data WTM and OVERRUN interrupt signal, 6D/4D direction detection interrupt signal, free fall detection interrupt signal, sleep and wake up detection interrupt signal, and single/double click detection interrupt signal. A high-precision calibration module is available within the IC to accurately compensate the senor's offset error and gain error. It has dynamically user selectable full scales of ±2G/±4G/±8G/±16G and it is capable of measuring accelerations with output data rates from 1Hz to 400Hz.

A self-test capability allows the user to check the functioning of the sensor in the final application. The available tilt calibration function is able to compensate the tilt caused by SMT or PCB installation, not occupying system resource, system update will not affect sensor parameters.

Features

- Supply voltage, 1.71V to 3.6V
- Independent IOs supply (1.8V)and supply voltage compatible
- Power Down mode consumption down to 1uA
- ±2G/±4G/±8G/±16G dynamically selectable full-scale
- 12-bit effective data (DLPF)
- I^2C/SPI digital output interface
- 6D/4D orientation detection
- Free-fall detection
- Single/double click detection and motion detection
- Programmable interrupt generator
- Embedded self test
- Embedded FIFO
- 10000g high shock survivability

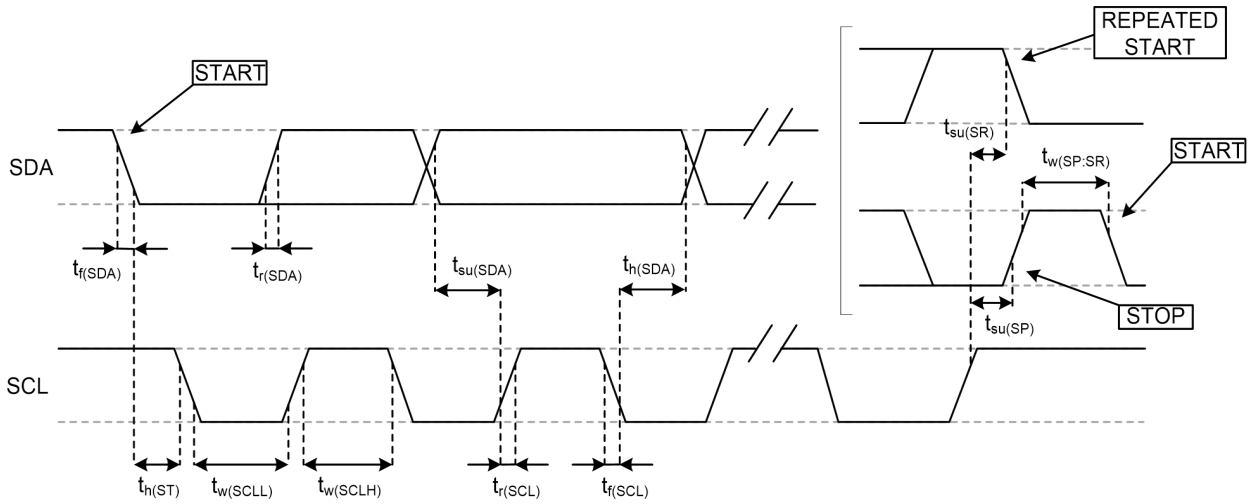
Applications

- Mobile phones/tablet
- Indoor navigation
- Image rotation
- Motion activated user interfaces
- Gaming
- Smart wearable device

Ordering Information

Part No.	Package	Hazardous Substance Control	Packing
LIS2DW12TR	LGA-12-2X2X1.0	Halogen free	Tape & Reel

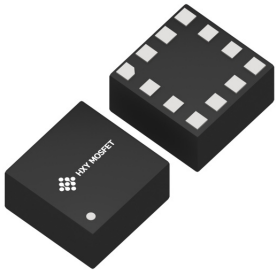
Block Diagram

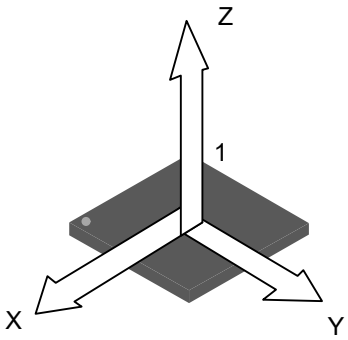


Absolute Maximum Rating

Characteristics	Symbol	Test conditions	Min.	Max.	Unit
Power supply voltage 1	V_{CC}	Circuit not damaged	-0.3	3.6	V
Power supply voltage 2	V_P	Circuit not damaged	-0.3	3.6	V
Arbitrary control pin	V_{in}	Circuit not damaged (CS/SDO/SCL/SDA/INT1/INT2)	-0.3	V_{DDIO}+0.3	V
Operating temperature	T_{OPR}	Circuit not damaged	-40	+85	°C
Storage temperature	T_{STG}	Circuit not damaged	-55	+150	°C

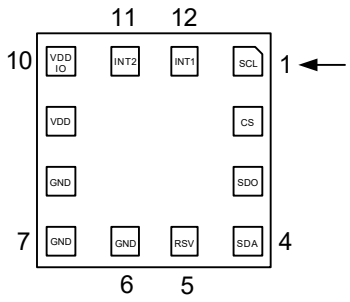
PIN Configuration





（俯视图）

可检加速度方向



（仰视图）

LGA12-2x2x1.0mm^3

PIN Description

Pin No.	Symbol	I/O	Description	Connection mode		
				I²C mode	SPI four-wire mode	SPI three-wire mode
1	SCL	I	I²C serial clock (SCL) SPI serial port clock (SPC)	SCL	SPC	SPC
2	CS	I	I²C/SPI mode selection (H:I²C mode, L: SPI mode)	NC	CS	CS
3	SDO	O	SPI serial data output, address selection in I²C mode	I2C Slave Device Address Select	SDO	NC
4	SDA	I/O	Used as SDA in I²C mode, Used as SDI in SPI 4-wire mode, Used as SDA in SPI 3-wire mode	SDA	SDI	SDA
5	RSV	--	--	--	--	--
6	GND	S	0V supply(Ground)	GND	GND	GND
7	GNDIO	S	0V supply(Ground)	GND	GND	GND
8	GND	S	0V supply(Ground)	GND	GND	GND
9	VDD	S	Analog power supply	VDD	VDD	VDD
10	VDDIO	S	Digital power supply for I/O pins	VDDIO	VDDIO	VDDIO
11	INT2	O	Interrupt pin 2, push–pull output	INT2	INT2	INT2
12	INT1	O	Interrupt pin 1, push–pull output	INT1	INT1	INT1

Note: I=input, O=output, I/O=input/output, S=power supply, OC=collector open-circuit output, RSV is floating or grounded.

Mechanical Characteristics (V_{DD}=2.5V, T_A=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Measurement range	F_{S0}	FS=0	--	±2.0	--	g
	F_{S1}	FS=1	--	±4.0	--	
	F_{S2}	FS=2	--	±8.0	--	
	F_{S3}	FS=3	--	±16.0	--	
Sensitivity	So0	FS=0 (HR mode)	--	1	--	mg/digit
	So1	FS=1 (HR mode)	--	2	--	
	So2	FS=2 (HR mode)	--	4	--	
	So3	FS=3 (HR mode)	--	8	--	
Sensitivity change vs temperature	T_{CSO}	FS=0	--	±0.01	--	%/°C
Typical zero-g level offset accuracy	Ty_{Off0}	FS=0	--	±80	--	mg
Zero-g level change vs temperature Note 1	TC_{Off}	Max delta from 25°C	--	±0.5	--	mg/°C
Self test output change	V_{st1}	FS=0, X axis	--	276	--	LSb
	V_{st2}	FS=0, Y axis	--	276	--	LSb
	V_{st3}	FS=0, Z axis	--	984	--	LSb
System bandwidth	BW	--	--	ODR/2	--	HZ
Operating temperature range	T_{OPR}	--	-40	--	+85	°C

Note: The product is calibrated at 2.5V by factory. The actual operating voltage ranges from 1.71V to 3.6V.

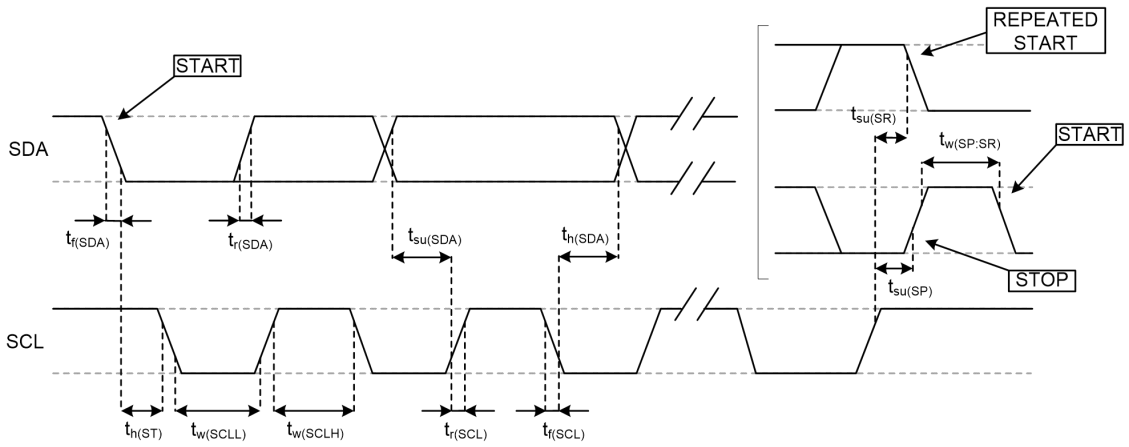
Electrical Characteristics (V_{DD}=2.5V, T_A=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	--	1.71	2.5	3.6	V
IO supply voltage	V_{DDIO}	--	1.71	--	V_{DD}+0.1	V
Supply current	I_{DD}	T_A=25°C, ODR=100HZ	--	20	--	μA
Current consumption in low-power mode	I_{DDLP}	T_A=25°C, ODR=100HZ	--	10	--	μA
Current consumption in power-down mode	I_{DDPdn}	T_A=25°C	--	0.5	--	μA
Digital high level input voltage	V_{IH}	--	0.8* V_{DDIO}	--	--	V
Digital low level input voltage	V_{IL}	--	--	--	0.2* V_{DDIO}	V
High level	V_{OH}	--	0.9* V_{DDIO}	--	--	V

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
output voltage						
Low level output voltage	V_{OL}	--	--	--	0.1* V_{DDIO}	V
Output data rate	ODR0	ODR= 1Hz	--	1	--	HZ
	ODR1	ODR= 10Hz	--	10	--	
	ODR2	ODR= 25Hz	--	25	--	
	ODR3	ODR= 50Hz	--	50	--	
	ODR4	ODR= 100Hz	--	100	--	
	ODR5	ODR= 200Hz	--	200	--	
	ODR6	ODR= 400Hz	--	400	--	
Turn-on time	T_{on}	ODR=100Hz	--	1	--	ms
Operating temperature range	T_{opr}	--	-40	--	+85	°C

I²C Control Interface Characteristics (V_{DD}=2.5V, T_A=25°C)

Characteristics	Symbol	I²C standard mode		I²C fast mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	$f_{(SCL)}$	0	100	0	400	KHz
SCL clock low time	$t_{w(SCLL)}$	4.7	--	1.3	--	μs
SCL clock high time	$t_{w(SCLH)}$	4.0	--	0.6	--	
SDA setup time	$t_{su(SDA)}$	250	--	100	--	ns
SDA data hold time	$t_{h(SDA)}$	0.01	3.45	0.01	1.2	μs
START condition hold time	$t_{h(ST)}$	4	--	0.6	--	μs
Repeated START condition setup time	$t_{su(SR)}$	4.7	--	0.6	--	
STOP condition setup time	$t_{su(SP)}$	4	--	0.6	--	
Bus free time between STOP and START conditions	$t_{w(SP:SR)}$	4.7	--	1.3	--	

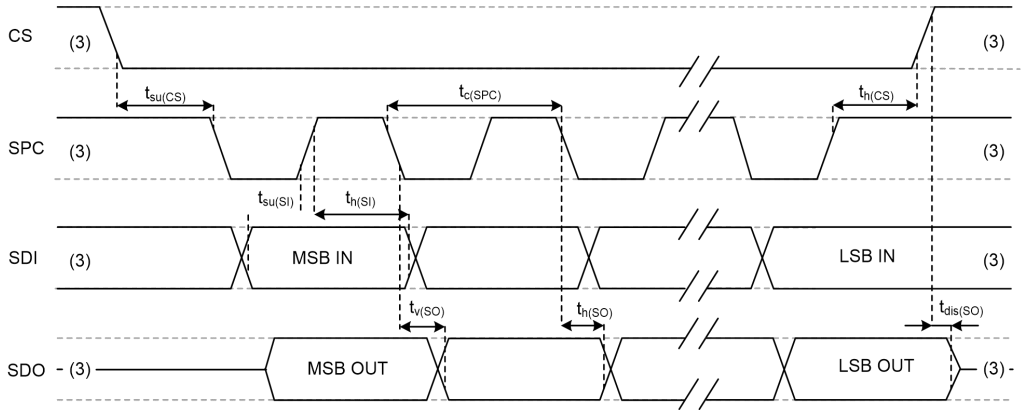


I²C slave timing diagram

SPI Serial Peripheral Interface Characteristics (V_{DD}=2.5V, T_A=25°C)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
SPI clock cycle[note]	$T_{c(SPC)}$	--	100	--	--	ns
SPI clock frequency	$F_{c(SPC)}$	--	--	--	10	MHz
CS setup time	$T_{su(CS)}$	--	5	--	--	ns
CS hold time	$T_{h(CS)}$	--	8	--	--	
SDI input setup time	$T_{su(SI)}$	--	5	--	--	
SDI input hold time	$T_{h(SI)}$	--	15	--	--	
SDO valid output time	$T_{v(SO)}$	--	--	--	50	
SDO output hold time	$T_{h(SO)}$	--	6	--	--	
SDO output disable time	$T_{dis(SO)}$	--	--	--	50	

Note: 10MHz clock frequency.



SPI slave timing diagram

Function Description

1 Detailed description

The LIS2DW12TR is an ultra compact low-power, digital output 3-axis linear accelerometer packaged in LGA. The complete device includes a mechanical sensing unit and an integrated circuit interface able to take the information from the sensing unit and to provide a signal to the external MCU through I²C or SPI interface.

2 Mechanical sensing unit

The mechanical sensing unit consists of suspended mass and silicon frame. The suspended mass are attached to the silicon frame in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation. When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.
At steady state the nominal value of the capacitors are few pF and when an acceleration is applied the maximum variation of the capacitive load is in fF range.

3 IC interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage that is finally available to the user by analog-to-digital converters. The acceleration data may be accessed through an I²C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller. The LIS2DW12TR features a data-ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device. It may also be configured to generate an inertial Wake-Up and Free-Fall interrupt signal
accordingly to a programmed acceleration event along the enabled axes.

4 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-g level (Ty_{Off}).
The trimming values are stored inside the device in EEPROM. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the normal operation. This allows to use the device without further calibration.

5 6D/4D detection

In this configuration the interrupt is generated when the device is stable in a known direction. 6-direction detections in a three-dimensional space are all enabled. Please refer to application note for detailed setting.

6 Free-fall detection

The interrupt is generated when the sensor is in free-fall state. In free-fall state, the sensor mass block is weightlessness, and theoretical three-axis output is zero, the sensor detector detects that the three-axis output is lower than threshold value, then the interrupt signal is generated, and corresponding state register is set.

7 Sleep and Wake up detection (static/motion detection

Sleep detection: when the sensor output keeps constant within given threshold range for a certain time, the sensor is judged as no action, corresponding state signal is set and interrupt signal is generated, the system enters low power mode. Refer to application note for details.
Wake up detection; when the sensor output becomes higher than the threshold value and lasts for a certain time, the sensor is judged as being action, corresponding state signal is set and interrupt signal is generated, the system restores normal operating mode. Refer to application note for details.

8 Single click and double click detection

The sensor judges whether the output reaches conditions for single/double click according to given threshold value and time, sets corresponding state signal and generates interrupt signal. Refer to application note for details.

9 Terminology

9.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The Sensitivity tolerance describes the range of sensitivities of a large population of sensors.

9.2 Zero-g level

Zero-g level Offset (Ty_{off}) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measure 0g in X axis and 0g in Y axis whereas the Z axis measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, "Zero-g offset" is called "temperature offset".

9.3 Self test

Self Test allows to check the sensor functionality without moving it. The Self Test function is off when the self-test bit is programmed to '0'. When the self-test bit is programmed to '1' an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When self test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside the range, then the sensor is working properly.

10 Digital interfaces

The registers embedded inside the LIS2DW12TR may be accessed through both the I2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode. The SPI 3-wire mode can be obtained through writing data into corresponding control bit in 4-wire write mode (only three wires needed for writing). These interfaces are multiplexed with communication pins. To use I2C interface, CS signal must be tied high (i.e . connected to V_{DDIO}).

Communication interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO)

10.1 I^2C serial interface

The LIS2DW12TR I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back. The relevant IIC terminology is given in the table below.

Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line and the serial Data line. The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to VDDIO through a pull-up resistor embedded inside the LIS2DW12TR. When the bus is free both the lines are high. The I2C interface is compliant with fast mode (400 KHz) I2C standards as well as with the normal mode.

10.1.1 I^2C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, ACK (low level at the 9^{th} CLK) is sent back to the master.

The Slave address (SAD) associated to the LIS2DW12TR is 0011xxxb. Data transfer with ACK signal is mandatory. The transmitter must release the SDA line in the 9th CLK. The receiver must then pull the data line LOW to complete one ACK return. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received. The I2C embedded inside the LIS2DW12TR behaves like a slave device and adheres to similar standard IIC protocol.

After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow multiple data read/ write.

The slave address is completed with a Read/Write bit. If the bit is '1' (Read), a repeated START (SR) condition is issued after the two sub-address bytes; if the bit is '0' (Write) the Master will transmit to the slave with direction unchanged.

I²C address

SDO external connection	7-bit I²C address	8-bit I²C address	Remark
Floating/logic high	0x19	0x32(W), 0x33(R)	Recommended
Logic low	0x18	0x30(W), 0x31(R)	Turn off internal pull-up resistor

Note: for SCL(PIN12)/SDA(PIN2)/SDO(PIN1), there are pull-up resistors by default on these three pins, and the resistance range of pull-up resistor is 50K ~ 60K. The voltage of pull-up resistor is VDDIO. If the external logic level of SDO is low, the internal pull-up resistor of SDO should be closed through I2C bus communication. If the LIS2DW12TR peripheral pull-up resistor can be ensured, the internal pull-up resistor of SCL and SDA can also be closed through I2C bus communication.

Transfer when master is writing one byte to slave

Master	ST	SAD+W	--	SUB	--	DATA	--	SP
Slave	--	--	SAK	--	SAK	--	SAK	--

Transfer when master is writing multiple bytes to slave

Master	ST	SAD+W	--	SUB	--	DATA	--	DATA	--	SP
Slave	--	--	SAK	--	SAK	--	SAK	--	SAK	--

Transfer when master is reading one byte of data from slave

Master	ST	SAD+W	--	SUB	--	SR	SAD+R	--	--	NMAK	SP
Slave	--	--	SAK	--	SAK	--	--	SAK	DATA	--	--

Transfer when master is reading multiple bytes data from slave

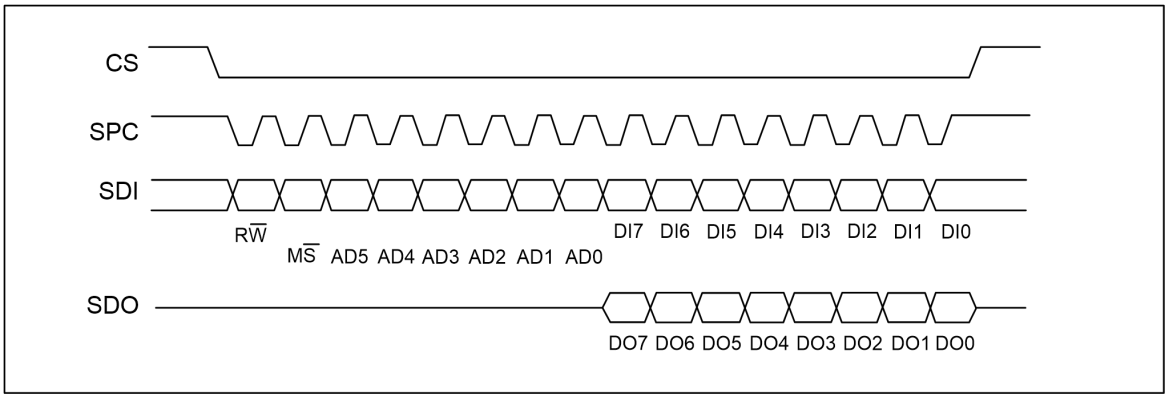
Master	ST	SAD+W	--	SUB	--	SR	SAD+R	--	--	MAK	--	MAK	--	NMAK	SP
Slave	--	--	SAK	--	SAK	--	--	SAK	DATA	--	DATA	--	DATA	--	--

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is

performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.
In order to read multiple bytes, it is necessary to assert the most significant bit of the subaddress field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.
For example, after the sensor is configured to work, continuous reading of triaxial data (register address 0x28 ~ 0x2d) is adopted, and the address of register data is 0xA8 (0x28 | 0x80).

10.2 SPI bus interface

The LIS2DW12TR SPI is a bus slave. The SPI allows to write and read the registers of the device.
The serial interface interacts with the outside world with 4 wires: CS, SPC, SDI, and SDO.



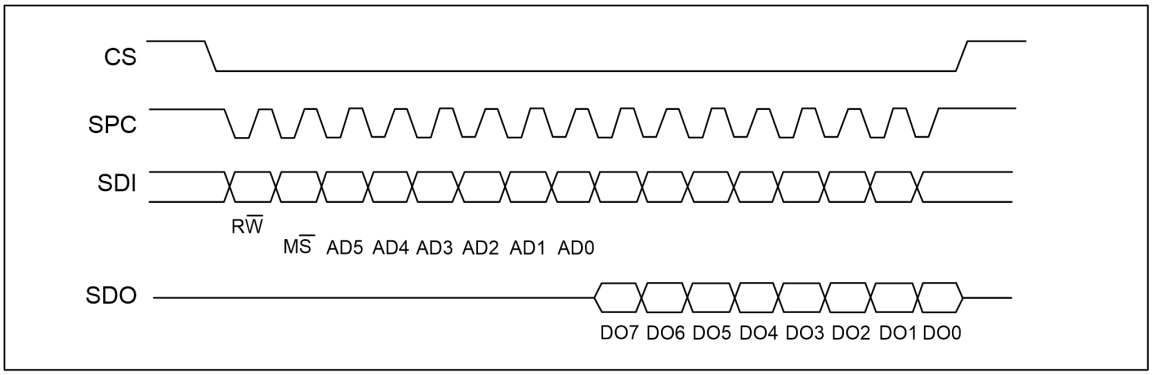
SPI read and write protocol

CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. SPC is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC. Both the read register and write register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple bytes read/write. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of CS.

- Bit0: $R\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) is read from the device. In latter case, the chip will drive SDO at the start of bit 8.
- Bit1: $M\overline{S}$ bit. When 0, the address remains unchanged. When 1, the address is auto incremented in multiple read/write commands.
- Bit2-7: address AD(5:0), the register address.
- Bit8-15: data DI(7:0) (write mode), the data that is written into the slave device (MSB first).
- Bit8-15: data DO(7:0) (read mode), the data that is read from the slave device (MSB first).

In multiple read/write commands further blocks of 8 clock periods are added. When $M\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When $M\overline{S}$ bit is 1 the address used to read/write data is incremented at every block. The function and behavior of SDI and SIO remain unchanged.

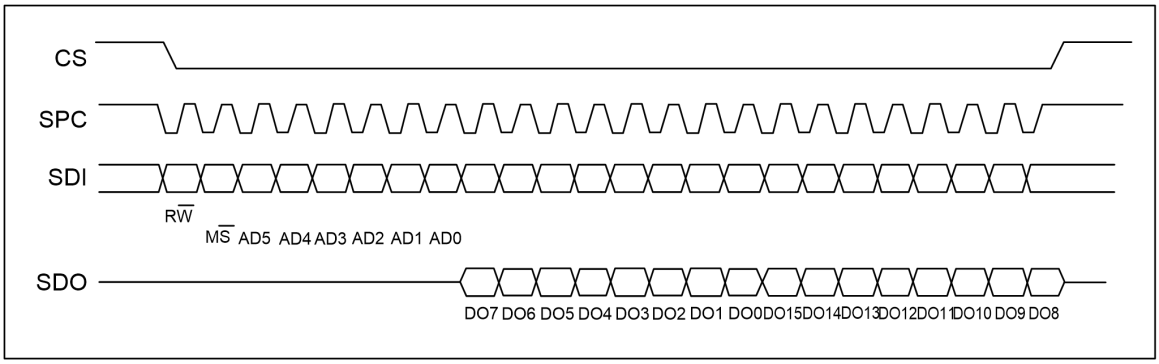
10.2.1 SPI read



SPI read protocol

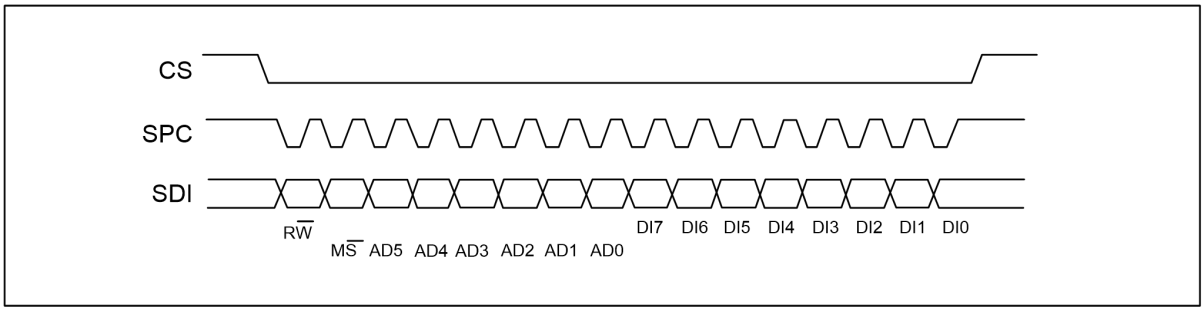
The SPI read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the pervious one.

- Bit0: read bit. The value is 1.
- Bit1: MS bit. When 0, do not increment address, when 1, increment address for multiple writing.
- Bit2-7: address AD(5:0), the register address.
- Bit8-15: data DO(7:0) (read mode), the data that is read from the slave device (MSB first).
- Bit16-…: data DO(…:8) (read mode), further data in multiple byte reading (MSB first).



Multiple bytes SPI read protocol (2 bytes example)

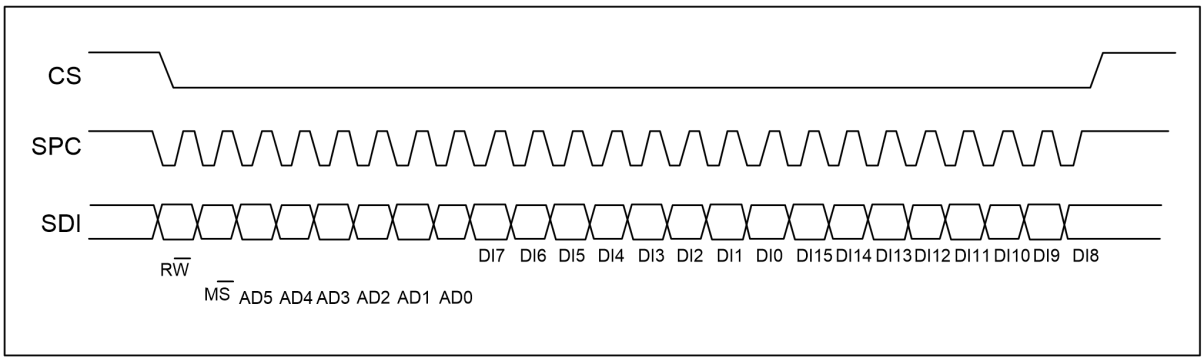
10.2.2 SPI write



SPI write protocol

The SPI write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the pervious one.

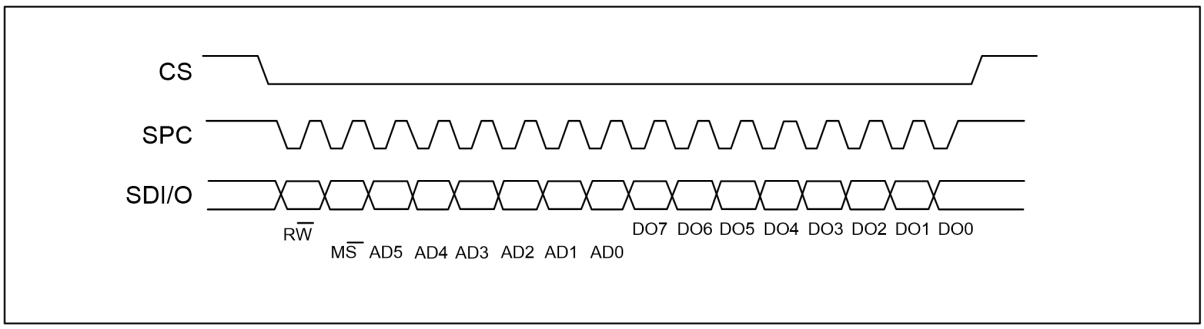
- Bit0: WRITE bit, the value is 0.
- Bit1: MS bit. When 0, do not increment address, when 1, increment address for multiple writing.
- Bit2-7: address AD(5:0), the register address.
- Bit8-15: data DI(7:0) (write mode), the data that is written inside the slave device (MSB first).
- Bit16-…: data DI(…:8) (write mode), further data in multiple byte writing (MSB first).



Multiple bytes SPI write protocol (2 bytes as an example)

10.2.3 SPI read in 3-wire mode

3-wire mode is entered by writing 1 to SIM bit. Only three signals lines are used in both 4-wire mode and 3-wire mode, and the logic and timing are both the same in these two modes, hence, it is able to configure the slave as 3-wire mode through 4-wire write mode.



SPI read protocol in 3-wire mode

The SPI read command is performed with 16 clock pulses.

- Bit0: read bit, the value is 1.
- Bit1: MS bit. When 0, do not increment address, when 1, increment address for multiple reading.
- Bit2-7: address AD(5:0), the register address.
- Bit8-15: data DO(7:0) (read mode), the data that is read from the slave device (MSB first).

When SPI mode is used to read three-axis FIFO data continuously, it needs to read from the register of 0x27, read 7 bytes of data continuously, and take the last 6 bytes to splice into three-axis data. Special attention: multiple SPI devices are forbidden to reuse SPC, MOSI and MISO.

11 Register mapping

The table given below lists all registers in LIS2DW12TR and their addresses and initial values.

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)	--	00-0B	--	--	Reserved
OUT_TEMP_L	r	0C	0001100	output	--
OUT_TEMP_H	r	0D	0001101	output	--
Reserved (do not modify)	--	0E	--	--	Reserved
WHO_AM_I	r	0F	000 1111	00010001	--
Reserved (do not modify)	--	10-12	--	--	Reserved
USER_CAL	--	13-1A	--	--	--
Reserved (do not modify)	--	1B-1D	--	--	Reserved
NVM_WR	rw	1E	001 1110	00000000	--
TEMP_CFG	rw	1F	001 1111	output	--
CTRL_REG1	rw	20	010 0000	00000111	--
CTRL_REG2	rw	21	010 0001	00000000	--
CTRL_REG3	rw	22	010 0010	00000000	--
CTRL_REG4	rw	23	010 0011	00000000	--
CTRL_REG5	rw	24	010 0100	00000000	--
CTRL_REG6	rw	25	010 0101	00000000	--
REFERENCE	rw	26	010 0110	00000000	--

Name	Type	Register address		Default	Comment
		Hex	Binary		
STATUS_REG	rw	27	010 0111	00000000	--
OUT_X_L(BLE=0)	r	28	010 1000	output	--
OUT_X_H(BLE=0)	r	29	010 1001	output	--
OUT_Y_L(BLE=0)	r	2A	010 1010	output	--
OUT_Y_H(BLE=0)	r	2B	010 1011	output	--
OUT_Z_L(BLE=0)	r	2C	010 1100	output	--
OUT_Z_H(BLE=0)	r	2D	010 1101	output	--
FIFO_CTRL_REG	rw	2E	010 1110	00000000	--
FIFO_SRC_REG	r	2F	010 1111	--	--
AOI1_CTRL_REG	rw	30	011 0000	00000000	--
AOI1_SRC	r	31	011 0001	00000000	--
AOI1_THS	rw	32	011 0010	00000000	--
AOI1_DURATION	rw	33	011 0011	00000000	--
AOI2_CTRL_REG	rw	34	011 0100	00000000	--
AOI2_SRC	r	35	011 0101	00000000	--
AOI2_THS	rw	36	011 0110	00000000	--
AOI2_DURATION	rw	37	011 0111	00000000	--
CLICK_CTRL_REG	rw	38	011 1000	00000000	--
CLICK_SRC	r	39	011 1001	00000000	--
CLICK_THS	rw	3A	011 1010	00000000	--
TIME_LIMIT	rw	3B	011 1011	00000000	--
TIME_LATENCY	rw	3C	011 1100	00000000	--
TIME_WINDOW	rw	3D	011 1101	00000000	--
DIG_CTRL	rw	57	101 0111	00000000	--

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

12 Register description

12.1 CTRL_REG1 (20h)

B7	B6	B5	B4	B3	B2	B1	B0
ODR3	ODR2	ODR1	ODR0	LPen	Zen	Yen	Xen

ODR3-0	Data rate selection, default value: 0000
LPen	Low power dissipation enable, default value: 0. (0: normal mode; 1: low power dissipation mode)

Zen	Z-axis enable, default value:1. (0: Z-axis disable, 1: Z-axis enable)
Yen	Y-axis enable, default value:1. (0: Y-axis disable, 1: Y-axis enable)
Xen	X-axis enable, default value:1. (0: X-axis disable, 1: X-axis enable)

ODR<3:0> is adopted for power supply mode and data rate selection. The frequency setting through ODR<3:0> is shown as below.

Data output rate setting:

ODR3	ODR2	ODR1	ODR0	Power supply mode selection
0	0	0	0	Power supply off mode
0	0	0	1	Normal l / low power dissipation mode (1 Hz)
0	0	1	0	Normal l / low power dissipation mode (10 Hz)
0	0	1	1	Normal l / low power dissipation mode (25 Hz)
0	1	0	0	Normal l / low power dissipation mode (50 Hz)
0	1	0	1	Normal l / low power dissipation mode (100 Hz)
0	1	1	0	Normal l / low power dissipation mode (200 Hz)
0	1	1	1	Normal l / low power dissipation mode (400 Hz)
1	0	0	0	low power dissipation mode (1.6 KHz)
1	0	0	1	Normal mode (1.25 kHz) / low power dissipation mode (5 KHz)

Note: during normal work:

1) When change from low ODR to high ODR, 0x97 (1.25 kHz/ Normal mode) should be configured first, then higher target ODR is configured.

2) After turning on DLPF_EN, 7 ODR clocks after sensor working are necessary to output the first data to register;

3) when ODR is small, acceleration amplitude may be affected after setting DLPF_EN to 1.

12.2 CTRL_REG2 (21h)

B7	B6	B5	B4	B3	B2	B1	B0
HPM1	HPM0	HPCF2	HPCF1	FDS	HPCLICK	HPIS2	HPIS1

HPM1-HPM0	High pass mode. Default value: 00 refer to “high pass mode configuration”
HPCF2 -HPCF1	High pass cutoff frequency selection
FDS	Data filtering selection. Default value: 0 (0: skip internal filtering; 1: data is output to data register or FIFO after filtering
HPCLICK	CLICK High pass filtering enable (0: filtering disable; 1: filtering enable)
HPIS2	Interrupt 2 AOI high pass filtering enable (0: filtering disable; 1: filtering enable)
HPIS1	Interrupt 1 AOI high pass filtering enable (0: filtering disable; 1: filtering enable)

High pass mode configuration

HPM1	HPM0	High pass filtering mode
0	0	Normal mode (read high pass filtering is reset automatically
0	1	Filtering reference signal
1	0	Normal mode
1	1	Interrupt event automatic reset

12.3 CTRL_REG3 (22h)

B7	B6	B5	B4	B3	B2	B1	B0
I1_CLICK	I1_AOI1	I1_AOI2	I1_DRDY1	I1_DRDY2	HI1_WTM	I1_OVERRUN	--

I1_CLICK	CLICK interrupt on INT1. Default value:0 (0: disable; 1: enable)
I1_AOI1	AOI1 interrupt on INT1. Default value:0 (0: disable; 1: enable)
I1_AOI2	AOI2 interrupt on INT1. Default value:0 (0: disable; 1: enable)
I1_DRDY1	DRDY1 interrupt on INT1. Default value:0 (0: disable; 1: enable)
I1_DRDY2	DRDY2 interrupt on INT1. Default value:0 (0: disable; 1: enable)
I1_WTM	FIFO interrupt on INT1. Default value:0 (0: disable; 1: enable)
I1_OVERRUN	FIFO interrupt on INT1. Default value:0 (0: disable; 1: enable)

12.4 CTRL_REG4 (23h)

B7	B6	B5	B4	B3	B2	B1	B0
BDU	BLE	FS1	FS0	DLPF_EN	ST1	ST0	SIM

BDU	Block data update. Default value: 0 (0: continuous update, 1: output is not updated until MSB and LSB are read)
BLE	Big/little-Endians data selection. Default value: 0 (0: low-byte data is in low-byte address; 1: high-byte data is in low-byte address;
FS1-FS0	Full scale selection. Default value: 00 (00: +/- 2G; 01: +/- 4G; 10: +/- 8G; 11: +/- 16G)

DLPF_EN	Low pass filtering mode enable. Default value: 0 (0: disable; 1: enable)
ST1-ST0	Self test enable. Default value: 00 (00: self test disable; others: refer to “self test mode configuration”)
SIM	SPI serial interface mode configuration. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

Self test mode configuration

ST1	ST0	Test mode
0	0	Normal mode
0	1	Self test 0
1	0	Self test 1

12.5 CTRL_REG5(24h)

B7	B6	B5	B4	B3	B2	B1	B0
BOOT	FIFO_EN	--	--	AOI1_LIR	AOI1_D4D	AOI2_LIR	AOI2_D4D

BOOT	Reload trimming value. Default value: 0 (0: normal mode; 1: reload trimming value)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable, FIFO mode of FIFO control register should be enabled at the same time)
AOI1_LIR	Interrupt response specified by lockoff interrupt AOI1 configuration register Interrupt lockout signal can be cleared through reading AOI1 configuration register. Default value: 0 (0: interrupt signal is unlocked; 1: interrupt signal is locked)
AOI1_D4D	4D enable: 4D detection is enable on AOI1, 6D of AOI1 configuration register is set to 1.
AOI2_LIR	Interrupt response specified by lockout interrupt AOI2 configuration register (H/L on PIN) Interrupt lockout signal can be cleared through reading AOI2 configuration register. Default value: 0 (0: interrupt signal is unlocked; 1: interrupt signal is locked)
AOI2_D4D	4D 使能： 使能 AOI2 上 4D 检测，需要同时要把 AOI2 配置寄存器中的 6D 为置 1。 4D enable: 4D detection is enable on AOI2, 6D of AOI2 configuration register is set to 1.

12.6 CTRL_REG6(25h)

B7	B6	B5	B4	B3	B2	B1	B0
I2_CLICK	I2_AOI1	I2_AOI2	I2_BOOT	0	--	H_LACTIVE	--

I2_CLICK	CLICK interrupt on INT2. Default value: 0 (0: disable; 1: enable)
I2_AOI1	AOI2 interrupt on INT1. Default value: 0 (0: disable; 1: enable)
I2_AOI2	AOI2 interrupt on INT2. Default value: 0 (0: disable; 1: enable)
I2_BOOT	BOOT interrupt on INT2. Default value: 0 (0: disable; 1: enable)
H_LACTIVE	Interrupt pin default control bit. Default value: 0 0: interrupt triggered by high level; 1: interrupt triggered by low level

12.7 Status register (27h)

B7	B6	B5	B4	B3	B2	B1	B0
ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

ZYXOR	One or more data of X/Y/Z-axis is covered by new data. Default value: 0 (0: no data of X/Y/Z-axis is covered by new data; 1: one or more data of X/Y/Z-axis is covered by new data
ZOR	Data of Z-axis is covered by new data. Default value: 0 (0: data of Z-axis is not covered by new data 1: data of Z-axis is covered by new data)
YOR	Data of Y-axis is covered by new data. Default value: 0 (0: data of Y-axis is not covered by new data 1: data of Y-axis is covered by new data)
XOR	Data of X-axis is covered by new data. Default value: 0 (0: data of X-axis is not covered by new data 1: data of X-axis is covered by new data)
ZYXDA	All data of X/Y/Z-axis are covered by new data. Default value: 0 (0: One or more data of X/Y/Z-axis is not covered by new data; 1: All data of X/Y/Z-axis are covered by new data.)
ZDA	Z-axis old data is covered by new data. Default value: 0 (0:Z-axis old data is not covered by new data; 1: Z-axis old data is covered by new data)
YDA	Y-axis old data is covered by new data. Default value: 0 (0:Y-axis old data is not covered by new data; 1: Y-axis old data is covered by new data)
XDA	X-axis old data is covered by new data. Default value: 0 (0:X-axis old data is not covered by new data; 1: X-axis old data is covered by new data)

Note: Whether the new data is in position can be judged by: If((Read(0x27)&0x0F)==0x0F){break;}

12.8 OUT_X_L(LSB), OUT_X_H (MSB)

X-axis accelerometer value, data is expressed as 2's complement number.

BLE	(28h)	(29h)
BLE=0	OUT_X_L	OUT_X_H
BLE=1	OUT_X_H	OUT_X_L

12.9 OUT_Y_L (LSB),OUT_Y_H (MSB)

Y-axis accelerometer value, data is expressed as 2's complement number.

BLE	(2Ah)	(2Bh)
BLE=0	OUT_Y_L	OUT_Y_H
BLE=1	OUT_Y_H	OUT_Y_L

12.10 OUT_Z_L (LSB),OUT_Z_H (MSB)

Z-axis accelerometer value, data is expressed as 2's complement number.

BLE	(2Ch)	(2Dh)
BLE=0	OUT_Z_L	OUT_Z_H
BLE=1	OUT_Z_H	OUT_Z_L

Take X- axis as an example:

OUT_X_H	OUT_X_L	16bits (DEC)	10bits (DEC)	FS[1:0]=00	FS[1:0]=01	FS[1:0]=10	FS[1:0]=11
0x40	0x00	16384	256	1.0g	2.0g	4.0g	8.0g
0x20	0x00	8192	128	0.5g	1.0g	2.0g	4.0g
0xE0	0x00	-8192	-128	-0.5g	-1.0g	-2.0g	-4.0g
0xC0	0x00	-16384	-256	-1.0g	-2.0g	-4.0g	-8.0g

```
unsigned  char  X_H,X_L,Y_H,Y_L,Z_H, Z_L;                    // Three-axis data (high and low)
signed short int  SL_ACCEL_X,SL_ ACCEL_Y,SL_ ACCEL_Z ;   // Three-axis data
SL_ACCEL_X =  (signed short int) ((X_H<< 8) | X_L);          // Merging data
SL_ACCEL_Y =  (signed short int) ((Y_H<< 8) | Y_L);          // Forcing data type conversion
SL_ACCEL_Z =  (signed short int) ((Z_H<< 8) | Z_L);          // 16 bit signed integer data
SL_ACCEL_X =   SL_ ACCEL_X>>6;                                // Take 10 signed integer data, same to Y,Z
```

12.11 FIFO_CFG(2Eh)

B7	B6	B5	B4	B3	B2	B1	B0
FM1	FM0	TR	FTH4	FTH3	FTH2	FTH1	FTH0

FM[1:0]	FIFO mode selection. Default value: 00 00: By-Pass mode (bypass mode, i.e., FIFO function is unused)

	01: FIFO mode (new data is discarded if the cache is full) 10: Stream mode (the oldest data is discarded and new data is added when the cache is full) 11: trigger mode (enter FIFO mode from stream mode when AOI1/AOI2 interrupt event is valid)
TR	FIFO trigger mode selection. Default value: 0 0: AOI1 interrupt as FIFO trigger mode interrupt event input 1: AOI2 interrupt as FIFO trigger mode interrupt event input
FTH[4:0]	FIFO function WTM threshold setting When the number of data in FIFO exceeds the threshold, corresponding status bit of FIFO status register will be set to “1”.

Note: when the accelerometer is working in FIFO mode, if FIFO data is accessed, users need to switch the FIFO mode to BY-PASS mode, and then switch back to FIFO mode to continue working.

12.12 FIFO_SRC(2Fh)

B7	B6	B5	B4	B3	B2	B1	B0
WTM	OVER	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

WTM	When the number of data in FIFO exceeds the threshold, WTM bit is set to “1”.
OVER	When the number of data in FIFO overflows, OVER bit is set to “1”.
EMPTY	When there is no data in FIFO, EMPTY bit is set to “1”.
FSS[4:0]	Number of unread data in FIFO. When a group of data in FIFO is accessed, FIFO data group number register will be automatically decreased by one.

Note: when B6(OVER)==1, 32 groups of FIFO data can be accessed.

12.13 AOI1_CRTL_REG (30h)

B7	B6	B5	B4	B3	B2	B1	B0
AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

AOI	And/or interrupt. Default value: 0. Refer to “interrupt mode”
6D	6D test enable. Default value: 0. Refer to “interrupt mode”
ZHIE/ ZUPE	Z-axis high interrupt or Z-axis direction test interrupt enable. Default value: 0. (0:Interrupt disabled; 1: interrupt enabled)
ZLIE/ ZDOWNE	Z-axis low interrupt or Z-axis direction test interrupt enable. Default value: 0. (0:Interrupt disabled; 1: interrupt enabled)
YHIE/ YUPE	Y-axis high interrupt or Y-axis direction test interrupt enable. Default value: 0. (0:Interrupt disabled; 1: interrupt enabled)
YLIE/	Y-axis low interrupt or Y-axis direction test interrupt enable. Default value: 0.

YDOWNE	(0:Interrupt disabled; 1: interrupt enabled)
XHIE/ XUPE	X-axis high interrupt or X-axis direction test interrupt enable. Default value: 0. (0:Interrupt disabled; 1: interrupt enabled)
XLIE/ XDOWNE	X-axis low interrupt or X-axis direction test interrupt enable. Default value: 0. (0:Interrupt disabled; 1: interrupt enabled)

AOI	6D	Interrupt mode
0	0	Or interrupt event
0	1	6D Motion Recognition
1	0	And interrupt event
1	1	6D position detection

12.14 AOI1_SRC (31h)

B7	B6	B5	B4	B3	B2	B1	B0
--	IA	ZH	ZL	YH	YL	XH	XL

IA	AOI1 interrupt activation. Default value: 0. (0: no interrupt ; 1: one or more interrupt occurs)
ZH	Z-axis high. Default value: 0. (0: no interrupt ; 1: Z-axis high event occurs)
ZL	Z-axis low. Default value: 0. (0: no interrupt ; 1: Z-axis low event occurs)
YH	Y-axis high. Default value: 0. (0: no interrupt ; 1: Y-axis high event occurs)
YL	Y-axis low. Default value: 0. (0: no interrupt ; 1: Y-axis low event occurs)
XH	X-axis high. Default value: 0. (0: no interrupt ; 1: X-axis high event occurs)
XL	X-axis low. Default value: 0. (0: no interrupt ; 1: X-axis low event occurs)

12.15 AOI1_THS (32h)

B7	B6	B5	B4	B3	B2	B1	B0
--	THS6	THS5	THS4	THS3	THS2	THS1	THS0

THS6 - THS0	**AOI1** threshold. Default value: 000 0000 1LSB=16mg @ FS=2g 1LSB=32mg @ FS=4g 1LSB=64mg @ FS=8g 1LSB=128mg @ FS=16g

12.16 AOI1_DURATION (33h)

B7	B6	B5	B4	B3	B2	B1	B0
--	D6	D5	D4	D3	D2	D1	D0

D6 - D0	Duration count value, 1LSB = 1/ODR. Default value: 000 0000 Min. duration of AOI1 is recognized through D6 - D0 position recognition. Max. duration and step is counted with clock of ODR. For example: to set D[6:0]=000 1000, the data of axis should be set to be continuously greater than the threshold 8 times.

Description of AOI1 interrupt data source:

According to the combinatorial logic of interrupt events, they are divided into AND events and OR events. As the name implies, AND event refers to the occurrence of multiple specified events at the same time to trigger an interrupt, OR event refers to the occurrence of any event of multiple specified events to trigger an interrupt; for example, the X-axis data is greater than the set threshold or the Y-axis data is greater than the set threshold, OR event interrupt function is needed; this function can be used for activity detection, in general, you need to configure high passed data as the data source.

According to the function of interrupt events, they are divided into direction motion recognition events and direction position recognition events. Direction motion recognition event means that the device will generate an interrupt from one direction (known or unknown) to another known direction, and the interrupt response time is 1/ODR. The direction position recognition event means that the device will trigger an interrupt when it is in a stable known direction, if the device is always at this preset known direction position, the level after interrupt triggered will remain unchanged. This function can be used for attitude detection, generally, the high-passed data cannot be configured as the data source of this function, and the threshold value that needs to be set is large, and the duration of the setting state is large.

6D/4D/3D recognition function:

When 6D function bit (30.6h) is not set to 1, the 3D function is realized;

When 6D function bit (30.6h) is set to 1, and 4D function bit (24.0h or 24.2h) is not set to 1, the 6D function is realized;

When 6D function bit (30.6h) is set to 1, and 4D function bit (24.0h or 24.2h) is set to 1, the 4D function is realized;

3D recognition function: if X-axis high event trigger is configured, it is triggered only when the absolute value of X data is greater than the threshold, i.e., both positive and negative data can trigger interrupts.

Before trigger, XL=1; after trigger, XH=1;

6D recognition function: if X-axis high event trigger is configured, it is triggered when X data is greater than the threshold, i.e., only positive data can trigger interrupts.

Before trigger, XH=0; after trigger XH=1. In order to trigger an interrupt when the absolute value of the data in both directions are large, it is necessary to configure X-axis high event trigger and X-axis low event trigger simultaneously.

Before trigger, XH=0, XL=0; after trigger, XH=1 or XL=1;

4D recognition function: in this configuration, the Z-axis position detection function id disabled, thus reducing position recognition.

The configurations of AOI2 are the same as the one of AOI1.

Note: when the AND/OR interrupt and the motion position interrupt are judging the number of times greater than the threshold, the count value is incremented by one in each case, and decremented by one in each case of failure; if the highest bit of AOI_DURATION is set to 1 (D7), it is possible to reduce the interrupt false trigger during judging the number of times greater than the threshold.

12.17 AOI2_CRTL_REG (34h)

B7	B6	B5	B4	B3	B2	B1	B0
AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

AOI	And/or interrupt. Default value: 0. Refer to “interrupt mode”
6D	6D test enable. Default value: 0. Refer to “interrupt mode”
ZHIE/ ZUPE	Z-axis high interrupt or Z-axis direction test interrupt enable. Default value: 0. (0:Interrupt is disable; 1: interrupt is enable)
ZLIE/ ZDOWNE	Z-axis low interrupt or Z-axis direction test interrupt enable. Default value: 0. (0:Interrupt is disable; 1: interrupt is enable)
YHIE/ YUPE	Y-axis high interrupt or Y-axis direction test interrupt enable. Default value: 0. (0:Interrupt is disable; 1: interrupt is enable)
YLIE/ YDOWNE	Y-axis low interrupt or Y-axis direction test interrupt enable. Default value: 0. (0:Interrupt is disable; 1: interrupt is enable)
XHIE/ XUPE	X-axis high interrupt or X-axis direction test interrupt enable. Default value: 0. (0:Interrupt is disable; 1: interrupt is enable)
XLIE/ XDOWNE	X-axis low interrupt or X-axis direction test interrupt enable. Default value: 0. (0:Interrupt is disable; 1: interrupt is enable)

AOI	**6D**	**Interrupt mode**
0	0	Or interrupt event
0	1	6D Motion Recognition
1	0	And interrupt event
1	1	6D position detection

12.18 AOI2_SRC (35h)

B7	B6	B5	B4	B3	B2	B1	B0
--	IA	ZH	ZL	YH	YL	XH	XL

IA	AOI2 interrupt activation. Default value: 0. (0: no interrupt ; 1: one or more interrupt occurs)
ZH	Z-axis high. Default value: 0. (0: no interrupt ; 1: Z-axis high event occurs)

ZL	Z-axis low. Default value: 0. (0: no interrupt ; 1: Z-axis low event occurs)
YH	Y-axis high. Default value: 0. (0: no interrupt ; 1: Y-axis high event occurs)
YL	Y-axis low. Default value: 0. (0: no interrupt ; 1: Y-axis low event occurs)
XH	X-axis high. Default value: 0. (0: no interrupt ; 1: X-axis high event occurs)
XL	X-axis low. Default value: 0. (0: no interrupt ; 1: X-axis low event occurs)

12.19 AOI2_THS (36h)

B7	B6	B5	B4	B3	B2	B1	B0
--	THS6	THS5	THS4	THS3	THS2	THS1	THS0

THS6 - THS0	**AOI2** threshold. Default value: 000 0000 1LSB=16mg @ FS=2g 1LSB=32mg @ FS=4g 1LSB=64mg @ FS=8g 1LSB=128mg @ FS=16g

12.20 AOI2_DURATION (37h)

B7	B6	B5	B4	B3	B2	B1	B0
--	D6	D5	D4	D3	D2	D1	D0

D6 - D0	Duration count value, 1LSB = 1/ODR. Default value: 000 0000 Min. duration of AOI2 is recognized through D6 - D0 position recognition. Max. duration and step is counted with clock of ODR. For example: to set D[6:0]=000 1000, the data of axis should be set to be continuously greater than the threshold 8 times.

12.21 CLICK_CRTL_REG (38h)

B7	B6	B5	B4	B3	B2	B1	B0
--	--	ZD	ZS	YD	YS	XD	XS

ZD	Z-axis double-click interrupt enable control. Default value: 0 (0: interrupt request disabled; 1: interrupt request enabled)
ZS	Z-axis single-click interrupt enable control. Default value: 0 (0: interrupt request disabled; 1: interrupt request enabled)
YD	Y-axis double-click interrupt enable control. Default value: 0

	(0: interrupt request disabled; 1: interrupt request enabled)
YS	Y-axis single-click interrupt enable control. Default value: 0 (0: interrupt request disabled; 1: interrupt request enabled)
XD	X-axis double-click interrupt enable control. Default value: 0 (0: interrupt request disabled; 1: interrupt request enabled)
XS	X-axis single-click interrupt enable control. Default value: 0 (0: interrupt request disabled; 1: interrupt request enabled)

12.22 CLICK_SRC (39h)

B7	B6	B5	B4	B3	B2	B1	B0
--	IA	DCLICK	SCLICK	Sign	Z	Y	X

IA	Interrupt activation. Default value: 0 (0: no interrupt generated; 1: one or more interrupts have been generated)
DCLICK	Double-click detection status bit. Default value: 0 (0: No double-click detected; 1: double-click detected)
SCLICK	Single-click detection status bit. Default value: 0 (0: No single-click detected; 1: single-click detected)
Sign	Positive/negative direction detected. (0: positive direction detected; 1: negative direction detected)
Z	Single/double-click detected at Z-axis. Default value: 0 (0: No interrupt detected; 1: interrupt detected)
Y	Single/double-click detected at Y-axis. Default value: 0 (0: No interrupt detected; 1: interrupt detected)
X	Single/double-click detected at X-axis. Default value: 0 (0: No interrupt detected; 1: interrupt detected)

12.23 CLICK_THS (3Ah)

B7	B6	B5	B4	B3	B2	B1	B0
--	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Ths6 - Ths0	The threshold for single/double-click trigger. Default value: 000 0000

12.24 TIME_LIMIT (3Bh)

B7	B6	B5	B4	B3	B2	B1	B0
--	TLI6	TLI 5	TLI 4	TLI 3	TLI 2	TLI 1	TLI 0

TLI 6 - TLI 0	Threshold for single-click detection time. Default value: 000 0000

12.25 TIME_LATENCY (3Ch)

B7	B6	B5	B4	B3	B2	B1	B0
TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

TLA7 – TLA0	Delay time. Default value: 000 0000

12.26 TIME_WINDOW (3Dh)

B7	B6	B5	B4	B3	B2	B1	B0
TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

TW7 – TW0	Time window. Default value: 000 0000

12.27 ACT_THS (3Eh)

B7	B6	B5	B4	B3	B2	B1	B0
--	Acth6	Acth5	Acth4	Acth3	Acth2	Acth1	Acth0
0	0	0	0	0	0	0	0

Acth[6:0]	When waking up from low power mode, the three-axis data need to be greater than the threshold. Default value: 000 0000 1LSb = 16mg @FS=2g 1LSb = 32 mg @FS=4g 1LSb = 62 mg @FS=8g 1LSb = 186 mg @FS=16g

12.28 Act_DUR (3Fh)

B7	B6	B5	B4	B3	B2	B1	B0
ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0
0	0	0	0	0	0	0	0

ActD[7:0]	The duration required from wake-up mode to low-power mode. Default: 0000 0000; T = (8*N+1)/ODR If any axis data is greater than Acth within this duration, the duration count will not be cleared. It is possible to disable low power wake-up function through setting ActD[7:0] to 0x00, otherwise it will automatically enter low power dissipation.

12.29 DIG_CTRL (57h)

B7	B6	B5	B4	B3	B2	B1	B0
--	--	--	--	SDO_PU	I2C_PU	--	--

SDO_PU	SDO internal pull-up resistor control bit. Default value: 0 (0: pull-up resistor enabled; 1: pull-up resistor disabled) This pin is in floating input mode after pull-up resistor disabled, please ensure that the peripheral level of the pin is determined, otherwise I²C communication will be abnormal.
I2C_PU	SDA and SCL internal pull-up resistor control bit. Default value: 0 (0: pull-up resistor enabled; 1: pull-up resistor disabled) This pin is in open drain mode after pull-up resistor disabled, please ensure that there is a pull-up resistor at the peripheral of the pin.

Note: 0x57 register realizes corresponding operation by I²C communication mode.

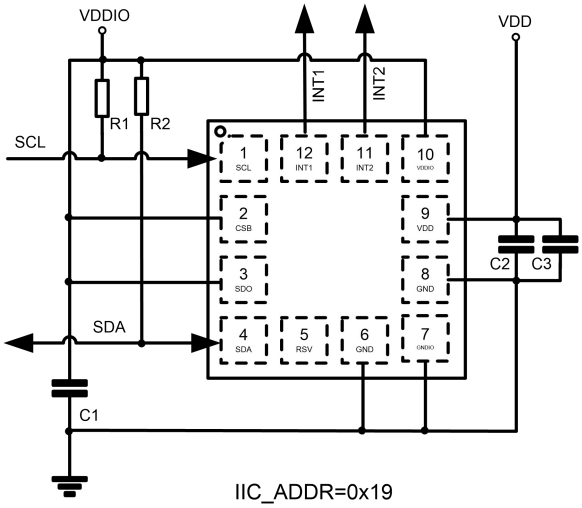
To turn off the SDO internal pull-up resistor separately:

```
Write(0x1E,0x05);        // Open operation authority, write 0x05 to 0x1E register
Read(0x57,sl_val);       // Read current configuration of register 0x57
sl_val=sl_val|0x08;      // Set SDO_PU to 1
Write(0x57,sl_val);      // Operate the SDO_PU bit, write configuration to 0x57 register
Write(0x1E,0x00);        // Close operation authority, write 0x00 to 0x1E register
```

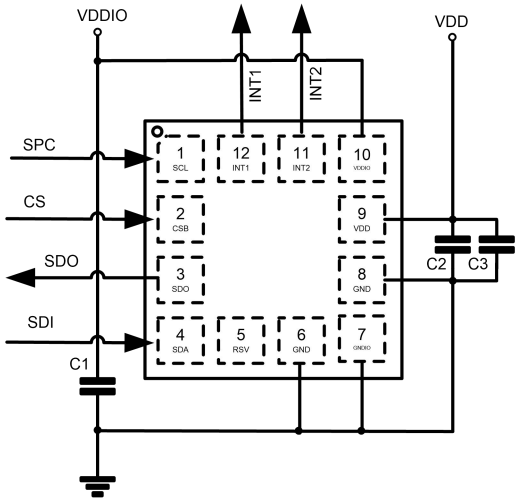
To turn off the I²C internal pull-up resistor separately:

```
Write(0x1E,0x05);        // Open operation authority, write 0x05 to 0x1E register
Read(0x57,sl_val);       // Read current configuration of 0x57 register
sl_val=sl_val|0x04;      // Set I²C_PU to 1
Write(0x57,sl_val);      // Operate I²C_PU bit, write configuration to 0x57 register
Write(0x1E,0x00);        // Close operation authority, write 0x00 to 0x1E register
```

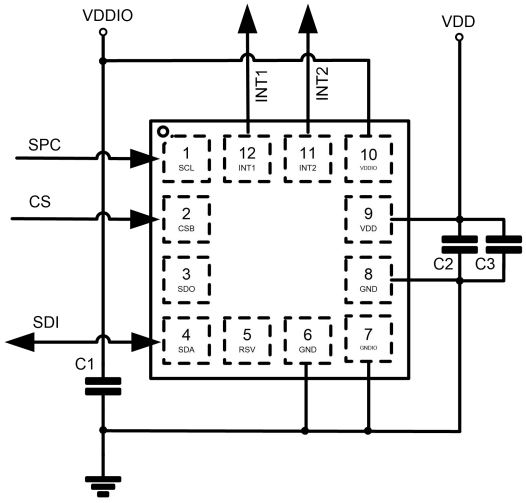
Typical Application Circuit



IIC_ADDR=0x19



4-wire SPI



3-wire SPI

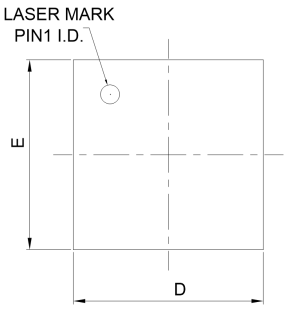
Note: C_1 and C_2 are recommended to be 100nF, C3 to be 10uF, while R_1 and R_2 to be 4.7KΩ.

When SPI communication is adopted, it is forbidden to use SPI bus (SDA/SDI/SDO/SPC) by various devices.

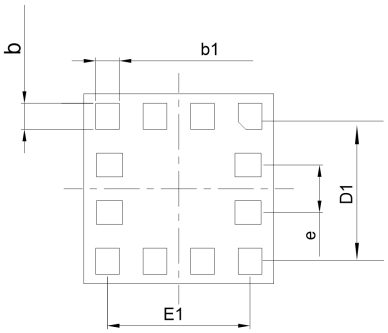
The device core is supplied through V_{DD} while the I/Os are supplied through V_{DDIO}. All the voltage and ground supplies must be present at the same time to have proper behavior of the IC. Voltage at CS/SDO/SCL/SDA/INT1/INT2 should not be higher than V_{DDIO}+0.3V.

Package Outline

LGA-12-2x2x1.0　单位：mm

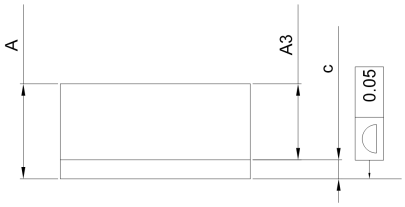


TOP VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.930	—	1.050
A3	0.650	—	0.850
c	0.130	—	0.300
D	1.900	2.000	2.100
E	1.900	2.000	2.100
D1	1.520 BSC		
E1	1.500 BSC		
b	0.220	0.275	0.325
b1	0.200	0.250	0.300
e	0.450	0.500	0.550



Seating plane

MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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