

Motorcomm

YT9213NB Datasheet

**LAYER 2 MANAGED 2+1 PORT 10/100/1000M
SWITCH CONTROLLER**

Issue V1.01

Date 2024-12-12

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General Description

YT9213NB is a QFN76 E-PAD, high-performance 2+1-port Gigabit Ethernet Switch. It integrates 2 PHY support 1000Base-T/100Base-Tx/10Base-Te, and 1 extra MAC port for specific applications which supports MII/RMII/RGMII/SGMII/1000Base-X/100Base-FX/2500Base-X.

The integrated GIGA-PHY complies with 10BASE-Te, 100BASE-TX, and 1000BASE-T IEEE standard 802.3 and also supports Motorcomm's proprietary LRE100-4 feature, which makes the device can auto-negotiate and link up with LRE100-4 compliant link partners. LRE100-4 in extended cable length applications up to 400 meters at 100Mbps over CAT5E cable.

The extension GMAC of the YT9213NB supports xMII or SerDes interfaces for connecting with an external PHY, MAC, external CPU, or RISC in specific applications, and also provides an optical port directly by SerDes. The xMII refers to Reduced Gigabit Media Independent Interface (RGMII), Media Independent Interface (MII), and Reduced Media Independent Interface (RMII). The SerDes supports IEEE SGMII, IEEE 1000Base-X, and IEEE 2500Base-X.

YT9213NB integrates a 4K look-up table with an efficient hashing algorithm for address searching and learning, each entry can be configured as a static entry.

YT9213NB supports IEEE 802.1Q VLAN and has a 4K-entry VLAN table. It provides VLAN classification according to port-based, protocol-based, VLAN translation, flow-based capability, and MAC-based. IP-subnet-based VLAN can be supported by configuration. It also supports IVL, SVL, and IVL/SVL for flexible network topology architecture.

YT9213NB supports standard 802.3x flow control frames for full duplex and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources. YT9213NB supports storm control.

YT9213NB supports 384-hardware entry ACL rule check and multiple action options, to support flexible traffic classification. The 384 entries are composed of 48 rows, each row has 8 entries. To support long rule, rule extension is supported by any combination of the 8 entries for each row. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action is configurable to Drop/Permit/Redirect/Mirror, change priority/DSCP value in 802.1q/Q tag, and rate policing.

Key Features

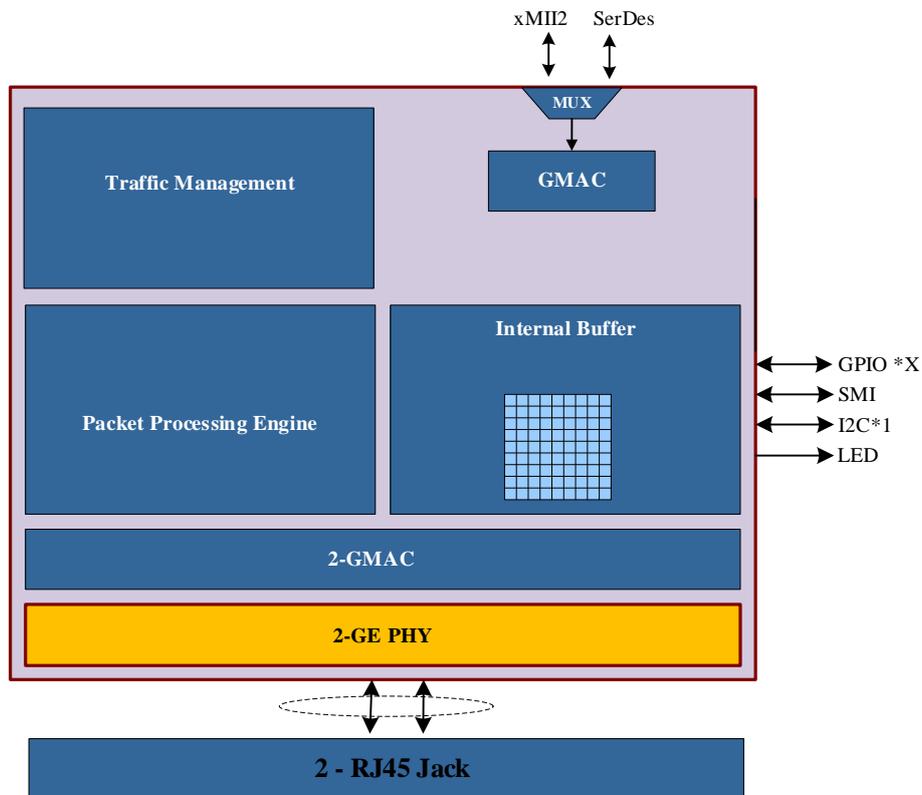
- High performance, nonblocking, 3 port Ethernet Switch integrating:
 - Two 10/100/1000Mbps PHYs with Advanced Cable Status Diagnostic (CSD)
 - Each PHY supports 10/100/1000M full duplex connectivity (half duplex only supported in 10/100M mode)
 - Full duplex and half duplex operation with IEEE 802.3x flow control and backpressure
- Interface
 - Embedded 2-port 1000Base-T/100Base-TX/10Base-Te PHY
 - Embedded one 3.125Gbps/1.25Gbps SerDes for 2500Base-X/SGMII/1000Base-X/100Base-FX
 - Embedded one RGMII/MII/RMII interface
- Advanced Features

- Support parallel LED output
- Support SMI/IIC Slave interface
- Support 1 interrupt output to external CPU for notification
- Support 64K-byte EEPROM space
- Link on cable length power saving
- Link down power saving
- Support 9K byte jumbo frames
- Support 2 IEEE 802.3ad Link aggregation port groups
- Security Filtering
 - Disable learning for each port
 - Disable learning-table aging for each port
 - Unknown DA filter mask
 - Support Port Isolation
 - Support Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
 - Support DOS attack prevention
- Control, Management, and Statistics
 - Support RFC MIB Counters
 - MIB-II (RFC 1213)
 - Ethernet-Like MIB (RFC 3635)
 - Interface Group MIB (RFC 2863)
 - RMON (RFC 2819)
 - Bridge MIB (RFC 1493)
 - Bridge MIB Extension (RFC 2674)
 - Support OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol)
 - Support Loop Detection
- Packet Process Engine
 - Support 802.1Q VLAN
 - Support 4K VLAN
 - Support untagged definition in each VLAN
 - Support VLAN policing and VLAN forwarding decision
 - Support port-based, tag-based, and protocol-based VLAN
 - Support per port egress VLAN tagged and untagged
 - Support IEEE 802.1D/s/w Spanning Tree Protocols
 - Support Multicast VLAN (MVR)
 - Support IVL, SVL, and IVL/SVL
 - Support IEEE 802.1ad Stacking VLAN
 - Support VLAN translation (1:1/2:1/2:2/N:1)

- Support IEEE 802.1x Access Control Protocol
 - Port-Based Access Control
 - MAC-Based Access Control
 - Guest VLAN
- Support ACL Rules
- Support Hardware/Software IGMP/MLD Snooping
 - Support fast leave
 - Support IGMP v1/v2/v3
 - Static/Dynamic Router port
- Mirror
 - Port-based mirror
 - Flow-based mirror
- Support reserved multicast control
- Support WOL
- Quality of Service (QoS)
 - Support queue-based DWRR/SP, packet/byte modes are both supported for DWRR
 - Support min-max queue-based shaping, packet/byte modes are both supported
 - Support single token bucket for port-based shaping, packet/byte modes are both supported
 - Support per port input bandwidth control, packet/byte modes are both supported
 - trTCM color aware/blind packet/byte modes
 - Traffic classification based on multiple source type
 - Support 8 unicast queues and 4 multicast queues for each port
 - Tail drop is supported for UQ/MQ, WRED is supported for UQ
- 25MHz crystal or 3.3V OSC input
- QFN 76-pin E-PAD package

Block Diagram

Figure 1 Block Diagram



System Applications

- 2-Port 1000Base-T+1-Port RGMII
- 2-Port 1000Base-T+1-Port 2500Base-X Switch
- 2-Port 1000Base-T Router with Single MII/RGMII
- 2-Port 1000Base-T Router with Single SGMII
- 2-Port 1000Base-T NVR
- 2-Port 1000Base-T ONU

Revision History

Revision	Release Date	Description
V1.01	2024-12-12	<ul style="list-style-type: none">Update Mechanical Information K, see 9 Mechanical Information.Update TskewR value, Data Input Hold Time min value, and AC Coupling Capacitor max value, see 7.4 AC Characteristics.
V1.0	2024-11-07	First version.

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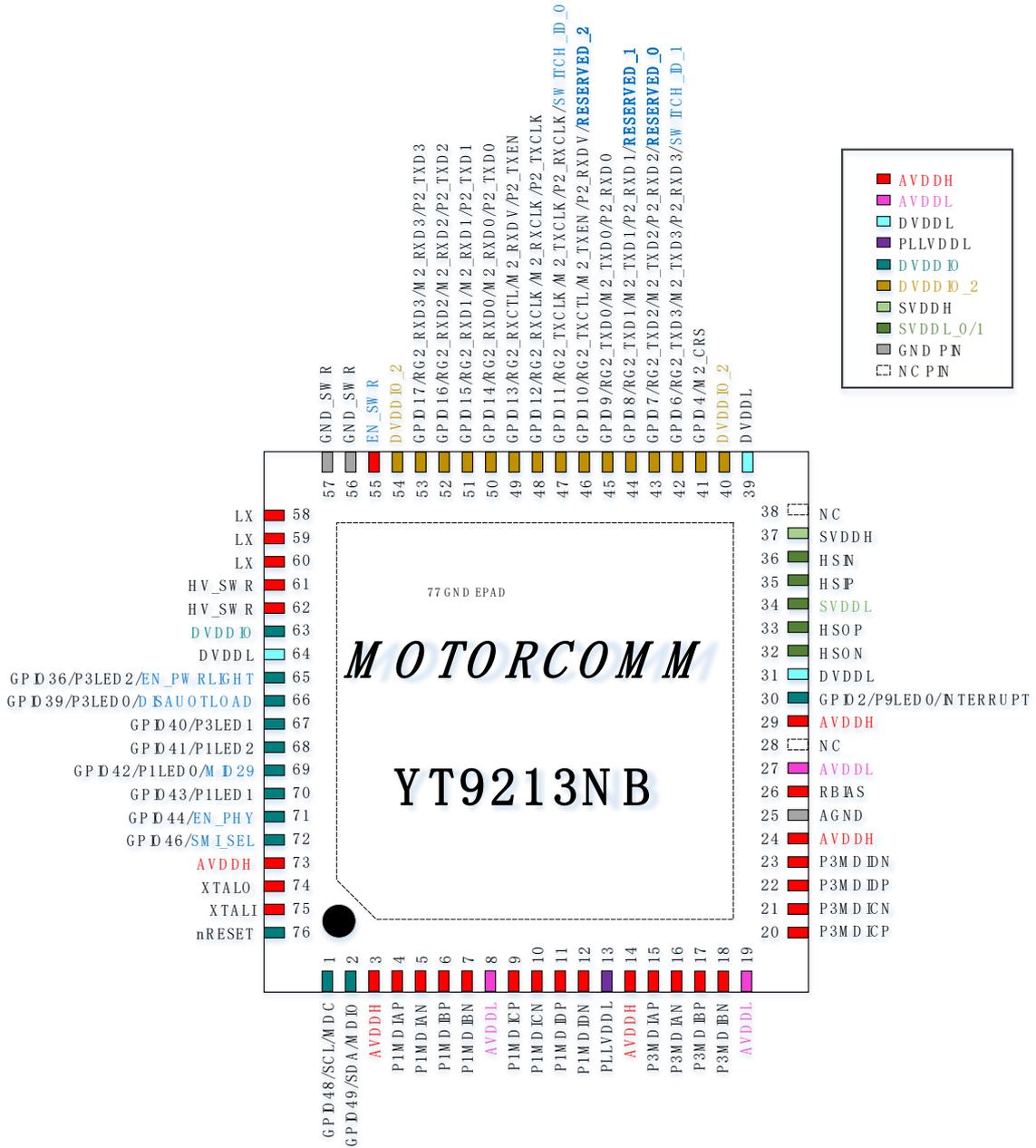
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1 Pin Assignment

1.1 Pin Assignment

The pin map is shown in the following figure.

Figure 2 Pin Assignment



1.2 Pin Assignment Table

Some pins have multiple functions.

Refer to the Pin Assignment figures for a graphical representation.

- I: Input
- O: Output
- IO: Bidirectional Input and Output
- P: Digital Power Pin
- G: Digital Ground Pin
- PU: Internal Pull Up
- LI: Latched Input During Power Up
- OD: Open Drain
- AI: Analog Input
- AO: Analog Output
- AIO: Analog Bidirectional Input and Output
- AP: Analog Power Pin
- AG: Analog Ground Pin
- PD: Internal Pull Down
- XT: Crystal Related

Table 1 Pin Assignment

No.	Pin Name	Type
1	GPIO48/SCL/MDC	IO/PU/OD
2	GPIO49/SDA/MDIO	IO/PU/OD
3	AVDDH	AP
4	P1MDIAP	AIO
5	P1MDIAN	AIO
6	P1MDIBP	AIO
7	P1MDIBN	AIO
8	AVDDL	AP
9	P1MDICP	AIO
10	P1MDICN	AIO
11	P1MDIDP	AIO
12	P1MDIDN	AIO
13	PLLVDL	AP
14	AVDDH	AP
15	P3MDIAP	AIO
16	P3MDIAN	AIO
17	P3MDIBP	AIO
18	P3MDIBN	AIO
19	AVDDL	AP
20	P3MDICP	AIO
21	P3MDICN	AIO
22	P3MDIDP	AIO
23	P3MDIDN	AIO
24	AVDDH	AP
25	AGND	AG
26	RBIAS	AO
27	AVDDL	AP
28	NC	-
29	AVDDH	AP
30	GPIO2/P9LED0/ INTERRUPT	IO/PU/OD
31	DVDDL	P

No.	Pin Name	Type
32	HS0N	AO
33	HS0P	AO
34	SVDDL	AP
35	HSIP	AI
36	HSIN	AI
37	SVDDH	AP
38	NC	-
39	DVDDL	P
40	DVDDIO_2	P
41	GPIO4/M2_CRS	IO/PD
42	GPIO6/RG2_TXD3/M2_TXD 3/P2_RXD3/SWITCH_ID_1	IO/LI/PD
43	GPIO7/RG2_TXD2/M2_TXD 2/P2_RXD2/RESERVED_0	IO/PU
44	GPIO8/RG2_TXD1/M2_TXD 1/P2_RXD1/RESERVED_1	IO/PU
45	GPIO9/RG2_TXD0/M2_TXD 0/P2_RXD0	IO/LI/PD
46	GPIO10/RG2_TXCTL/M2_T XEN/P2_RXDV/RESERVED_ 2	IO/PD
47	GPIO11/RG2_TXCLK/M2_T XCLK/P2_RXCLK/SWITCH_ ID_0	IO/LI/PD
48	GPIO12/RG2_RXCLK/M2_R XCLK/P2_TXCLK	IO/PU
49	GPIO13/RG2_RXCTL/M2_R XDV/P2_TXEN	IO/PU
50	GPIO14/RG2_RXD0/M2_RX D0/P2_TXD0	IO/PU
51	GPIO15/RG2_RXD1/M2_RX D1/P2_TXD1	IO/PU
52	GPIO16/RG2_RXD2/M2_RX D2/P2_TXD2	IO/PU

No.	Pin Name	Type
53	GPIO17/RG2_RXD3/M2_RXD3/P2_TXD3	IO/PU
54	DVDDIO_2	P
55	EN_SWR	AI
56	GND_SWR	AG
57	GND_SWR	AG
58	LX	AO
59	LX	AO
60	LX	AO
61	HV_SWR	AP
62	HV_SWR	AP
63	DVDDIO	P
64	DVDDL	P
65	GPIO36/P3LED2/ EN_PWRLIGHT	IO/LI/PU

No.	Pin Name	Type
66	GPIO39/P3LED0/DISAUOTL OAD	IO/LI/PU
67	GPIO40/P3LED1	IO/PU
68	GPIO41/P1LED2	IO/PU
69	GPIO42/P1LED0/MID29	IO/PU
70	GPIO43/P1LED1	IO/PU/OD
71	GPIO44/EN_PHY	IO/LI/PU
72	GPIO46/SMI_SEL	IO/LI/PU
73	AVDDH	AP
74	XTALO	XT
75	XTALI	XT
76	nRESET	I/PU
77	GND EPAD	G

2 Pin Description

2.1 MDI Interface Pins

Table 2 Transceiver Interface Pins

No.	Pin Name	Type	Description
4	P1MDIAP	AIO	Port 1 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
5	P1MDIAN	AIO	
6	P1MDIBP	AIO	Port 1 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
7	P1MDIBN	AIO	
9	P1MDICP	AIO	Port 1 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
10	P1MDICN	AIO	
11	P1MDIDP	AIO	Port 1 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
12	P1MDIDN	AIO	
15	P3MDIAP	AIO	Port 3 Media-dependent interface, differential pairs A, with 100Ω termination resistor.
16	P3MDIAN	AIO	
17	P3MDIBP	AIO	Port 3 Media-dependent interface, differential pairs B, with 100Ω termination resistor.
18	P3MDIBN	AIO	
20	P3MDICP	AIO	Port 3 Media-dependent interface, differential pairs C, with 100Ω termination resistor.
21	P3MDICN	AIO	
22	P3MDIDP	AIO	Port 3 Media-dependent interface, differential pairs D, with 100Ω termination resistor.
23	P3MDIDN	AIO	

2.2 RGMII Interface Pins

Table 3 RGMII Interface Pins

No.	Pin Name	Type	Description
47	RG2_TXCLK	O/LI/PD	<p>RGMII 2 Transmit Reference Clock will be 125MHz, 25MHz, or 2.5MHz depending on speed.</p> <ul style="list-style-type: none"> For Gigabit operation, the clocks will operate at 125MHz. For 10/100Mbps operation, the clocks will operate at 2.5MHz or 25MHz respectively. <p>TXCLK is an output pin in RGMII mode.</p>
46	RG2_TXCTL	O/PD	<p>RGMII 2 Transmit Control Signal from the MAC.</p> <p>TXCTL is an output pin in RGMII mode.</p>
42	RG2_TXD3	O/LI/PD	<p>RGMII 2 Transmit Data.</p> <p>Data is transmitted from MAC to PHY via TXD[3:0].</p> <p>TXD[3:0] are output pins in RGMII mode.</p>
43	RG2_TXD2	O/PU	
44	RG2_TXD1	O/PU	
45	RG2_TXD0	O/LI/PD	
48	RG2_RXCLK	I/PU	<p>RGMII 2 Continuous Receive Reference Clock will be 125MHz, 25MHz, or 2.5MHz, derived from the received data stream.</p> <p>RXCLK is an input pin in RGMII mode.</p>

No.	Pin Name	Type	Description
49	RG2_RXCTL	I/PU	RGMII 2 Receive Control Signal to the MAC. RXCTL is an input pin in RGMII mode.
53	RG2_RXD3	I/PU	RGMII 2 Receive Data. Data is transmitted from PHY to MAC via RXD[3:0]. RXD[3:0] are input pins in RGMII mode.
52	RG2_RXD2	I/PU	
51	RG2_RXD1	I/PU	
50	RG2_RXD0	I/PU	

2.3 MII Interface Pins

Table 4 MII Interface Pins

No.	Pin Name	Type	Description
47	M2_TXCLK/ P2_RXCLK	IO/LI/PD	<ul style="list-style-type: none"> M_TXCLK Pin in MII MAC Mode. MII Transmit Clock (input). Used to synchronize M_TXD[3:0], and M_TXEN. M_TXCLK is an input pin in MII MAC mode. P_RXCLK Pin in MII PHY Mode. MII Receive Clock (output). Used to synchronize P_RXD[3:0], and P_RXDV. P_RXCLK is an output pin in MII PHY mode. <p>The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te.</p>
46	M2_TXEN/ P2_RXDV	O/PD	<ul style="list-style-type: none"> M_TXEN Pin in MII MAC Mode. MII Transmit Enable. The synchronous output indicates that valid data is being driven on the M_TXD bus. M_TXEN synchronizes to M_TXCLK. P_RXDV Pin in MII PHY Mode. MII Receive Data Valid. This synchronous output is asserted when valid data is driven on the P_RXD bus. P_RXDV synchronizes to P_RXCLK. <p>M_TXEN/P_RXDV is an output pin in MII MAC mode/MII PHY mode.</p>
42	M2_TXD3/ P2_RXD3	O/LI/PD	<ul style="list-style-type: none"> M_TXD[3:0] Pin in MII MAC Mode. MII Transmit Data Bus. M_TXD[3:0] synchronize to M_TXCLK. P_RXD[3:0] Pin in MII PHY Mode. MII Receive Data Bus. P_RXD[3:0] synchronize to P_RXCLK. <p>M_TXD[3:0]/P_RXD[3:0] are output pins in MII MAC mode/MII PHY mode.</p>
43	M2_TXD2/ P2_RXD2	O/PU	
44	M2_TXD1/ P2_RXD1	O/PU	
45	M2_TXD0/ P2_RXD0	O/LI/PD	
48	M2_RXCLK/ P2_TXCLK	IO/PU	<ul style="list-style-type: none"> M_RXCLK Pin in MII MAC Mode. MII Receive Clock (input). Used to synchronize M_RXD[3:0], and M_RXDV.

No.	Pin Name	Type	Description
			<p>M_RXCLK is an input pin in MII MAC mode</p> <ul style="list-style-type: none"> P_TXCLK Pin in MII PHY Mode. <p>MII Transmit Clock (output). Used to synchronize P_TXD[3:0], and P_TXEN.</p> <p>P_TXCLK is an output pin in MII PHY mode.</p> <p>The frequency depends on the link speed, that is 25MHz at 100Base-TX, and 2.5MHz at 10Base-Te.</p>
49	M2_RXDV/ P2_TXEN	I/PU	<ul style="list-style-type: none"> M_RXDV Pin in MII MAC Mode. <p>MII Receive Data Valid. This synchronous input is asserted when valid data is driven on the M_RXD bus. M_RXDV synchronizes to M_RXCLK.</p> <ul style="list-style-type: none"> P_TXEN Pin in MII PHY Mode. <p>MII Transmit Enable. The synchronous input indicates that valid data is being driven on the P_TXD bus. P_TXEN synchronizes to P_TXCLK.</p> <p>M_RXDV/P_TXEN is an input pin in MII MAC mode/MII PHY mode.</p>
53	M2_RXD3/ P2_TXD3	I/PU	<ul style="list-style-type: none"> M_RXD[3:0] Pin in MII MAC Mode. <p>MII Receive Data Bus. M_RXD[3:0] synchronize to M_RXCLK.</p> <ul style="list-style-type: none"> P_TXD[3:0] Pin in MII PHY Mode. <p>MII Transmit Data Bus. P_TXD[3:0] synchronize to P_TXCLK.</p> <p>M_RXD[3:0]/P_TXD[3:0] are input pins in MII MAC mode/MII PHY mode.</p>
52	M2_RXD2/ P2_TXD2	I/PU	
51	M2_RXD1/ P2_TXD1	I/PU	
50	M2_RXD0/ P2_TXD0	I/PU	
41	M2_CRS	I/PD	<p>Carrier Sense Input in MII MAC mode when operating in 10/100M half-duplex modes.</p> <p>This pin should be pulled low with a 1kΩ resistor if not used.</p>

2.4 RMII Interface Pins

Table 5 RMII Interface Pins

No.	Pin Name	Type	Description
47	M2_TXCLK/ P2_RXCLK	IO/LI/PD	<p>REFCLK Pin in RMII Mode.</p> <ul style="list-style-type: none"> In RMII MAC Mode, REFCLK is an input pin. In RMII PHY Mode, REFCLK is an output pin. <p>REF_CLK is a 50MHz clock that provides the timing reference for RXDV, RXD[1:0], TXEN, TXD[1:0].</p>

No.	Pin Name	Type	Description
46	M2_TXEN/ P2_RXDV	O/PD	<ul style="list-style-type: none"> TXEN Pin in RMII MAC Mode. The synchronous output indicates that valid data is being driven on the TXD bus. TXEN synchronize to REFCLK. RXDV Pin in RMII PHY Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK. <p>M_TXEN/P_RXDV is an output pin in MII MAC mode/MII PHY mode.</p>
44	M2_TXD1/ P2_RXD1	O/PU	<ul style="list-style-type: none"> TXD[1:0] Pin in RMII MAC Mode, synchronize to REFCLK. RXD[1:0] Pin in RMII PHY Mode, synchronize to REFCLK. <p>M_TXD[1:0]/P_RXD[1:0] are output pins in MII MAC mode/MII PHY mode.</p>
45	M2_TXD0/ P2_RXD0	O/PD	
49	M2_RXDV/ P2_TXEN	I/PU	<ul style="list-style-type: none"> RXDV Pin in RMII MAC Mode. Carrier Sense/Receive Data Valid. This shall be asserted by the PHY when the receive medium is non-idle synchronized with REFCLK. TXEN Pin in RMII PHY Mode. The synchronous input indicates that valid data is being driven on the TXD bus. TXEN synchronize to REFCLK. <p>M_RXDV/P_TXEN is an input pin in MII MAC mode/MII PHY mode.</p>
51	M2_RXD1/ P2_TXD1	I/PU	<ul style="list-style-type: none"> RXD[1:0] Pin in RMII MAC Mode, synchronize to RXC. TXD[1:0] Pin in RMII PHY Mode, synchronize to TXC . <p>M_RXD[1:0]/P_TXD[1:0] are input pins in MII MAC mode/MII PHY mode.</p>
50	M2_RXD0/ P2_TXD0	I/PU	

2.5 High-Speed Serial Interface Pins

Table 6 High-Speed Serial Interface Pins

No.	Pin Name	Type	Description
32	HS0N	AO	High-Speed Serial Interface Pins: support 3.125Gbps or 1.25Gbps. Differential serial output interface.
33	HS0P	AO	
35	HS1P	AI	High-Speed Serial Interface Pins: support 3.125Gbps or 1.25Gbps. Differential serial input interface.
36	HS1N	AI	

2.6 Parallel LED Pins

Table 7 Parallel LED Pins

No.	Pin Name	Type	Description
30	P9LED0	IO/PU/OD	This pin can indicate P9LED0 by software configuration which means extra MAC LED0.
65	P3LED2	IO/LI/PU	Default port 3 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
67	P3LED1	IO/PU	Default port 3 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
66	P3LED0	IO/LI/PU	Default port 3 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM
68	P1LED2	IO/PU	Default port 1 Parallel LED LED2 Output Signal. The LED indicates information is defined by register or EEPROM
70	P1LED1	IO/PU/OD	Default port 1 Parallel LED LED1 Output Signal. The LED indicates information is defined by register or EEPROM
69	P1LED0	IO/LI/PU	Default port 1 Parallel LED LED0 Output Signal. The LED indicates information is defined by register or EEPROM

2.7 Management Interface Pins

Table 8 Management Interface Pins

No.	Pin Name	Type	Description
1	SCL/MDC	IO/PU/OD	EEPROM auto load mode serial clock output I2C slave mode serial clock input SMI slave mode serial clock input
2	SDA/MDIO	IO/PU/OD	EEPROM auto load mode serial data input I2C slave mode serial data SMI slave mode serial data

2.8 GPIO Pins

Table 9 GPIO Pins

No.	Pin Name	Type	Description
30	GPIO2	IO/PU/OD	General Purpose Input/Output Interfaces IO2.
41	GPIO4	IO/PD	General Purpose Input/Output Interfaces IO4.
42	GPIO6	IO/LI/PD	General Purpose Input/Output Interfaces IO6.
43	GPIO7	IO/PU	General Purpose Input/Output Interfaces IO7.
44	GPIO8	IO/PU	General Purpose Input/Output Interfaces IO8.
45	GPIO9	IO/LI/PD	General Purpose Input/Output Interfaces IO9.

No.	Pin Name	Type	Description
46	GPI010	IO/PD	General Purpose Input/Output Interfaces IO10.
47	GPI011	IO/LI/PD	General Purpose Input/Output Interfaces IO11.
48	GPI012	IO/PU	General Purpose Input/Output Interfaces IO12.
49	GPI013	IO/PU	General Purpose Input/Output Interfaces IO13
50	GPI014	IO/PU	General Purpose Input/Output Interfaces IO14.
51	GPI015	IO/PU	General Purpose Input/Output Interfaces IO15.
52	GPI016	IO/PU	General Purpose Input/Output Interfaces IO16.
53	GPI017	IO/PU	General Purpose Input/Output Interfaces IO17.
65	GPI036	IO/LI/PU	General Purpose Input/Output Interfaces IO36.
66	GPI039	IO/LI/PU	General Purpose Input/Output Interfaces IO39.
67	GPI040	IO/PU	General Purpose Input/Output Interfaces IO40.
68	GPI041	IO/PU	General Purpose Input/Output Interfaces IO41.
69	GPI042	IO/PU	General Purpose Input/Output Interfaces IO42.
70	GPI043	IO/PU/OD	General Purpose Input/Output Interfaces IO43.
71	GPI044	IO/LI/PU	General Purpose Input/Output Interfaces IO44.
72	GPI046	IO/LI/PU	General Purpose Input/Output Interfaces IO46.
1	GPI048	IO/PU/OD	General Purpose Input/Output Interfaces IO48.
2	GPI049	IO/PU/OD	General Purpose Input/Output Interfaces IO49.

2.9 Configuration Pins

Table 10 Configuration Pins

No.	Pin Name	Type	Description
42	SWITCH_ID_1	IO/LI/PD	Switch_ID[1:0] for slave SMI and slave I2C format.
47	SWITCH_ID_0	IO/LI/PD	
55	EN_SWR	AI	Disable/Enable internal switching regulator. <ul style="list-style-type: none"> ● Pull Down: Disable SWR ● Pull Up: Enable SWR
65	EN_PWRLIGHT	IO/LI/PU	Disable/Enable LED function when powered on. <ul style="list-style-type: none"> ● Pull Up: Enable LED ● Pull Down: Disable LED.
66	DISAUTOLOAD	IO/LI/PU	Disable EEPROM Autoload. <ul style="list-style-type: none"> ● Pull Up: Disable EEPROM autoload upon power on or reset ● Pull Down: Enable EEPROM autoload upon power on or reset
69	MID29	IO/PU	Slave SMI (MDC/MDIO) Device Address. <ul style="list-style-type: none"> ● Pull Up: Slave SMI (MDC/MDIO) Device Address is 0x1d ● Pull Down: Slave SMI (MDC/MDIO) Device Address is 0x0
71	EN_PHY	IO/LI/PU	Enable Embedded PHY.

No.	Pin Name	Type	Description
			<ul style="list-style-type: none"> Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY
72	SMI_SEL	IO/LI/PU	Management Interface Selection. <ul style="list-style-type: none"> Pull Up: Slave I2C interface Pull Down: Slave MDIO interface
43	RESERVED_0	-	Reserved. This pin must be pulled high via an external 4.7kΩ resistor to DVDDIO_2 upon power on.
44	RESERVED_1	-	Reserved. This pin must be pulled high via an external 4.7kΩ resistor to DVDDIO_2 upon power on.
46	RESERVED_2	-	Reserved. This pin must be pulled high via an external 4.7kΩ resistor to DVDDIO_2 upon power on.

2.10 Power Related Pins

Table 11 Power Related Pins

No.	Pin Name	Type	Description
63	DVDDIO	P	Digital power 2.5V/3.3V Note: When DVDDIO uses 2.5V, its external interface must also support the corresponding voltage.
40, 54	DVDDIO_2	P	Digital power 1.8V/2.5V/3.3V for extension port Note: When DVDDIO_2 uses 1.8V/2.5V, its external interface must also support the corresponding voltage.
31, 39, 64	DVDDL	P	Digital power 1.1V
3, 14, 24, 29, 73	AVDDH	AP	Analog power 3.3V
8, 19, 27	AVDDL	AP	Analog power 1.1V
37	SVDDH	AP	SerDes power 3.3V
34	SVDDL	AP	SerDes power 1.1V for group 0.
13	PLLVDDL	AP	PLL Power 1.1V.
25	AGND	AG	Analog GND.
77	GND EPAD	G	GND

2.11 Clock Pins

Table 12 Clock Pins

No.	Pin Name	Type	Description
75	XTAL_I	XT	25MHz Crystal Input pin. If use external oscillator or clock from another device. <ul style="list-style-type: none"> When connect an external 25MHz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND.

No.	Pin Name	Type	Description
			<ul style="list-style-type: none"> When connect an external 25MHz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.
74	XTAL_O	XT	25MHz Crystal Output pin. If use external oscillator or clock from another device. <ul style="list-style-type: none"> When connect an external 25MHz oscillator or clock from another device to XTAL_O pin, XTAL_I must be shorted to GND. When connect an external 25MHz oscillator or clock from another device to XTAL_I pin, keep the XTAL_O floating.

2.12 Reset Pins

Table 13 Reset Pins

No.	Pin Name	Type	Description
76	nRESET	I/PU	Hardware reset, active low. Requires an external pull-up resistor.

2.13 Miscellaneous Pins

Table 14 Miscellaneous Pins

No.	Pin Name	Type	Description
26	RBIAS	AO	Bias Resistor. An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND.
28, 38	NC	-	Not connect. Must be left floating in normal operation.

3 Integrated PHY Functional

YT9213NB integrates two 10/100/1000M Giga PHY ports. Each PHY port supports 1000Base-T, 100Base-TX, and 10Base-Te by four signal pairs (MDIAP/N, MDIBP/N, MDICP/N and MDIDP/N). Each signal pair consists of two bi-directional pins that can transmit and receive at the same time.

- For 1000Base-T, all four pairs are used in both directions at the same time.
- For 100Base-TX and 10Base-Te, only MDIAP/N and MDIBP/N are used.

3.1 Transmit Encoder Modes

3.1.1 1000BASE-T

In 1000BASE-T mode, the PHY port scrambles data bytes to be transmitted from the MAC interfaces to 9-bit symbols and encodes them into 4D five-level PAM signals over the four pairs of CAT5E UTP cable.

3.1.2 100BASE-TX

In 100BASE-TX mode, 4-bit data from the MII is 4B/5B serialized, scrambled, and encoded to a three-level MLT3 sequence transmitted by the PMA.

3.1.3 10BASE-Te

In 10BASE-Te mode, the PHY port transmits Manchester-encoded data.

3.2 Receive Decoder Modes

3.2.1 1000BASE-T

In 1000BASE-T mode, the PMA recovers the 4D PAM signals after accounting for the cabling conditions such as skew among the four pairs, the pair swap order, and the polarity of the pairs. The resulting code group is decoded into 8-bit data values. Data stream delimiters are translated appropriately, and data is output to the MAC interfaces.

3.2.2 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and descrambled to align to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded to 4-bit data. This output runs to MAC interfaces after data stream delimiters have been translated.

3.2.3 10BASE-Te

In 10BASE-Te mode, the recovered 10BASE-Te signal is decoded from Manchester then aligned.

3.3 Echo Cancellor

A hybrid circuit is used to transmit and receive simultaneously on each pair. A signal reflects as an echo if the transmitter is not perfectly matched to the line. Other connector or cable imperfections, such as

patch panel discontinuity and variations in cable impedance along the twisted pair cable, also lead to drastic SNR degradation on the receive signal. The PHY port implements a digital echo canceller to adjust for echo and is adaptive to compensate for the varied channel conditions.

3.4 NEXT Cancellor

The 1000BASE-T physical layer uses all four pairs of wires to transmit data. Because the four twisted pairs are bundled, significant high-frequency crosstalk occurs between adjacent pairs in the bundle. The PHY port uses three parallel NEXT cancellers on each receive channel to cancel high frequency crosstalk. The PHY port cancels NEXT by subtracting an estimate of these signals from the equalizer output.

3.5 Baseline Wander Cancellor

Baseline wander results from Ethernet links that AC coupling to the transceivers, and AC coupling cannot maintain voltage levels for a long time. Baseline wander distorts the transmitted pulse, which in turn affects the sampling value of the pulse. Baseline wander is more susceptible in the 1000BASE-T environment than in 100BASE-TX due to the DC baseline shift in the transmit and receive signals.

The YT9213NB device uses an advanced baseline wander cancellation circuit that continuously monitors and compensates for this effect, minimizing the impact of DC baseline shift on the overall error rate.

3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver and takes signals from ADC output. It uses a combination of FFE (Feedforward Equalizer) and DFE (Decision Feedback Equalizer) for the best-optimized SNR (Signal-to-Noise Ratio) ratio.

3.7 Auto-Negotiation

The integrated PHY port negotiates its operation mode using the auto-negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto-negotiation supports choosing the mode of operation automatically by comparing the abilities of itself and its link partner.

Auto-negotiation is enabled for YT9213NB by default and can be disabled by software control.

3.8 Auto Crossover and Polarity Correction

The integrated PHY port can detect and correct two types of cable errors:

- Auto crossover of pairs within the UTP cable (between pair 0 and pair 1, and(or) between pair 2 and pair 3)
- Swapping of polarity within a pair.

4 General Function

4.1 Reset

4.1.1 Hardware Reset

YT9213NB has a hardware reset pin (nRESET) which is low active. The reset signal should be active for at least 10ms. Hardware reset should be applied after power on correctly.

After the reset is released, YT9213NB will start the reset initialization procedures by the following steps:

- 1 Reset All internal logic to a known state, and reset all registers to default value.
- 2 Latch input value on configuration pins which are used as configuration information to provide flexible applications.
- 3 Complete the memory BIST process and initialize the packet buffer.
- 4 Autoload from the EEPROM, or boot from Flash or EEPROM by internal CPU if needed.

4.1.2 Software Reset

YT9213NB supports two software resets that can be triggered by programming switch global control register: a chip reset (CHIP_RESET, bit 31 of register 0x8_0000) and a software reset (SW_RESET, bit 1 of register 0x8_0000).

4.1.2.1 CHIP_RESET

The CHIP_RESET is set to 1 to take effect and self-clear. The chip will obey the following steps:

- 1 Reset all the digital and analog circuits to default.
- 2 Reinitialize the packet buffer and clear all the lookup and VLAN tables.
- 3 Autoload from the EEPROM, or boot from Flash or EEPROM by internal CPU if needed, and the chip will be configured again.
- 4 The integrated PHYs will restart the auto-negotiation process.

4.1.2.2 SW_RESET

The SW_RESET is also set to 1 to take effect and self-clear, and its function is similar to the CHIP_RESET except the analog circuit of integrated PHYs will not be reset.

4.2 Flexible Applications by Configuration Pins

According to the system application, user can select the most suitable mode by configuration pins DISAUTOLOAD and SMI_SEL, shown in the following table.

Table 15 Flexible Applications

DISAUTOLOAD	SMI_SEL	Initial Stage Loading Data*	
		From	To
0	1	EEPROM	RAM

Note*: Initial Stage means power on, hardware reset, or software reset.

4.3 IEEE 802.3x Full Duplex Flow Control

YT9213NB supports IEEE 802.3x flow control in 10/100/1000M full duplex modes. The result of Auto-Negotiation or software configuration can decide the flow control ability.

In most cases, MAC ports with integrated PHY get flow control ability by Auto-Negotiation and two extra MAC ports with MII/RMII/RGMII by software configuration.

4.4 Half Duplex Flow Control

When the PHY port works as 10/100M half-duplex modes, it will collide with the link partner when transmitting and receiving data. Then this will make the buffer overflow and drop packets. YT9213NB supports two methods (jam mode and defer mode) to avoid this.

The maximum retry count limitation is 16 which follows the definition in IEEE 802.3. But for YT9213NB, the retry count limitation is configurable and will not drop packet by default.

4.5 FDB Table

4.5.1 Lookup and Forward

YT9213NB MAC address table consists of a 4K-entry FDB table. On receiving a packet, YT9213NB uses DA, FID to search the 4K-entry FDB table.

- If an entry is matched, the received packet will be forwarded to the corresponding destination port.
- If no entry is matched, YT9213NB floods the packet according to the VLAN configuration.

4.5.2 MAC Address Learning

YT9213NB uses the source MAC address and FID to search the 4K-entry FDB table when a packet is received.

- If there is a match with one of the entries, YT9213NB will update the entry with new information.
- If there is no matching entry, the packet information is learned into the entry.

4.5.3 MAC Address Aging

The aging mechanism of MAC address is as follows:

When a packet flow reaches a port, the port learns the MAC address dynamically.

- If the port keeps receiving this packet flow, the corresponding MAC address is updated continuously and will not be aged.
- If the packet flow stops, the MAC address is deleted after the aging time. The aging time of YT9213NB is between 5 and 327,675 seconds (the typical value 300 seconds).

4.6 IVL SVL and IVL/SVL

YT9213NB supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (Both Independent and Shared VLAN Learning).

4.7 Reserved Multicast Address

YT9213NB supports drop/forward/copy IEEE 802.3 specified reserved multicast MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting for these reserved multicast MAC addresses is forwarding. Frames with multicast MAC address 01-80-C2-00-00-01 (802.3x Pause) will always be dropped.

4.8 Storm Control

YT9213NB supports storm control for broadcast, multicast and unknown DA, each storm type can be enabled/disabled per-port, default is disabled. If the RX rate of these type of packets exceeds configured rate, all following storm packets will be dropped. The rate can be configured with packet mode (pps) or byte mode (bps).

4.9 Port Security

YT9213NB supports the following security mechanism to prevent malicious attacks:

- Per-port enable/disable SA auto-learning
- Per-port enable/disable FDB aging update
- Per-port enable/disable unknown DA packet drop

4.10 MIB

YT9213NB supports the following MIB standards for common management:

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

4.11 Port Mirror

YT9213NB supports 1 group of port mirrors for all ports. The TX/RX or both direction packets from each port can be mirrored to the monitor port.

4.12 VLAN Function

YT9213NB supports a 4K VLAN table, can be configured as port-based VLAN, IEEE 802.1Q tag-based VLAN, Protocol-based VLAN, and also supports the IVC (VLAN Translate) function. Ingress-filtering, egress-filtering, and accept-frame-type options provide flexible VLAN configuration:

- Ingress Filtering: Packets from an input port not in the VLAN member will be dropped.
- Egress Filtering: Packets to an output port not in the VLAN member will be dropped.

- Accept Frame Type: The input port can be configured as “Accept All”, “Accept Tagged”, “Accept Untagged”, and “Drop All”.

The packets at the output port can be inserted or removed VLAN tag. For untagged packets, YT9213NB can insert a VLAN TAG or remove the VLAN TAG from tagged frames.

4.12.1 Port-Based VLAN

The 4K-entry VLAN Table designed into YT9213NB provides full flexibility for users to configure the input ports to associate with different VLAN entries. Each input port can join with more than one VLAN entry.

Port-based VLAN mapping is the simplest and most effective mapping rule. It defines VLAN members based on device ports. All the packets received from a given input port will be forwarded to this port’s VLAN members.

4.12.2 IEEE 802.1Q Tag-Based VLAN

In 802.1Q VLAN mapping, the device uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. YT9213NB compares the VID in the VLAN tag with the 4K VLAN Table to determine the packet forwarding action.

4.12.3 Port VID

YT9213NB supports Port VID (PVID) for each port. When an untagged or priority-tagged packet is forwarded to the output port without hitting other assigned vid rules and the egress tag mode set tagged, the device supports inserting a PVID in the VLAN tag.

4.13 QoS Function

YT9213NB supports 8 unicast priority queues, 4 multicast priority queues, and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1Q Tag-based priority, VLAN entry-based priority, MAC SA-based priority, MAC DA-based priority, DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in YT9213NB, the packet’s priority will be assigned based on the priority selection table.

Per-queue in each output port can be set as Strict Priority (SP) or Deficit Weighted Round Robin (DWRR) for the packet scheduling algorithm.

4.13.1 Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic exceeds the RX Bandwidth parameter, if flow control is enabled, this port will send out a “pause ON” frame; if flow control is disabled, it will drop the input packet. Per-port input bandwidth control rates can be set from 9Kbps to 2.5Gbps (in 9Kbps steps).

4.13.2 Priority Assignment

Priority assignment specifies the priority of a received packet based on various rules. YT9213NB can recognize the QoS priority information of receiving packets to give a different service priority.

YT9213NB identifies the priority of packets based on seven types of QoS priority information:

- Port-based priority
- 802.1Q-based priority
- DSCP-based priority
- ACL-based priority
- VLAN entry-based priority
- MAC SA-based priority
- MAC DA-based priority

4.13.3 Priority Queue Scheduling

The packet scheduler controls the various traffics (control packets sending a sequence of the priority queue), YT9213NB scheduling algorithm is Deficit Weighted Round Robin (DWRR). DWRR supports byte-based or packet-based.

In addition, each queue of each port can select Strict Priority or DWRR packet scheduling, and DWRR can co-exist with the SP schedule.

4.13.4 IEEE 802.1Q and DSCP Remarking

YT9213NB supports the IEEE 802.1Q and DSCP remarking functions. If the remarking function is enabled, when packets egress from one of the 12 queues, the packet's 802.1Q priority and DSCP can be remarked to a configured value. 802.1Q priority & DSCP value can be remarked based on internal priority.

4.14 IGMP & MLD Snooping Function

YT9213NB supports hardware IGMPv1/v2/v3 snooping and MLDv1/v2 snooping. These multicast groups are learned and deleted/aged out automatically. For data packets of a known multicast group, YT9213NB forwards them according to the learned group membership.

YT9213NB supports bypassing designated IP multicast address with global control and per ingress port join/leave packets allowed control.

YT9213NB supports IGMP Dynamic Router Port Learning, dynamic router port enable control is based on per-port basis. The aging time can be configured by SW, the router port will be removed when timeout.

YT9213NB supports IGMP/MLD Hardware Fast Leave, when left, the multicast group will be marked as invalid again.

YT9213NB supports IGMP/MLD Packet Copy/Trap/Flood based on global control.

4.15 IEEE 802.1x Function

YT9213NB supports IEEE 802.1x Port-Based.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port

- Guest VLAN

4.15.1 Port-Based Access Control

Each port of YT9213NB can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

4.15.2 Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, its port authorization status can be set to authorized.

4.15.3 Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when the port authorization direction is "BOTH". If the authorization direction of an 802.1X unauthorized port is "IN", incoming frames to that port will be dropped, but outgoing frames will be transmitted.

4.15.4 Guest VLAN

When YT9213NB enables the Port-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, YT9213NB will drop all packets from this port. If configuring Guest VLAN, YT9213NB will allow packets from unauthorized ports to be forwarded to a limited VLAN domain.

4.16 Spanning Tree

IEEE 802.1D Spanning Tree allows bridges to prevent and resolve Layer 2 forwarding loops automatically. Switches exchange BPDUs and configuration messages and selectively enable and disable forwarding on specified ports. YT9213NB supports 16 STP instances and four statuses (Disabled/Blocking/Learning /Forwarding) for each port when the CPU implements the STP/RSTP/MSTP function.

4.17 Embedded RISC-V

A RISC-V MCU is embedded in YT9213NB to support software management/protocol functions. The RISC-V MCU can transmit to or receive frames from the switch core. The features of the RISC-V MCU are listed below:

- On-chip 64K SRAM
- On-chip 16K boot ROM
- 2K I-Cache
- Up to 8M-Byte serial I/O, dual I/O SPI Flash supported

4.18 Cable Status Diagnostic

Physical layer transceivers of YT9213NB support Motorcomm's Advanced Cable Status Diagnostic (CSD) feature. Some of the possible problems that can be diagnosed in each differential pair. The result of CSD is summarized as normal, open, and short.

4.19 LED Indicators

The YT9213NB supports parallel LEDs for each port. Each PHY port has three LED indicator pins, LED0, LED1, and LED2. Each LED of each port may have different indicator information defined in [Table 16](#). LED0 default indicates Link/Act, LED1 default indicates 1000M_Link, and LED2 default indicates 100M_Link.

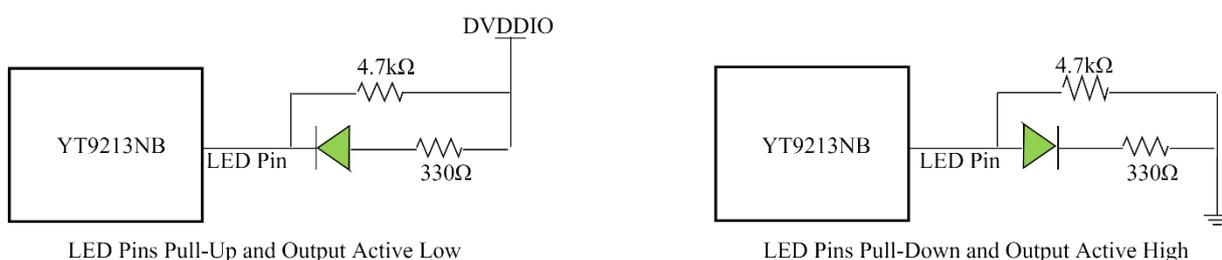
YT9213NB supports the power-on-blinking feature by the EN_PWRLIGHT pin and software configuration. The LEDs will blink once after reset.

Table 16 LED Definitions

LED Definition	Description
Full	Full Duplex Indicator. LED on when the corresponding port links at full duplex.
Half	Half Duplex Indicator. LED on when the corresponding port links at half duplex.
Link	Link Indicator. LED on when the corresponding port links up.
1000M_Link	1000Mbps Link Indicator. LED on when the corresponding port links at 1000Mbps.
100M_Link	100Mbps Link Indicator. LED on when the corresponding port links at 100Mbps.
10M_Link	10Mbps Link Indicator. LED on when the corresponding port links at 10Mbps.
Act	Activity Indicator. LED blinks when the corresponding port is transmitting or receiving.
1000M_Act	1000Mbps Activity Indicator. LED blinks when the corresponding port links at 1000Mbps and is transmitting or receiving.
100M_Act	100Mbps Activity Indicator. LED blinks when the corresponding port links at 100Mbps and is transmitting or receiving.
10M_Act	10Mbps Activity Indicator. LED blinks when the corresponding port links at 10Mbps and is transmitting or receiving.
TX_Act	TX Activity Indicator. LED blinks when the corresponding port is transmitting.
RX_Act	RX Activity Indicator. LED blinks when the corresponding port is received.
EEE_Act	EEE Mode Indicator. LED blinks when the corresponding port enters EEE mode.
Loop_Act	Loop Detection Indicator. LED blinks when the corresponding port detects a loop.

LED signals are active low by default. The LED pins also support hardware configuration functions, so they are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. When the pin input is pulled high upon reset, the pin output is active low for LED function after reset. When the pin input is pulled down upon reset, the pin output is active high for LED function after reset. Typical values for pull-up/pull-down resistors are 4.7k Ω .

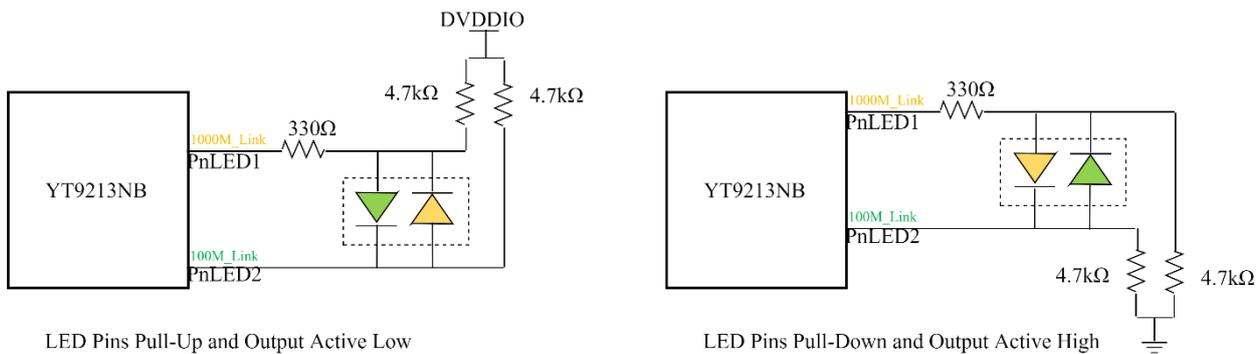
Figure 3 Pull-Up and Pull-Down of LED Pins



The LED Pins can also support Bi-color LED applications. Both LED pins connected to the Bi-color LED should have the same polarity active, and the LED definition of both will not appear at the same time.

For example, refer to [Figure 4](#) PnLED1 and PnLED2 will be Pull-Up or Pull-Down together. The PnLED1 definition is 1000M_Link. Nevertheless, the PnLED2 definition is 100M_Link. PnLED1 and PnLED2 will not be ON at the same time.

Figure 4 Typical Application for Bi-color LED



4.20 Link Down Power Saving (Sleep Mode)

Physical layer transceivers of YT9213NB support link-down power saving, also called sleep mode. When the UTP port link down and no signals over the UTP cable for 40 seconds, Physical layer transceivers will enter sleep mode. In this mode, some circuits of physical layer transceivers will be disabled, and the power consumption of the whole chip will be lower.

Once detected signals are over the UTP cable, the physical layer transceiver will exit sleep mode to normal mode.

4.21 Energy Efficient Ethernet

YT9213NB supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation.

IEEE 802.3az is an extension of the IEEE 802.3 standard. It defines the PHY transceivers to operate in Low Power Idle (LPI) mode which supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY transceiver's circuitry and save power consumption.

When Low Power Idle mode is enabled by MAC and PHY, the YT9213NB MAC uses Low Power Idle signaling to indicate to the PHY that a period of idle in the data stream is expected. Both local and link partner PHY transceivers may use this information to enter power-saving modes.

4.22 Interrupt Pin for External CPU

YT9213NB provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with the mask.

When the port link-up or link-down interrupt mask is enabled, the YT9213NB will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

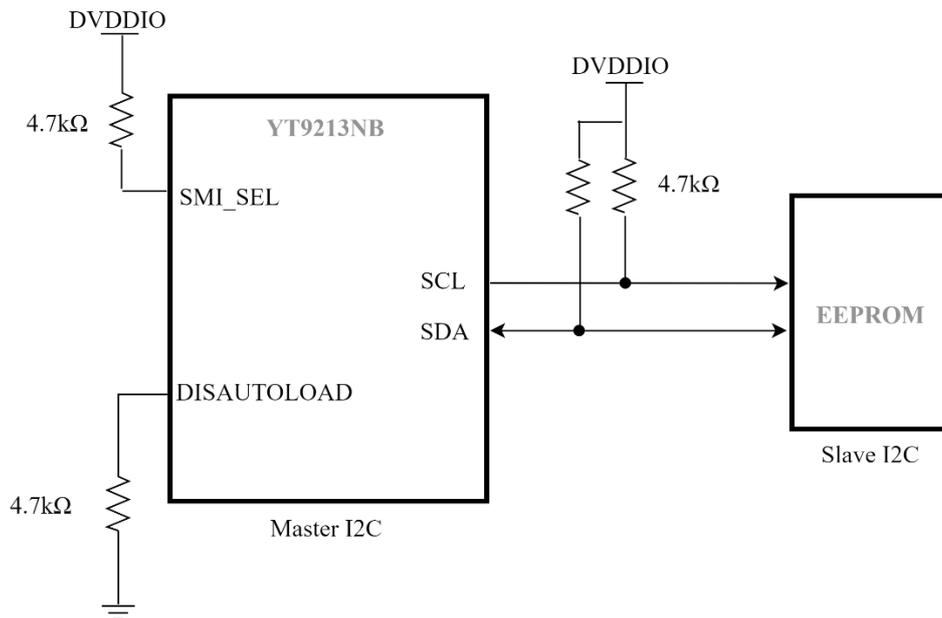
5 Interface Descriptions

5.1 Master I2C Interface for EEPROM Auto-load

The EEPROM auto-load interface of the YT9213NB uses the serial bus I2C to read the Serial EEPROM. After YT9213NB power on or reset, it drives SCL and SDA to read the data from the EEPROM by configuration pins.

As shown in the following figure, Pull-Up resistors, for example, 4.7kΩ should be connected to SCL and SDA signals.

Figure 5 Auto-load From EEPROM To RAM

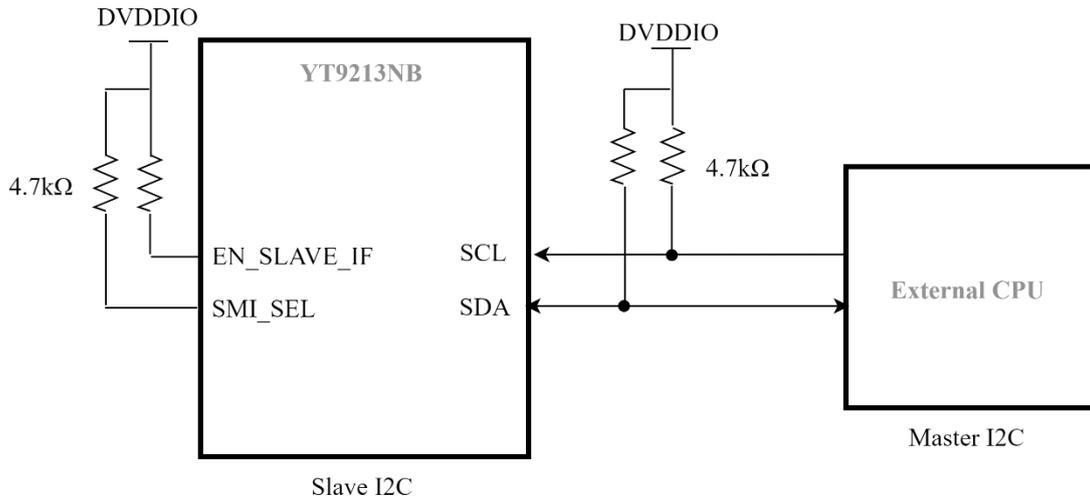


YT9213NB only supports 2 bytes word address mode EEPROM, that size should be 32Kbit~512Kbit.

5.2 Management Interfaces

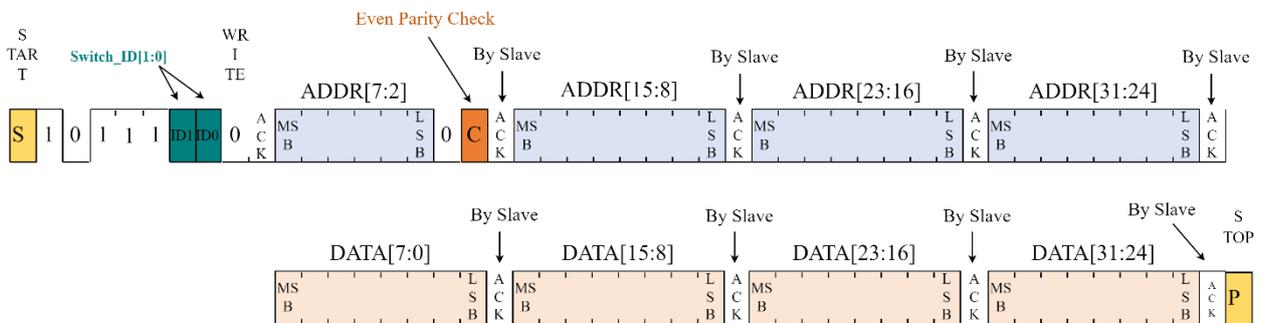
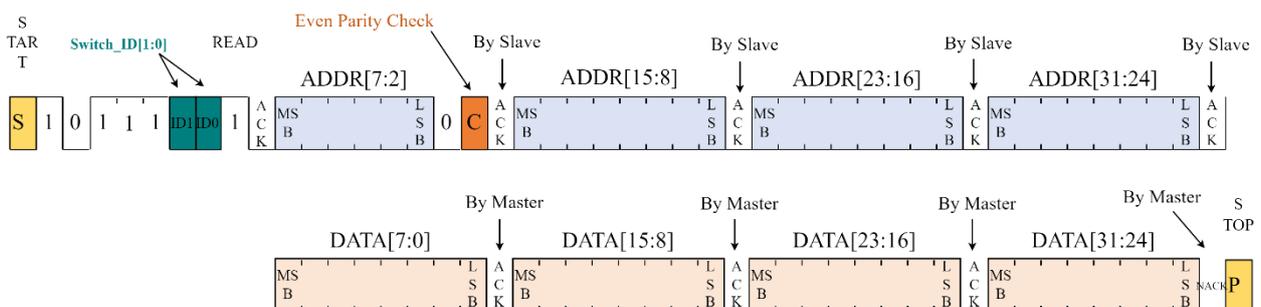
5.2.1 Slave I2C Interface for External CPU

YT9213NB registers can be accessed via slave I2C interfaces (SCK and SDA) by an external CPU. The configuration pins EN_SLAVE_IF and SMI_SEL should be high up on power on or reset, to select slave I2C interface.

Figure 6 Slave I2C Interface Connection Example


The slave I2C format is derived from the standard I2C, as shown in the following diagram. Switch_ID [1:0] comes from the configuration pins SWITCH_ID_1 and SWITCH_ID_0. P stands for the even parity check of ADDR[31:2].

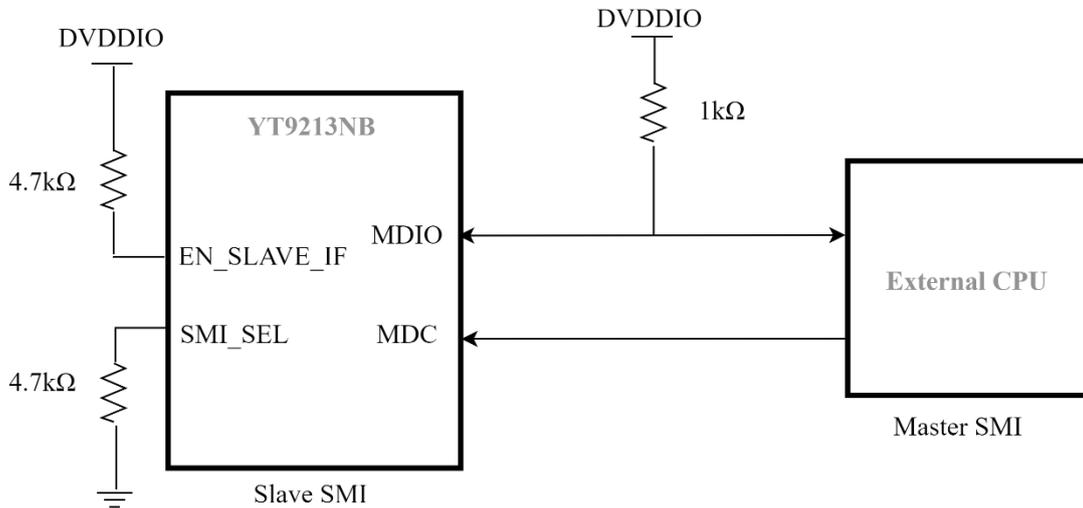
- P = 0, if there is an even number of "1" in ADDR [31:2].
- P = 1, if there is an odd number of "1" in ADDR [31:2].

Figure 7 External CPU Write Register into YT9213NB By Slave I2C

Figure 8 External CPU Read Register from YT9213NB By Slave I2C


5.2.2 Slave SMI Interface for External CPU

If the SMI_SEL is low or high upon power on or reset, the slave SMI (MDC/MDIO) is selected to access YT9213NB registers.

Figure 9 External CPU Read Register from YT9213NB By Slave SMI



5.3 General Purpose Interface

YT9213NB supports two extension interfaces. The two Extension GMAC (GMAC1 and GMAC2) both support RGMII mode, MII MAC mode, MII PHY mode, RMII MAC mode, and RMII PHY mode. The Extension GMAC2 also supports SGMII MAC mode, SGMII PHY mode, 2500Base-X mode, 1000Base-X mode, and 100Base-FX mode. All modes can be configured by register.

5.3.1 Extension Ports SGMII MAC/PHY Mode (10/100/1000Mbps)

The Extension GMAC2 supports SGMII MAC/PHY interfaces to an external CPU.

5.3.2 Extension Ports Fiber Mode (100FX/1000BX/2500BX)

The Extension GMAC2 supports Fiber (100FX/1000BX/2500BX) interfaces to an external CPU or optical module.

5.3.3 Extension Ports RGMII Mode (10/100/1000Mbps)

The two Extension GMAC (GMAC1 and GMAC2) both support single-port RGMII interfaces to an external CPU.

5.3.4 Extension Ports MII MAC/PHY Mode Interface (10/100Mbps)

The two Extension GMAC (GMAC1 and GMAC2) both support MII MAC/PHY mode interfaces to an external CPU.

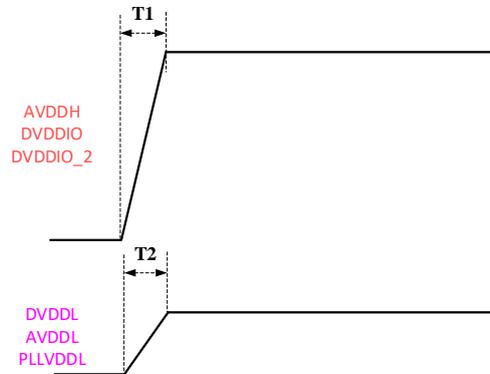
5.3.5 Extension Ports RMII MAC/PHY Mode Interface (10/100Mbps)

The two Extension GMAC (GMAC1 and GMAC2) both support RMII MAC/PHY mode interfaces to an external CPU.

6 Power Requirements

6.1 Power Sequence

Figure 10 Power Sequence Diagram



Power Sequence Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
T1	The rising time of AVDDH, DVDDIO, DVDDIO_2.	0.5	-	-	ms
T2	The rising time of DVDDL, AVDDL, PLLVDDL.	0.5	-	-	ms

6.2 Power Consumption

YT9213NB Power Consumption

Condition	AVDDH + SVDDH+DVDDIO + DVDDIO_2 (3.3V, mA)	DVDDL + AVDDL +SVDDL+ PLLVDDL (1.15V, mA)	Power Consumption (mW)
Link Down	77	107	372
2 UTP Link Up @1000Mbps	134	264	733
2 UTP Traffic @1000Mbps	133	295	763
2 UTP + 2 RGMII Link Up @1000Mbps	149	272	791
2 UTP + 2 RGMII Traffic @1000Mbps	163	315	884
2 UTP + 1 RGMII + 1 Serdes (2.5G) Traffic @1000Mbps	171	373	975

Test Condition: Port 1 and Port 3 work as 1000BT. TT IC with AVDDH/DVDDIO/DVDDIO_2 = 3.3V and DVDDL/AVDDL/PLLVDDL = 1.15V at room temperature.

6.3 Power Ripple

The AVDDH/DVDDIO/DVDDIO_2 supply ripple should be under 100mV. The DVDDL ripple should be under 80mV, and the AVDDL and PLLVDDL ripple should be under 50mV.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 17 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Junction Temperature (T_j)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO, DVDDIO_2, AVDDH, SVDDH, Supply Referenced to GND and AGND	GND-0.3	+3.70	V
DVDDL, AVDDL, PLLVDDL, SVDDL, Supply Referenced to GND, AGND and PLLGND	GND-0.3	+1.40	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

7.2 Recommended Operating Range

Table 18 Recommended Operating Range

Parameter	Min	Typ	Max	Unit	
Ambient Operating Temperature (T_a)	0	-	70	°C	
DVDDIO, AVDDH, SVDDH Supply Voltage Range	3.135	3.3	3.63	V	
DVDDIO_2 Supply Voltage Range (DVDDIO_2: Extension Port 2 Supports 1.8V, 2.5V, 3.3V)	3.3V	3.135	3.3	3.63	V
	2.5V	2.25	2.5	2.75	V
	1.8V	1.620	1.8	1.98	V
DVDDL, AVDDL, PLLVDDL, SVDDL, Supply Voltage Range	1.08	1.15	1.32	V	

7.3 DC Characteristics

Table 19 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VOH (3.3V)	Minimum High-Level Output Voltage	2.4	-	3.63	V
VOL (3.3V)	Maximum Low-Level Output Voltage	-0.3	-	0.4	V
VIH (3.3V)	Minimum High-Level Input Voltage	2	-	-	V
VIL (3.3V)	Maximum Low-Level Input Voltage	-	-	0.8	V
VOH (2.5V)	Minimum High Level Output Voltage	2	-	2.8	V
VOL (2.5V)	Maximum Low-Level Output Voltage	-0.3	-	0.4	V
VIH (2.5V)	Minimum High-Level Input Voltage	1.7	-	-	V
VIL (2.5V)	Maximum Low-Level Input Voltage	-	-	0.7	V
VOH (1.8V)	Minimum High-Level Output Voltage	1.62	-	2.1	V
VOL (1.8V)	Maximum Low-Level Output Voltage	-0.3	-	0.4	V
VIH (1.8V)	Minimum High-Level Input Voltage	1.2	-	-	V

Symbol	Parameter	Min	Typ	Max	Unit
VIL (1.8V)	Maximum Low-Level Input Voltage	-	-	0.5	V

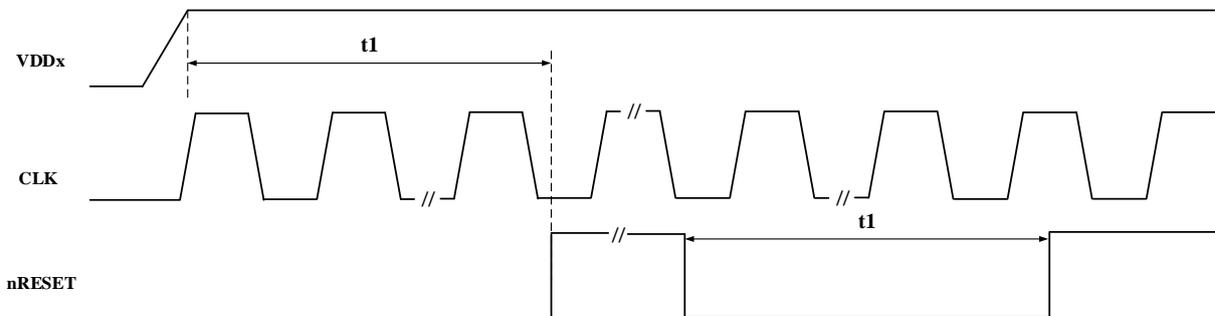
7.4 AC Characteristics

7.4.1 Reset Timing

Table 20 Reset Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
t1	The time from all powers steady to nRESET de-asserted, or the nRESET assertion time after power up.	10	-	-	ms

Figure 11 Reset Timing Diagram



7.4.2 SPI Flash Interface Timing Characteristics

Figure 12 SPI Flash Interface Timing

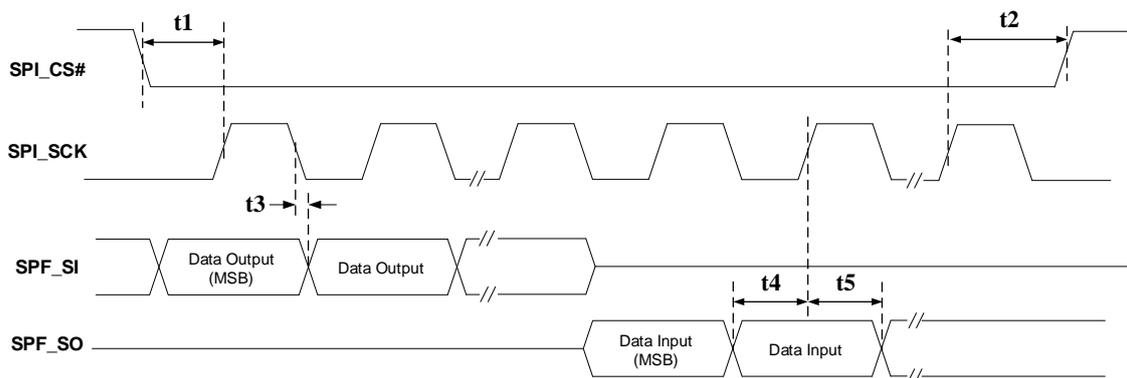


Table 21 SPI Flash Interface Timing Parameter

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Clock Frequency of SPI_SCK	-	31.25	-	MHz
t1	SPI_CS# Active Setup Time relative to SPI_SCK	20	-	-	ns

t2	SPI_CS# Not Active Hold Time relative to SPI_SCK	80	-	-	ns
t3	SPI_SI Output Valid Time	0	-	15	ns
t4	SPI_SO Input Setup Time	2	-	-	ns
t5	SPI_SO Input Hold Time	0	-	-	ns

7.4.3 Master I2C for EEPROM Auto-load Timing Characteristics

Figure 13 Master I2C for EEPROM Auto-load Timing

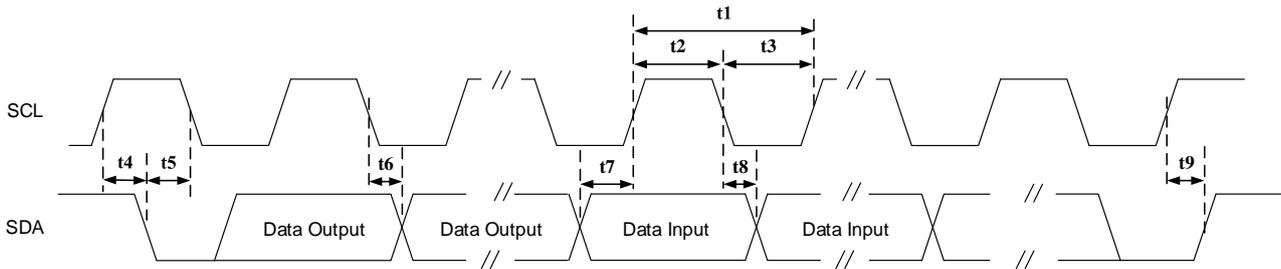


Table 22 Master I2C for EEPROM Auto-load Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
Tfreq	SCL Clock Frequency	-	100	800	kHz
t1	SCL Clock Period	1.25	10	-	μ s
t2	SCL High Time	$0.3*t1$	$0.5*t1$	-	μ s
t3	SCL Low Time	$0.3*t1$	$0.5*t1$	-	μ s
t4	START Setup Time	$0.25*t1$	-	-	μ s
t5	START Hold Time	$0.25*t1$	-	-	μ s
t6	SCL Low to Data Output Valid	$0.1*t1$	-	$0.2*t1$	μ s
t7	Data Input Setup Time	0	-	-	ns
t8	Data Input Hold Time	0	-	-	ns
t9	Stop Setup Time	$0.3*t1$	-	-	μ s

7.4.4 Slave I2C Timing Characteristics

Figure 14 Slave I2C Timing

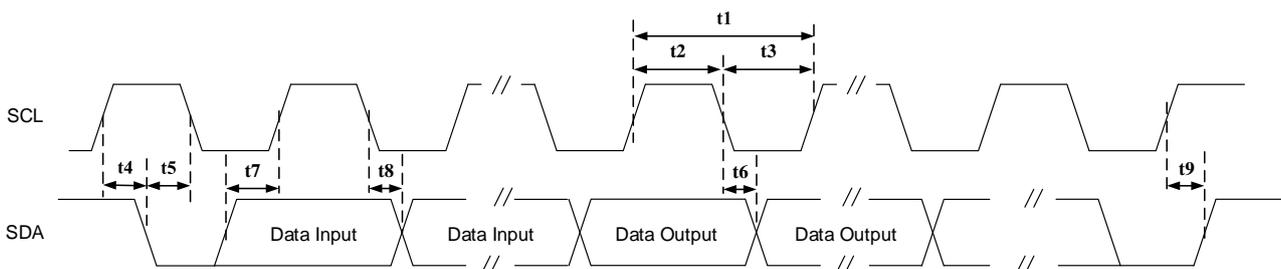
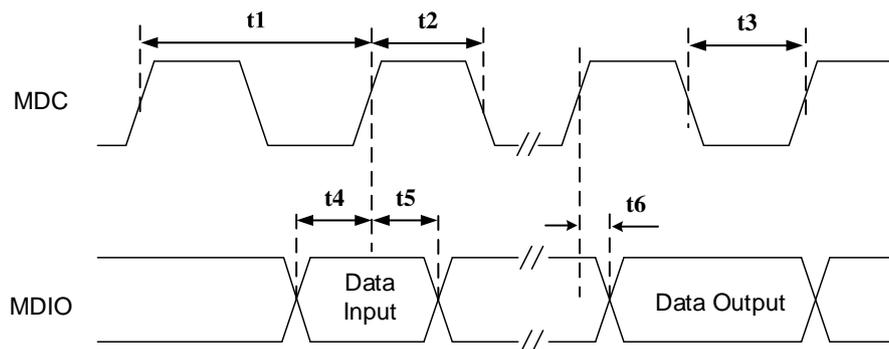


Table 23 Slave I2C Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
Tfreq	SCL Clock Frequency	-	-	400	kHz
t1	SCL Clock Period	2.5	-	-	μs
t2	SCL High Time	0.8	-	-	μs
t3	SCL Low Time	0.8	-	-	μs
t4	START Setup Time	0.3	-	-	μs
t5	START Hold Time	0.3	-	-	μs
t6	SCL Low to Data Output Valid	0.1	-	0.3	μs
t7	Data Input Setup Time	0	-	-	ns
t8	Data Input Hold Time	200	-	-	ns
t9	Stop Setup Time	0.3	-	-	μs

7.4.5 Slave SMI Timing Characteristics

Figure 15 Slave SMI Timing

Table 24 Slave SMI Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
t1	MDC Clock Period	250*	-	-	ns
t2	MDC High Time	80	-	-	ns
t3	MDC Low Time	80	-	-	ns
t4	MDIO to MDC Rising Setup Time (Data Input)	10	-	-	ns
t5	MDIO to MDC Rising Hold Time (Data Input)	10	-	-	ns
t6	MDIO Valid from MDC rising edge (Data Output)	5	-	40*	ns

Note*: The MDIO pin type is Open Drain when working as a slave SMI interface. Therefore, the minimum value of t_1 and the maximum value of t_6 depend on the value of the pull-up resistor on the MDIO signal. Parameters in is the result under the condition of pull-up 1kΩ resistor.

7.4.6 RGMII Timing W/O Delay

Figure 16 RGMII Timing W/O Delay

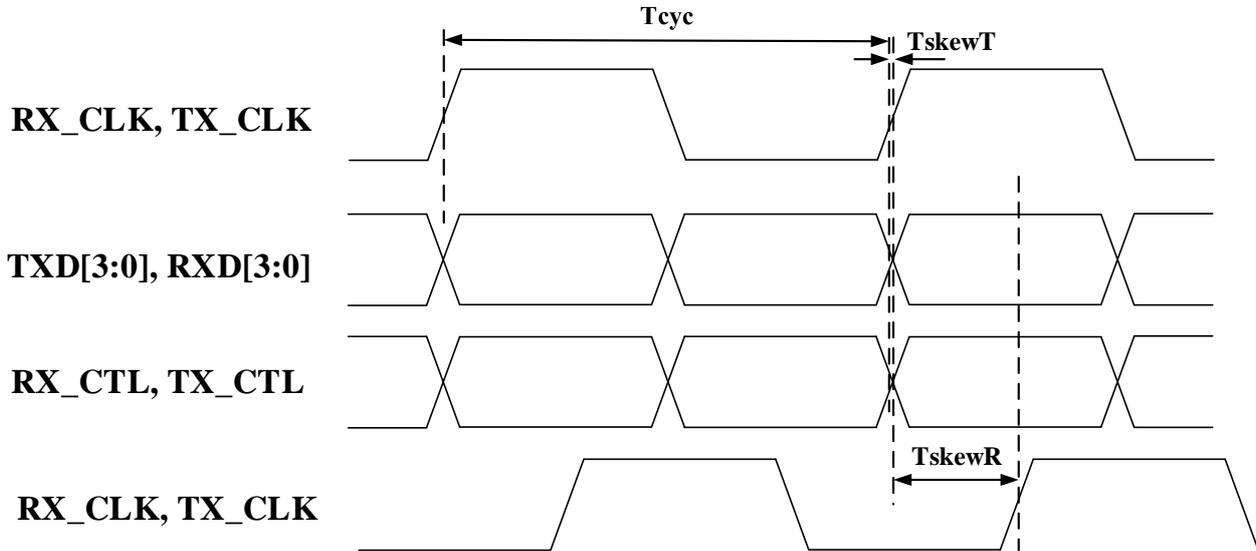


Table 25 RGMII Timing W/O delay

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to clock output skew (at Transmitter)	-500	0	500	ps
TskewR	Data to clock output skew (at Receiver)	1	1.5	2.0	ns
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns
Duty_G	Duty cycle for Gigabit	45	50	55	%
Duty_T	Duty cycle for 10/100T	40	50	60	%

7.4.7 RGMII Timing with Internal Delay

Figure 17 RGMII Timing with Internal Delay

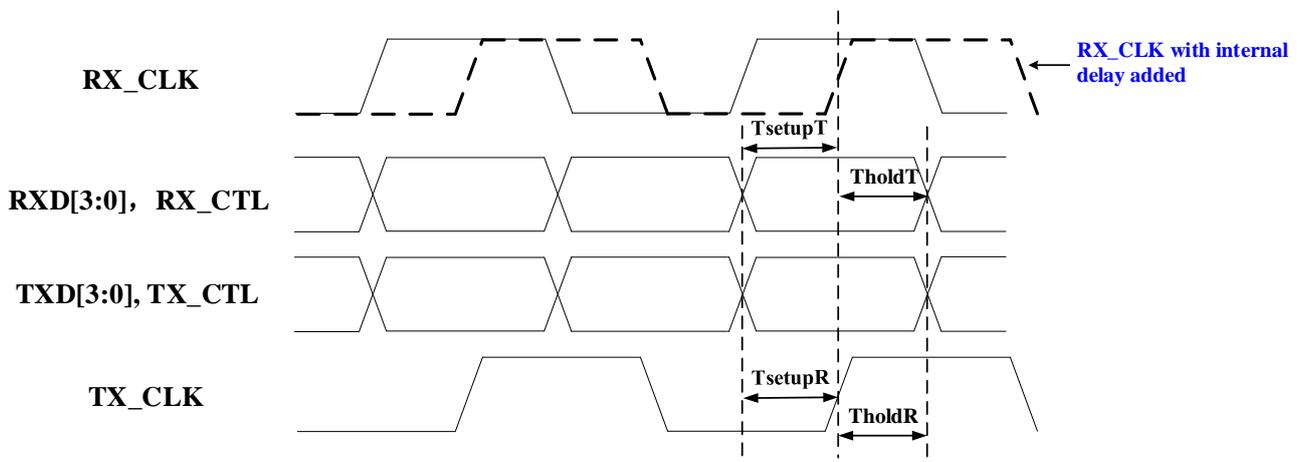


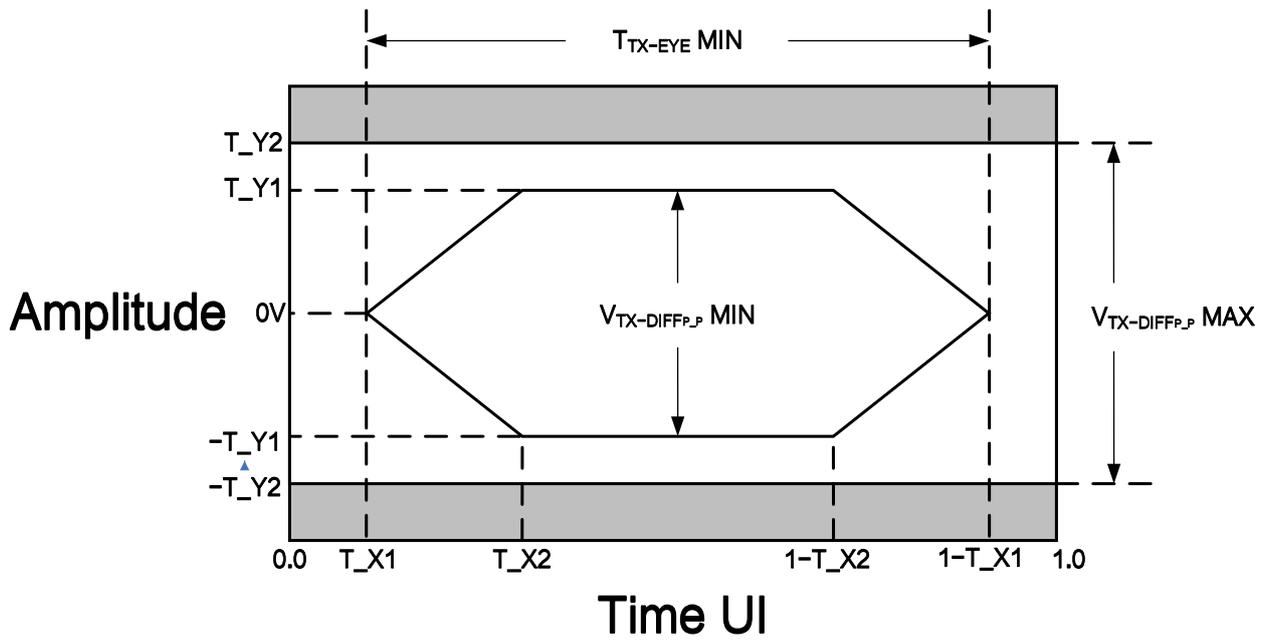
Table 26 RGMII Timing with Internal Delay

Symbol	Parameter	Min	Typ	Max	Unit
TsetupT	Data to Clock output Setup Time (at Transmitter integrated delay)	1.0	2.0	-	ns
TholdT	Clock to Data output Hold Time (at Transmitter integrated delay)	1.0	2.0	-	ns
TsetupR	Data to Clock input Setup Time (at Receiver integrated delay)	1.0	2.0	-	ns
TholdR	Data to Clock input Hold Time (at Receiver integrated delay)	1.0	2.0	-	ns

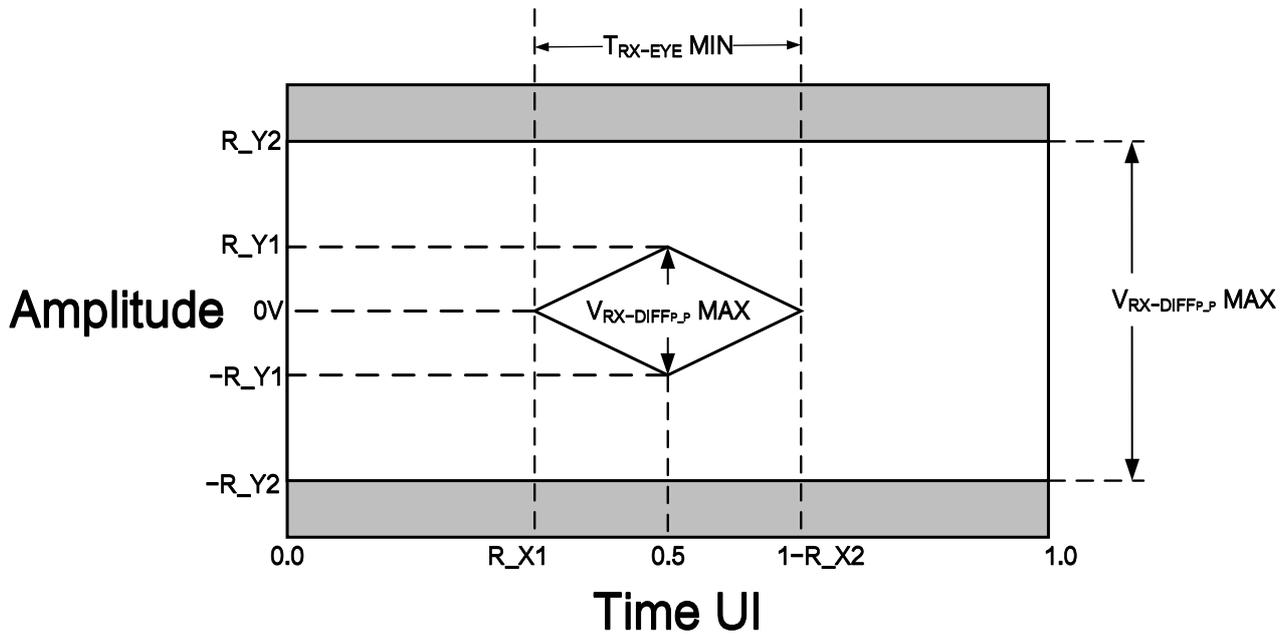
7.4.8 2500Base-X Characteristics

Table 27 2500Base-X Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask	T_X1	-	-	0.2	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mV	-
Eye Mask	T_Y2	-	-	500	mV	-
Output Differential Voltage	$V_{TX-DIFFP-P}$	350	500	900	mV	-
Output Jitter	TJ	$T_{TX-Jitter}$	-	0.3	UI	$T_{TX-JITTER-MAX} = 1 - T_{TX-EYE-MIN} = 0.30UI$
	DJ		-	0.165	UI	-
Minimum TX Eye Width	T_{TX-EYE}	0.7	-	-	UI	-
Output Rise Time	$T_{TX-Rise}$	0.125	-	-	UI	20%-80%
Output Fall Time	$T_{TX-Fall}$	0.125	-	-	UI	20%-80%
Output Differential Impedence	R_{TX}	80	100	120	Ω	-
AC Coupling Capacitor	C_{TX}	80	100	200	nF	-
Transmit Length in PCB	L_{TX}	-	-	20	inch	-

Figure 18 2500Base-X Differential Transmitter Eye Diagram

Table 28 2500Base-X Differential Receiver Characteristics

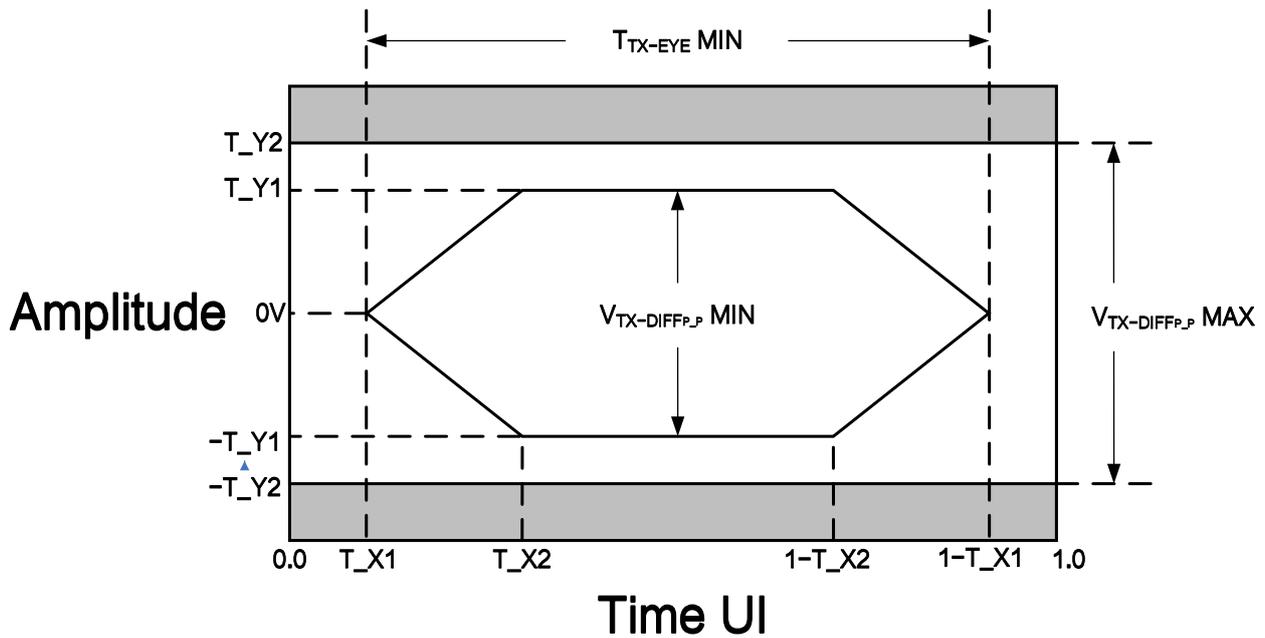
Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	319.968	320	320.032	ps	320ps ± 100ppm
Eye Mask	R_X1	-	-	0.3	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	600	mV	-
Input Differential Voltage	$V_{RX-DIFFP-P}$	200	-	1200	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-Jitter}$	-	-	0.6	UI	$T_{RX-JITTER-MAX} = 1 - T_{RX-EYE-MIN} = 0.6UI$
Input Differential Impedence	R_{RX}	80	100	120	Ω	-

Figure 19 2500Base-X Differential Receiver Eye Diagram


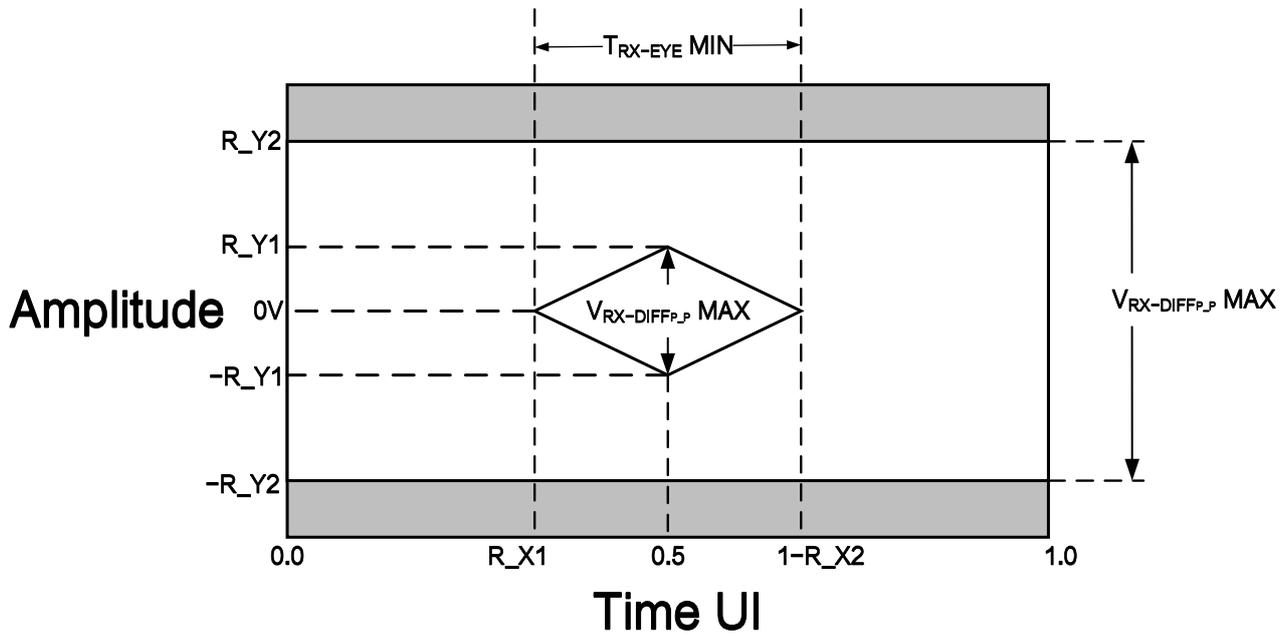
7.4.9 SGMII Characteristics

Table 29 SGMII Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mv	-
Eye Mask	T_Y2	-	-	500	mv	-
Output Differential Voltage	V _{TX-DIFFP-P}	350	700	1000	mv	-
Minimum TX Eye Width	T _{TX-EYE}	0.7	-	-	UI	-
Output Jitter	T _{TX-Jitter}	-	-	0.3	UI	T _{TX-JITTER-MAX} = 1 - T _{TX-EYE-MIN} = 0.30UI
Data-dependent Jitter		-	70	-	ps	-
Output Rise Time	T _{TX-Rise}	100	-	200	ps	20%-80%
Output Fall Time	T _{TX-Fall}	100	-	200	ps	20%-80%
Output Differential Impedance	R _{TX}	80	100	120	Ω	-
AC Coupling Capacitor	C _{TX}	80	100	200	nF	-
Transmit Length in PCB	L _{TX}	-	-	20	inch	-

Figure 20 SGMII Differential Transmitter Eye Diagram

Table 30 SGMII Differential Receiver Characteristics

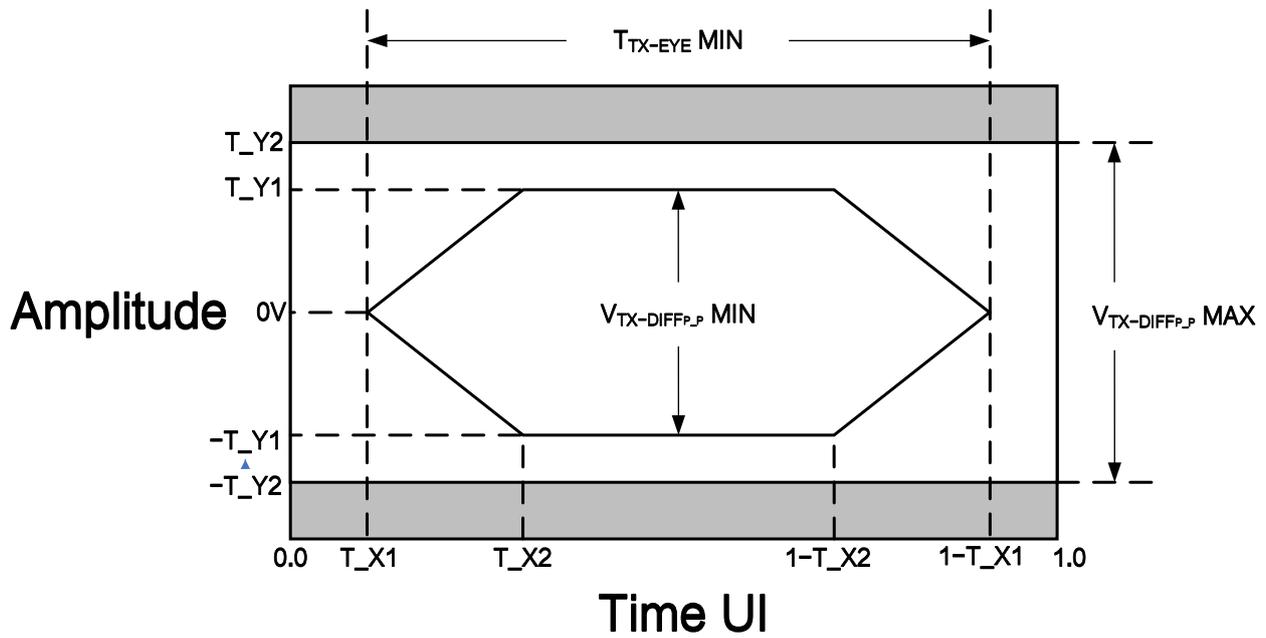
Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	R_X1	-	-	0.3	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	600	mV	-
Input Differential Voltage	$V_{RX-DIFFP-P}$	200	-	1200	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-Jitter}$	-	-	0.6	UI	$T_{RX-JITTER-MAX} = 1 - T_{RX-EYE-MIN} = 0.6UI$
Input Differential Impedence	R_{RX}	80	100	120	Ω	-

Figure 21 SGMII Differential Receiver Eye Diagram


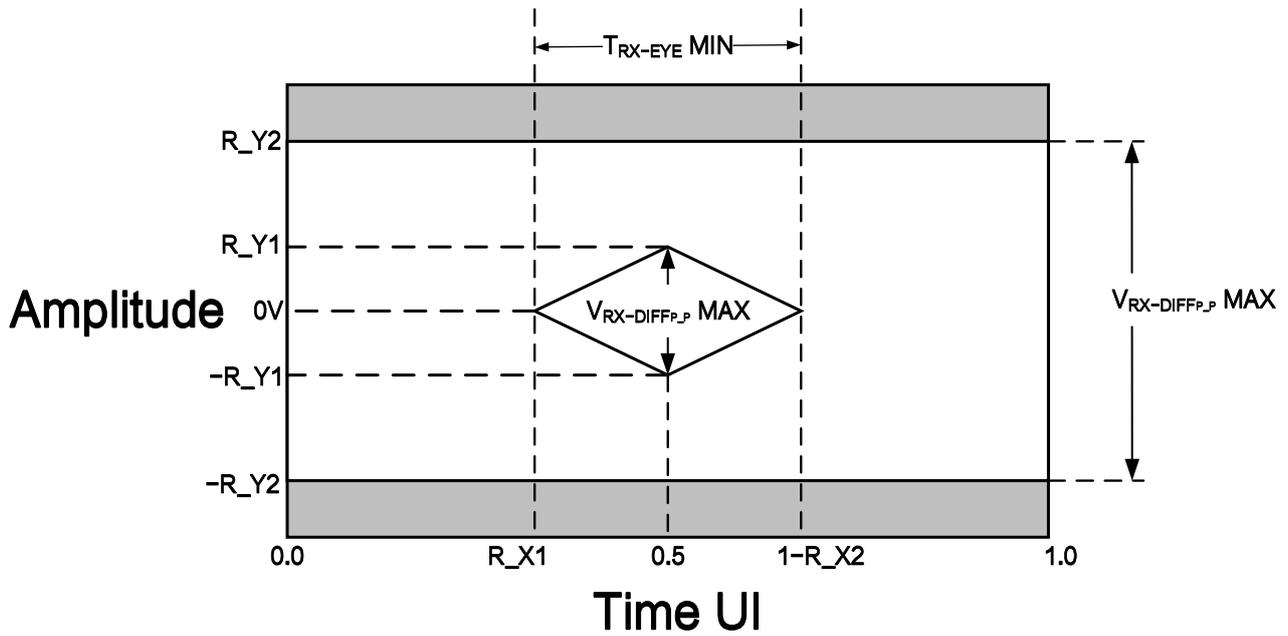
7.4.10 1000Base-X Characteristics

Table 31 1000Base-X Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	799.76	800	800.24	ps	800ps ± 300ppm
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mv	-
Eye Mask	T_Y2	-	-	500	mv	-
Output Differential Voltage	V _{TX-DIFFP-P}	300	700	900	mv	-
Minimum TX Eye Width	T _{TX-EYE}	0.7	-	-	UI	-
Output Jitter	T _{TX-Jitter}	-	-	0.3	UI	T _{TX-JITTER-MAX} = 1 - T _{TX-EYE-MIN} = 0.30UI
Output Rise Time	T _{TX-Rise}	0.075	-	-	UI	20%-80%
Output Fall Time	T _{TX-Fall}	0.075	-	-	UI	20%-80%
Output Impedence	R _{TX}	80	100	120	Ω	-
AC Coupling Capacitor	C _{TX}	80	100	200	nF	-
Transmit Length in PCB	L _{TX}	-	-	20	inch	-

Figure 22 1000Base-X Differential Transmitter Eye Diagram

Table 32 1000Base-X Differential Receiver Characteristics

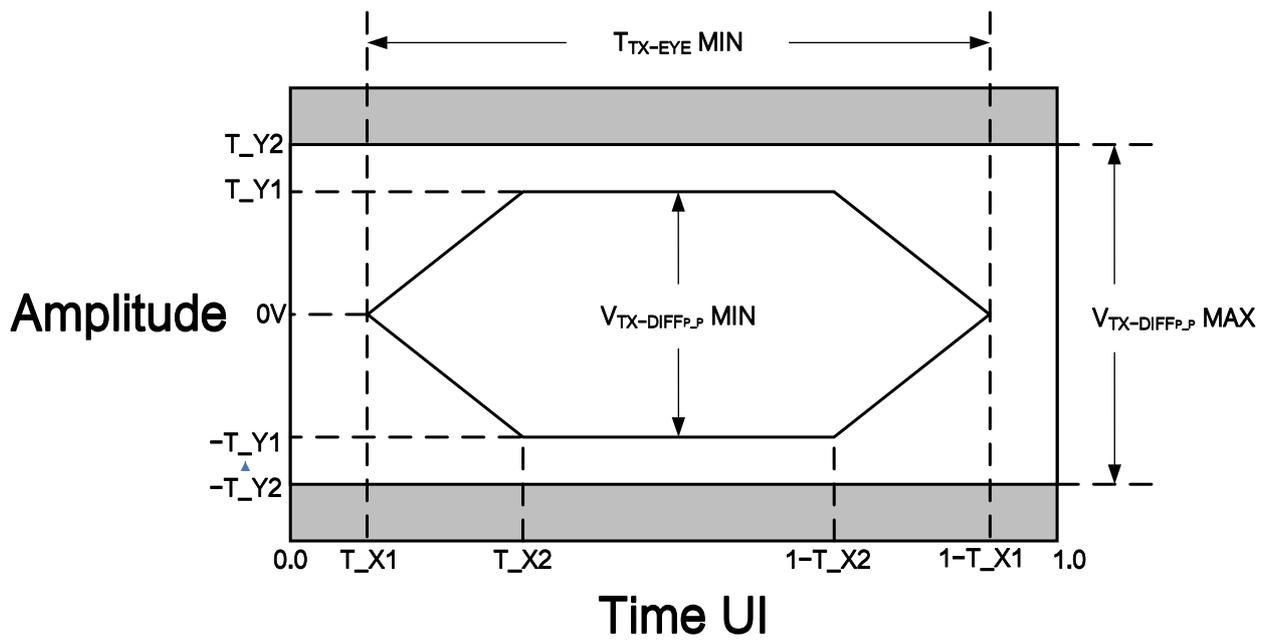
Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	799.76	800	800.24	ps	$800ps \pm 300ppm$
Eye Mask	R_X1	-	-	0.3	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	600	mV	-
Input Differential Voltage	$V_{RX-DIFFP-P}$	200	-	1200	mV	-
Minimum RX Eye Width	T_{RX-EYE}	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{RX-Jitter}$	-	-	0.6	UI	$T_{RX-JITTER-MAX} = 1 - T_{RX-EYE-MIN} = 0.6UI$
Input Differential Impedance	R_{RX}	80	100	120	Ω	-

Figure 23 1000Base-X Differential Receiver Eye Diagram


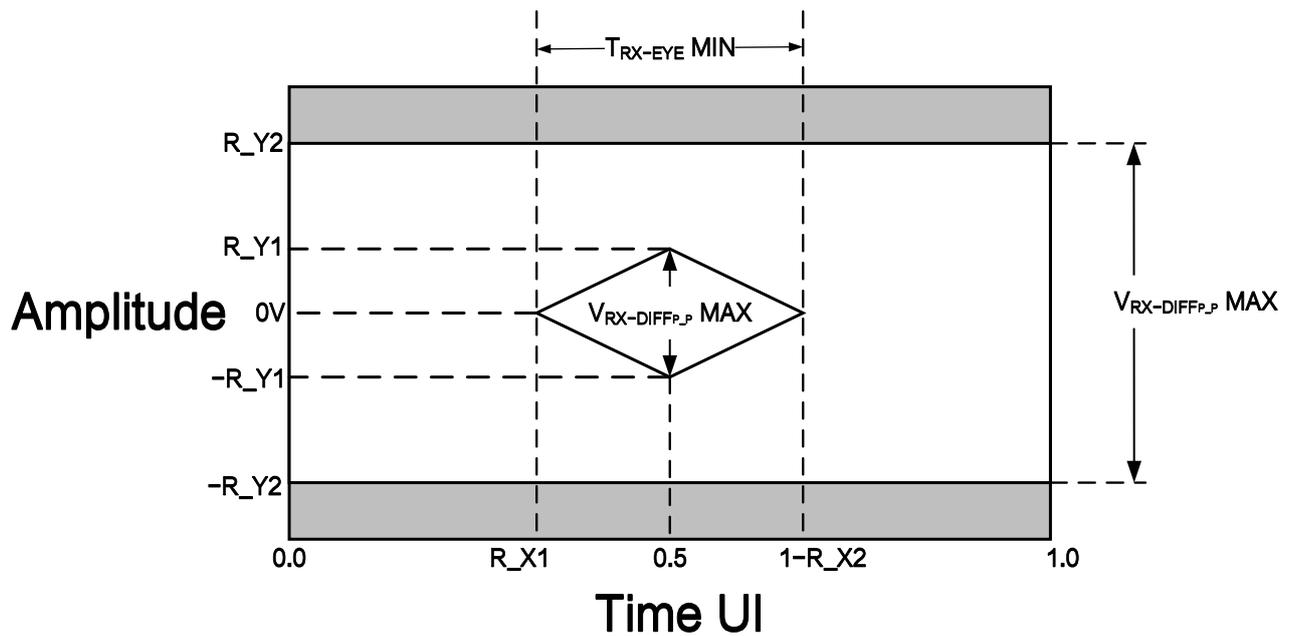
7.4.11 100Base-FX Characteristics

Table 33 100Base-FX Differential Transmitter Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	7.9976	8	8.0024	ns	8ns ± 300ppm
Eye Mask	T_X1	-	-	0.15	UI	-
Eye Mask	T_X2	-	-	0.4	UI	-
Eye Mask	T_Y1	150	-	-	mv	-
Eye Mask	T_Y2	-	-	500	mv	-
Output Differential Voltage	V _{TX-DIFFP-P}	350	700	900	mv	-
Minimum TX Eye Width	T _{TX-EYE}	0.7	-	-	UI	-
Output Jitter	T _{TX-Jitter}	-	-	0.3	UI	T _{TX-JITTER-MAX} = 1 - T _{TX-EYE-MIN} = 0.30UI
Output Rise Time	T _{TX-Rise}	0.075	-	-	UI	20%-80%
Output Fall Time	T _{TX-Fall}	0.075	-	-	UI	20%-80%
Output Impedence	R _{TX}	80	100	120	Ω	-
AC Coupling Capacitor	C _{TX}	80	100	200	nF	-
Transmit Length in PCB	L _{TX}	-	-	20	inch	-

Figure 24 100Base-FX Differential Transmitter Eye Diagram

Table 34 100Base-FX Differential Receiver Characteristics

Parameter	SYM	Min	Typ	Max	Unit	Note
Unit Interval	UI	7.9976	8	8.0024	ns	$8\text{ns} \pm 300\text{ppm}$
Eye Mask	R_X1	-	-	0.3	UI	-
Eye Mask	R_Y1	100	-	-	mV	-
Eye Mask	R_Y2	-	-	600	mV	-
Input Differential Voltage	$V_{\text{RX-DIFFP-P}}$	200	-	1200	mV	-
Minimum RX Eye Width	$T_{\text{RX-EYE}}$	0.4	-	-	UI	-
Input Jitter Tolerance	$T_{\text{RX-Jitter}}$	-	-	0.6	UI	$T_{\text{RX-JITTER-MAX}} = 1 - T_{\text{RX-EYE-MIN}} = 0.6\text{UI}$
Input Differential Impedence	R_{RX}	80	100	120	Ω	-

Figure 25 100Base-FX Differential Receiver Eye Diagram


7.4.12 Crystal Requirement

Table 35 Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Parallel Resonant Crystal Reference Frequency	-	25	-	MHz
Fref Tolerance	Parallel Resonant Crystal Reference Frequency Tolerance	-50	-	50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle	40	-	60	%
ESR	Equivalent Series Resistance	-	-	50	Ω
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.4	-	-	V
Vil	Crystal output low level	-	-	0.7	V

7.4.13 Oscillator/External Clock Requirement

Table 36 Oscillator/External Clock Requirement

Parameter	Min	Typ	Max	Unit
Frequency	-	25	-	MHz
Frequency tolerance	-50	-	50	PPM
Duty Cycle	40	-	60	%
VIH	1.4	-	AVDDH+0.3	V
VIL	-	-	0.7	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns

8 Thermal Resistance

Table 37 Thermal Resistance

Symbol	Parameter	Condition	Typ	Unit
θ_{JA}	Thermal resistance - junction to ambient $\theta_{JA} = (T_J - T_A) / P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no airflow TA=25°C	19.5	°C/W

9 Mechanical Information

Figure 26 Top View

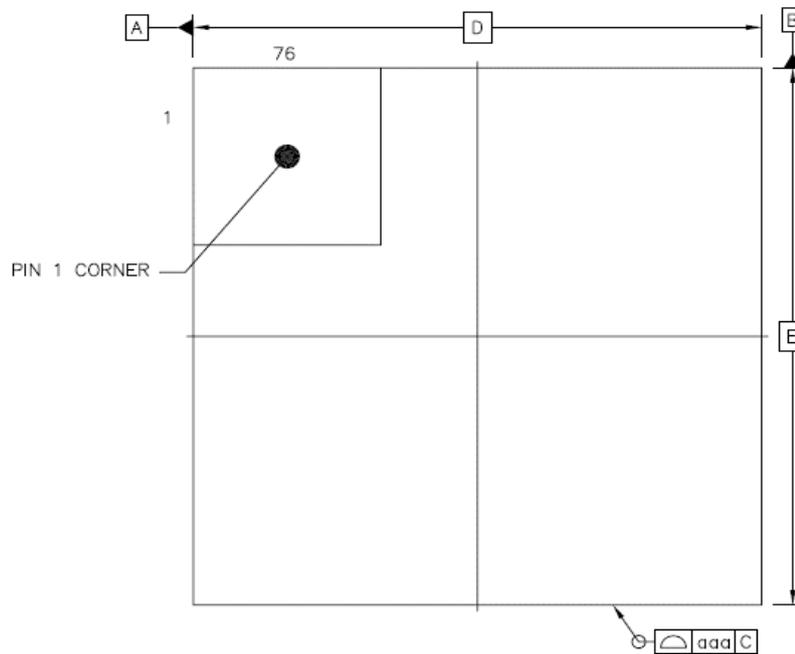


Figure 27 Bottom View

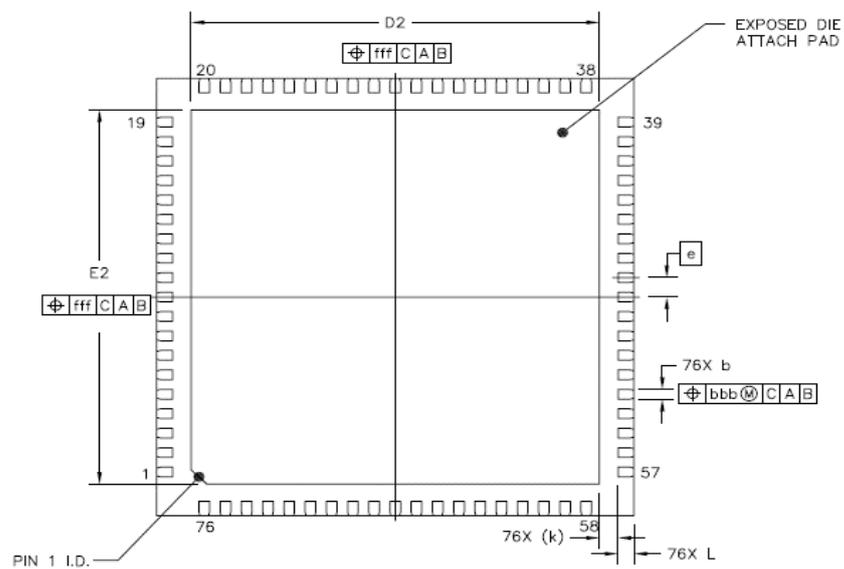


Figure 28 Side View

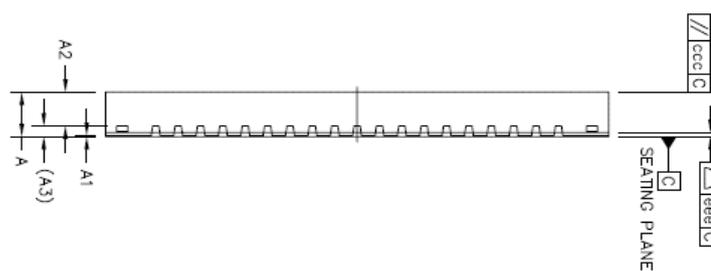


Table 38 Mechanical Dimensions in mm

ITEM		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	-	0.65	-
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	7.6	7.7	7.8
	Y	E2	7.6	7.7	7.8
LEAD LENGTH		L	0.2	0.3	0.4
LEAD TIP TO EXPOSED PAD EDGE		K	0.35 REF		

10 Ordering Information

Motorcomm offers a RoHS package that is compliant with RoHS.

Table 39 Ordering Information

Part Number	Grade	Package	Pack	Status	Operation Temp
YT9213NB	Consumer	QFN76 E-PAD	Tape Reel 2000 ea	Mass Production	0~70°C