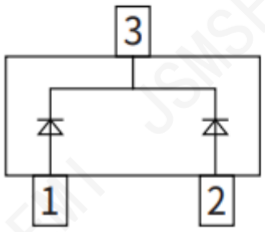
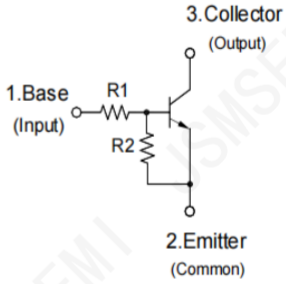
Description

The PDTD113ZT,215-JSM an NPN silicon epitaxial planar digital transistor with built-in bias resistors. It features a compact SOT-23 package, simplifying circuit design while ensuring reliable digital switching performance for various electronic applications.



Features

- Built-in bias resistors for simplified circuit design
- Reduces component count and manufacturing processes
- SOT-23 surface-mounted compact package
- DC current gain (hFE) ≥82 at VCE=5V, IC=50mA
- Transition frequency (fT) typ. 200MHz for high-speed operation



Applications

- Consumer Electronics
- Digital Circuits
- Portable Devices
- Signal Switching Circuits
- Low-Power Electronic Systems

Ordering Information

Order number	Package	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
PDTD113ZT,215-JSM	SOT-23	-55 to+150℃	3	T&R,3000	Rohs

Maximum Ratings(TA=25℃)

Parameter	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	50	V
Input Voltage	V_I	- 10 to + 10	V
Collector Current	I_C	500	mA
Power Dissipation	P_{tot}	200	mW
Junction Temperature	T_j	150	℃
Storage Temperature Range	T_{stg}	- 55 to + 150	℃

Electrical Characteristics(TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = 5 V, I_C = 50 mA	h_{FE}	82	-	-	-
Collector Base Cutoff Current at V_{CB} = 50 V	I_{CBO}	-	-	500	nA
Emitter Base Cutoff Current at V_{EB} = 5 V	I_{EBO}	-	-	7.2	mA
Collector Emitter Saturation Voltage at I_C = 50 mA, I_B = 2.5 mA	$V_{CE(sat)}$	-	-	0.3	V
Input on Voltage at V_{CE} = 0.3 V, I_C = 20 mA	$V_{I(on)}$	-	-	1.5	V
Input off Voltage at V_{CE} = 5 V, I_C = 100 μA	$V_{I(off)}$	0.3	-	-	V
Transition frequency at V_{CE} = 10 V, $-I_E$ = 5 0mA, f = 100 MHz	f_T	-	200	-	MHz
Input Resistance	R_1	0.7	1	1.3	KΩ
Resistance Ratio	R_2 / R_1	0.8	1	1.2	-

Typical Performance Curves

Fig.1 Input voltage vs. output current (ON characteristics)

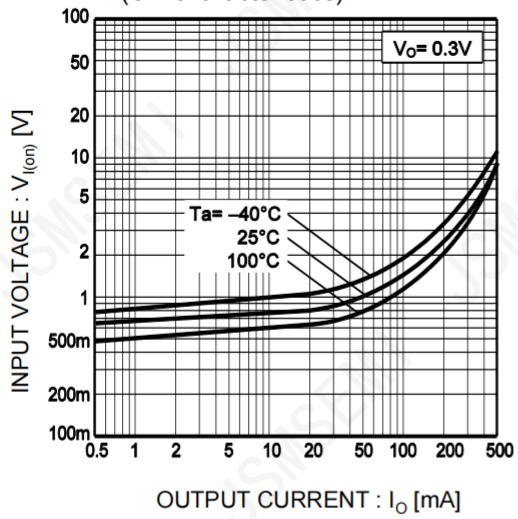


Fig.2 Output current vs. input voltage (OFF characteristics)

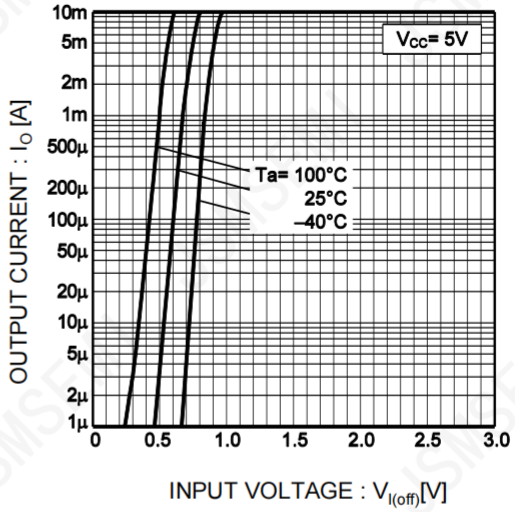


Fig.3 Output current vs. output voltage

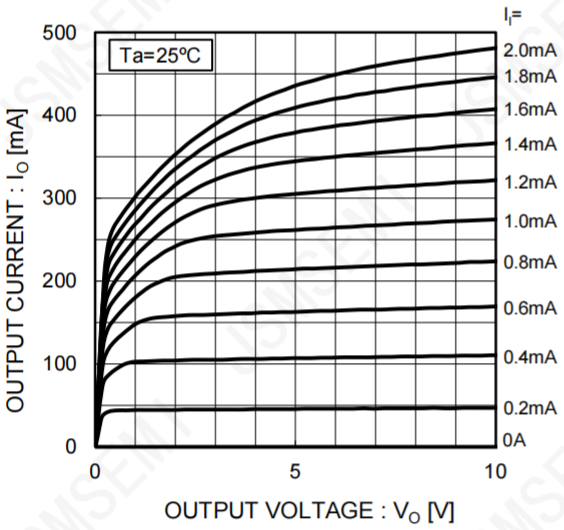


Fig.4 DC current gain vs. output current

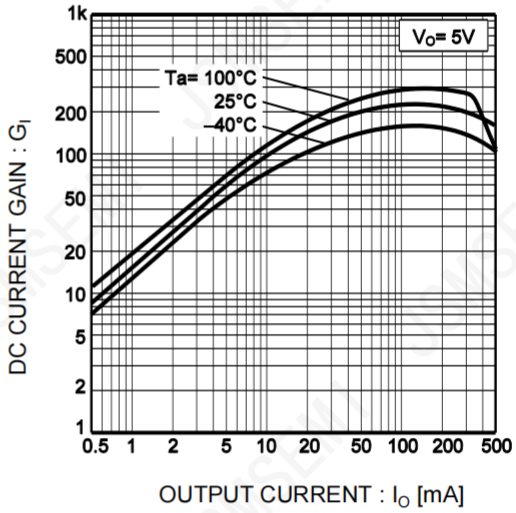
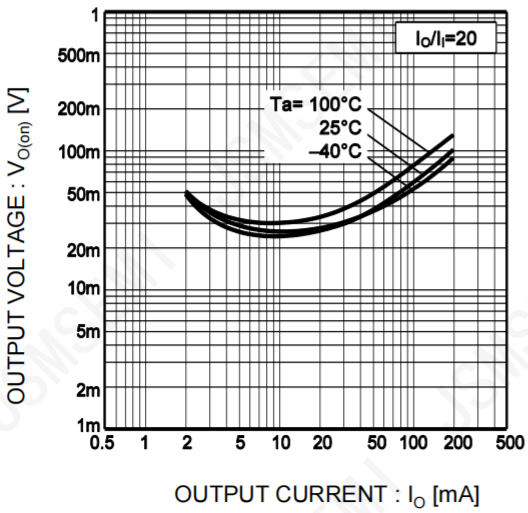
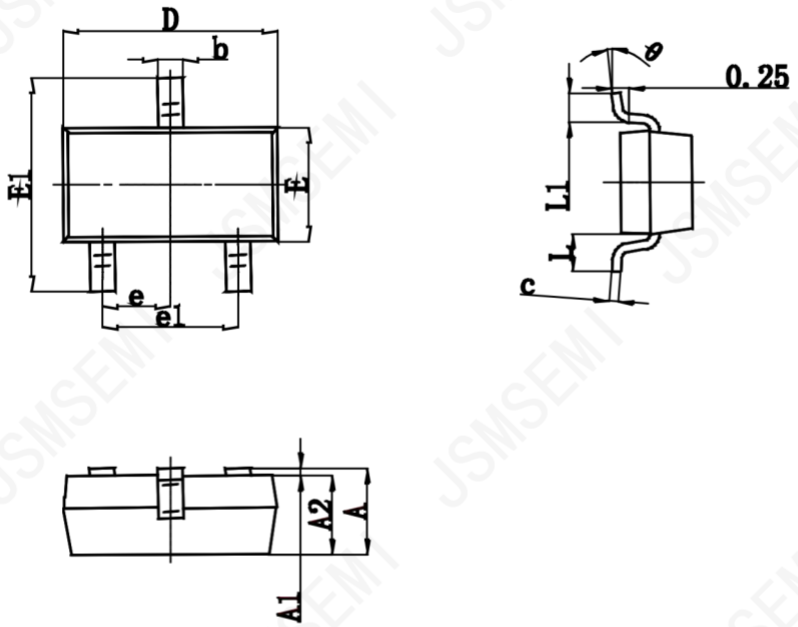


Fig.5 Output voltage vs. output current

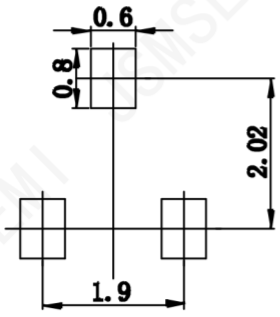


SOT-23 Package Qutline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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