

1、General Description

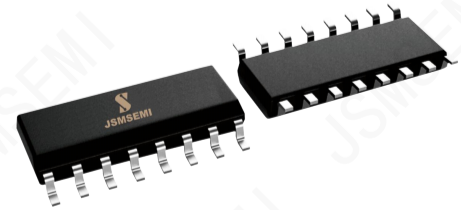
The 74HC4052D,653-JSM is a dual single-pole quad-throw analog switch ($2 \times \text{SP4T}$) suitable for use in analog or digital 4:1 multiplexer/demultiplexer applications. Each switch features four independent inputs/outputs (nY_0 , nY_1 , nY_2 and nY_3) and a common input/output (nZ). A digital enable input ($\bar{E}$) and two digital select inputs (S_0 and S_1) are common to both switches. When $\bar{E}$ is HIGH, the switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features:

- Wide analog input voltage range from -4.5V to +4.5V
- Low ON resistance:
 - 80 Ω (typical) at $V_{CC}-V_{EE}=4.5V$
 - 70 Ω (typical) at $V_{CC}-V_{EE}=6.0V$
 - 60 Ω (typical) at $V_{CC}-V_{EE}=9.0V$

Applications:

- Signal gating
- Digital multiplexing and demultiplexing



- Typical “break before make” built-in
 - Input levels:
 - For 74HC4052: CMOS level
 - Specified from -40°C to +125°C
 - Packaging information: SOP16
- Analog multiplexing and demultiplexing

2、Block Diagram And Pin Description

2.1、Block Diagram

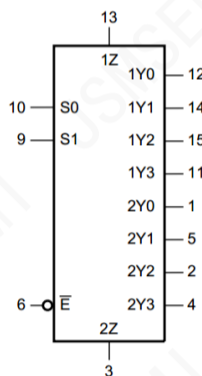


Figure 1. Logic symbol

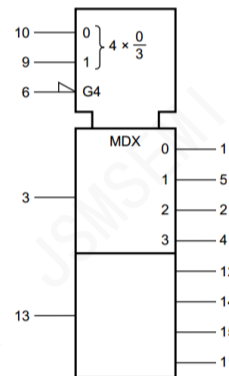


Figure 2. IEC logic symbol

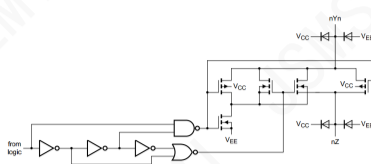


Figure 3. Schematic diagram (one switch)

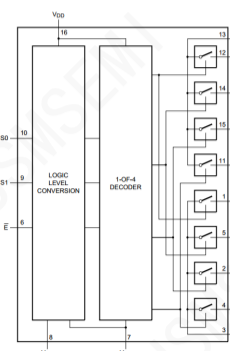
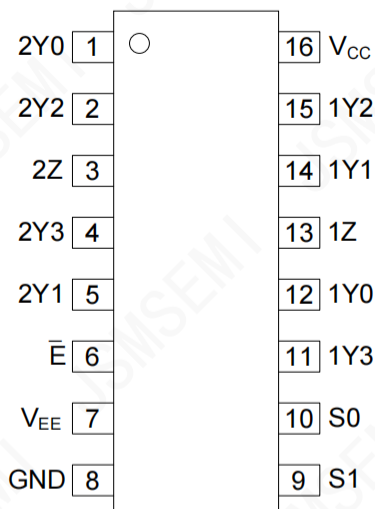


Figure 4. Functional diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	2Y0	independent input or output
2	2Y2	independent input or output
3	2Z	common input or output
4	2Y3	independent input or output
5	2Y1	independent input or output
6	$\bar{E}$	enable input (active LOW)
7	V_{EE}	negative supply voltage
8	GND	ground supply voltage
9	S1	select logic input
10	S0	select logic input
11	1Y3	independent input or output
12	1Y0	independent input or output
13	1Z	common input or output
14	1Y1	independent input or output
15	1Y2	independent input or output
16	V_{CC}	positive supply voltage

2.4、Function Table

Input			Channel ON
$\bar{E}$	S1	S0	
L	L	L	nY0 and nZ
L	L	H	nY1 and nZ
L	H	L	nY2 and nZ
L	H	H	nY3 and nZ
H	X	X	none

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to $V_{EE} = \text{GND}$ (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	- [1]	-0.5	+11	V
input clamping current	I_{IK}	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
switch clamping current	I_{SK}	$V_{SW} < -0.5 \text{ V}$ or $V_{SW} > V_{CC} + 0.5 \text{ V}$	-	± 20	mA
switch current	I_{SW}	$-0.5 \text{ V} < V_{SW} < V_{CC} + 0.5 \text{ V}$	-	± 25	mA
supply current	I_{EE}	-	-	± 20	mA
supply current	I_{CC}	-	-	50	mA
ground current	I_{GND}	-	-	-50	mA
storage temperature	T_{stg}	-	-65	+150	°C
total power dissipation	P_{tot}	-	-	500	mW
power dissipation	P	per switch	-	100	mW
Soldering temperature	T_L	10s	260		°C

Note:

[1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows into terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nYn, and in this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE} .

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{CC}	$V_{CC} - \text{GND}$	3.0	5.0	9.0	V
		$V_{CC} - V_{EE}$	3.0	5.0	9.0	V
input voltage	V_I	-	0	-	V_{CC}	V
switch voltage	V_{SW}	-	V_{EE}	-	V_{CC}	V
ambient temperature	T_{amb}	in free air	-40	-	+125	°C
input transition rise and fall rate	$\Delta t / \Delta V$	$V_{CC} = 4.5 \text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	ns/V
		$V_{CC} = 9.0 \text{ V}$	-	-	31	ns/V

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb} = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$, voltages are reference to GND (ground=0V), unless otherwise specified, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. ^[1]	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	$V_{is} = V_{CC} \text{ to } V_{EE};$ $I_{SW} = 1000 \text{ uA}$	$V_{CC} = 4.5 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	100	225	Ω
			$V_{CC} = 6.0 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	90	200	Ω
			$V_{CC} = 4.5 \text{ V};$ $V_{EE} = -4.5 \text{ V}$	-	70	165	Ω
ON resistance (rail)	$R_{ON(rail)}$	$V_{is} = V_{EE};$ $I_{SW} = 1000 \text{ uA}$	$V_{CC} = 4.5 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	80	175	Ω
			$V_{CC} = 6.0 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	70	150	Ω
			$V_{CC} = 4.5 \text{ V};$ $V_{EE} = -4.5 \text{ V}$	-	60	130	Ω
		$V_{is} = V_{CC};$ $I_{SW} = 1000 \text{ uA}$	$V_{CC} = 4.5 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	90	200	Ω
			$V_{CC} = 6.0 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	80	175	Ω
			$V_{CC} = 4.5 \text{ V};$ $V_{EE} = -4.5 \text{ V}$	-	65	150	Ω
ON resistance mismatch between channels	ΔR_{ON}	$V_{is} = V_{CC} \text{ to } V_{EE}$	$V_{CC} = 4.5 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	9	-	Ω
			$V_{CC} = 6.0 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	8	-	Ω
			$V_{CC} = 4.5 \text{ V};$ $V_{EE} = -4.5 \text{ V}$	-	6	-	Ω
HIGH-level input voltage	V_{IH}	$V_{CC} = 4.5 \text{ V}$		3.15	2.4	-	V
		$V_{CC} = 6.0 \text{ V}$		4.2	3.2	-	V
		$V_{CC} = 9.0 \text{ V}$		6.3	4.7	-	V
LOW-level input voltage	V_{IL}	$V_{CC} = 4.5 \text{ V}$		-	2.1	1.35	V
		$V_{CC} = 6.0 \text{ V}$		-	2.8	1.8	V
		$V_{CC} = 9.0 \text{ V}$		-	4.3	2.7	V
input leakage current	I_I	$V_{EE} = 0 \text{ V};$ $V_I = V_{CC} \text{ or GND}$	$V_{CC} = 6.0 \text{ V}$	-	-	± 1.0	μA
			$V_{CC} = 9.0 \text{ V}$	-	-	± 2.0	μA

OFF-state leakage current	$I_{S(OFF)}$	$V_{CC}=9.0\text{ V};$ $V_{EE}=0\text{ V};$ $V_I=V_{IH}\text{ or }V_{IL};$ $ V_{SW} =V_{CC}-V_{EE};$ see Figure 7	per channel	-	-	± 1.0	μA
			all channels	-	-	± 2.0	μA
ON-state leakage current	$I_{S(ON)}$	$V_I=V_{IH}\text{ or }V_{IL}; V_{SW} =V_{CC}-V_{EE};$ $V_{CC}=9.0\text{ V};V_{EE}=0\text{ V};$ see Figure 8	-	-	-	± 2.0	μA
supply current	I_{CC}	$V_{EE}=0\text{ V};$ $V_I=V_{CC}\text{ or GND};$ $V_{is}=V_{EE}\text{ or }V_{CC};$ $V_{os}=V_{CC}\text{ or }V_{EE}$	$V_{CC}=6.0\text{ V}$	-	-	80.0	μA
			$V_{CC}=9.0\text{ V}$	-	-	160.0	μA
input capacitance	C_I	-	-	3.5	-	-	pF
switch capacitance	C_{SW}	independent pins nYn	-	5	-	-	pF
		common pins nZ	-	12	-	-	pF

Note:

[1] All typical values are measured at $T_{amb}=25^\circ\text{C}$.

[2] $V_I=V_{IH}\text{ or }V_{IL}$; for test circuit see Figure 5.

[3] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[4] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

3.3.2、DC Characteristics 2

($T_{amb} = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$, voltages are reference to GND (ground=0V), unless otherwise specified, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. ^[1]	Max.	Unit
ON resistance (peak)	$R_{ON(peak)}$	$V_{is} = V_{CC} \text{ to } V_{EE};$ $I_{SW} = 1000 \text{ uA}$	$V_{CC} = 4.5 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	-	270	Ω
			$V_{CC} = 6.0 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	-	240	Ω
			$V_{CC} = 4.5 \text{ V};$ $V_{EE} = -4.5 \text{ V}$	-	-	195	Ω
ON resistance (rail)	$R_{ON(rail)}$	$V_{is} = V_{EE};$ $I_{SW} = 1000 \text{ uA}$	$V_{CC} = 4.5 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	-	210	Ω
			$V_{CC} = 6.0 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	-	180	Ω
			$V_{CC} = 4.5 \text{ V};$ $V_{EE} = -4.5 \text{ V}$	-	-	160	Ω
		$V_{is} = V_{CC};$ $I_{SW} = 1000 \text{ uA}$	$V_{CC} = 4.5 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	-	240	Ω
			$V_{CC} = 6.0 \text{ V};$ $V_{EE} = 0 \text{ V}$	-	-	210	Ω
			$V_{CC} = 4.5 \text{ V};$ $V_{EE} = -4.5 \text{ V}$	-	-	180	Ω
HIGH-level input voltage	V_{IH}	$V_{CC} = 4.5 \text{ V}$		3.15	-	-	V
		$V_{CC} = 6.0 \text{ V}$		4.2	-	-	V
		$V_{CC} = 9.0 \text{ V}$		6.3	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC} = 4.5 \text{ V}$		-	-	1.35	V
		$V_{CC} = 6.0 \text{ V}$		-	-	1.8	V
		$V_{CC} = 9.0 \text{ V}$		-	-	2.7	V
input leakage current	I_I	$V_{EE} = 0 \text{ V};$ $V_I = V_{CC} \text{ or GND}$	$V_{CC} = 6.0 \text{ V}$	-	-	± 1.0	μA
			$V_{CC} = 9.0 \text{ V}$	-	-	± 2.0	μA
OFF-state leakage current	$I_{S(OFF)}$	$V_{CC} = 9.0 \text{ V};$ $V_{EE} = 0 \text{ V};$ $V_I = V_{IH} \text{ or } V_{IL};$ $ V_{SW} = V_{CC} - V_{EE};$	per channel	-	-	± 1.0	μA
			all channels	-	-	± 2.0	μA

		see Figure 7					
ON-state leakage current	$I_{S(ON)}$	$V_I = V_{IH} \text{ or } V_{IL}; V_{SW} = V_{CC} - V_{EE};$ $V_{CC} = 9.0 \text{ V}; V_{EE} = 0 \text{ V};$ see Figure 8		-	-	± 2.0	μA
supply current	I_{CC}	$V_{EE} = 0 \text{ V};$ $V_I = V_{CC} \text{ or } \text{GND};$ $V_{is} = V_{EE} \text{ or } V_{CC};$ $V_{os} = V_{CC} \text{ or } V_{EE}$	$V_{CC} = 6.0 \text{ V}$	-	-	160.0	μA
		$V_{CC} = 9.0 \text{ V}$	-	-	320.0	μA	

Note:

[1] All typical values are measured at $T_{amb} = 25^\circ\text{C}$.

[2] $V_I = V_{IH} \text{ or } V_{IL}$; for test circuit see Figure 5.

[3] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[4] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

3.3.3、AC Characteristics 1

($T_{amb} = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$; $GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. ^[1]	Max.	Unit
propagation delay	t _{pd}	V _{is} to V _{os} ; R _L = ∞ Ω; see Figure 9 ^[2]	V _{CC} = 4.5 V; V _{EE} = 0 V	-	5	15	ns
			V _{CC} = 6.0 V; V _{EE} = 0 V	-	4	13	ns
			V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	4	10	ns
turn-on time	t _{on}	$\bar{E}$, Sn to V _{os} ; R _L = ∞ Ω; see Figure 10 ^[3]	V _{CC} = 4.5 V; V _{EE} = 0 V	-	38	81	ns
			V _{CC} = 5.0 V; V _{EE} =0V; C _L =15pF	-	28	-	ns
			V _{CC} = 6.0 V; V _{EE} = 0 V	-	30	69	ns
			V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	26	58	ns
turn-off time	t _{off}	$\bar{E}$, Sn to V _{os} ; R _L = 1 kΩ; see Figure 10 ^[4]	V _{CC} = 4.5 V; V _{EE} = 0 V	-	27	63	ns
			V _{CC} = 5.0 V; V _{EE} =0V; C _L =15pF	-	21	-	ns
			V _{CC} = 6.0 V; V _{EE} = 0 V	-	22	54	ns
			V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	22	48	ns
power dissipation capacitance	C _{PD}	per switch;V _I = GND to V _{CC} ^[5]		-	57	-	pF

Note: [1] All typical values are measured at $T_{amb} = 25^{\circ}\text{C}$.

[2] t_{pd} is the same as t_{PHL} and t_{PLH} .

[3] t_{on} is the same as t_{pZH} and t_{pZL} .

[4] t_{off} is the same as t_{pHZ} and t_{pLZ} .

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum \{(C_L + C_{SW}) \times V_{CC}^2 \times f_o\} \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

N = number of inputs switching;

$\sum \{(C_L + C_{SW}) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_{SW} = switch capacitance in pF;

V_{CC} = supply voltage in V.

[6] For test circuit see Figure 11.

[7] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[8] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

3.3.4、AC Characteristics 2

($T_{amb} = -40^{\circ}\text{C} \sim +125^{\circ}\text{C}$; $GND = 0\text{ V}$; $t_r = t_f = 6\text{ ns}$; $C_L = 50\text{ pF}$; unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ. ^[1]	Max.	Unit
propagation delay	t _{pd}	V _{is} to V _{os} ; R _L = ∞ Ω; see Figure 9 ^[2]	V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	18	ns
			V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	15	ns
			V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	12	ns
turn-on time	t _{on}	$\bar{E}$, Sn to V _{os} ; R _L = ∞ Ω; see Figure 10 ^[3]	V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	98	ns
			V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	83	ns
			V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	69	ns
turn-off time	t _{off}	$\bar{E}$, Sn to V _{os} ; R _L = 1 kΩ; see Figure 10 ^[4]	V _{CC} = 4.5 V; V _{EE} = 0 V	-	-	75	ns
			V _{CC} = 6.0 V; V _{EE} = 0 V	-	-	64	ns
			V _{CC} = 4.5 V; V _{EE} = -4.5 V	-	-	57	ns

Note:

[1] All typical values are measured at $T_{amb} = 25^{\circ}\text{C}$.

[2] t_{pd} is the same as t_{PHL} and t_{PLH} .

[3] t_{on} is the same as t_{pZH} and t_{pZL} .

[4] t_{off} is the same as t_{pHZ} and t_{pLZ} .

[5] For test circuit see Figure 11.

[6] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

[7] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

3.3.5、AC Characteristics 3

($T_{amb} = 25^{\circ}\text{C}$; $GND = 0\text{V}$; $C_L = 50\text{pF}$; recommended conditions and typical values.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
sine-wave distortion	d_{sin}	$f_i = 1\text{ kHz};$ $R_L = 10\text{ k}\Omega;$ see Figure 12	$V_{is} = 4.0\text{ V (p-p)};$ $V_{CC} = 2.25\text{ V};$ $V_{EE} = -2.25\text{ V}$	-	0.04	-	%
			$V_{is} = 8.0\text{ V (p-p)};$ $V_{CC} = 4.5\text{ V};$ $V_{EE} = -4.5\text{ V}$	-	0.02	-	%
		$f_i = 10\text{ kHz};$ $R_L = 10\text{ k}\Omega;$ see Figure 12	$V_{is} = 4.0\text{ V (p-p)};$ $V_{CC} = 2.25\text{ V};$ $V_{EE} = -2.25\text{ V}$	-	0.12	-	%
			$V_{is} = 8.0\text{ V (p-p)};$ $V_{CC} = 4.5\text{ V};$ $V_{EE} = -4.5\text{ V}$	-	0.06	-	%
isolation (OFF-state)	α_{iso}	$R_L = 600\text{ }\Omega;$ $f_i = 1\text{ MHz};$ see Figure 13	$V_{CC} = 2.25\text{ V};$ ^[1] $V_{EE} = -2.25\text{ V}$	-	-50	-	dB
			$V_{CC} = 4.5\text{ V};$ ^[1] $V_{EE} = -4.5\text{ V}$	-	-50	-	dB
crosstalk	Xtalk	between two switches/multiplexers; $R_L = 600\text{ }\Omega; f_i = 1\text{ MHz};$ see Figure 14	$V_{CC} = 2.25\text{ V};$ ^[1] $V_{EE} = -2.25\text{ V}$	-	-60	-	dB
			$V_{CC} = 4.5\text{ V};$ ^[1] $V_{EE} = -4.5\text{ V}$	-	-60	-	dB
crosstalk voltage	V_{ct}	peak-to-peak value; between control and any switch; $R_L = 600\text{ }\Omega; f_i = 1\text{ MHz};$ $\bar{E}$ or Sn square wave between V_{CC} and GND; $t_r = t_f = 6\text{ ns};$ see Figure 15	$V_{CC} = 4.5\text{ V};$ $V_{EE} = 0\text{ V}$	-	110	-	mV
			$V_{CC} = 4.5\text{ V};$ $V_{EE} = -4.5\text{ V}$	-	220	-	mV
-3dB frequency response	$f_{(-3dB)}$	$R_L = 50\text{ }\Omega;$ see Figure 16	$V_{CC} = 2.25\text{ V};$ ^[2] $V_{EE} = -2.25\text{ V}$	-	170	-	MHz
			$V_{CC} = 4.5\text{ V};$ ^[2] $V_{EE} = -4.5\text{ V}$	-	180	-	MHz

Note:

- [1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).
 [2] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).
 [3] V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
 [4] V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

4、Testing Circuit

4.1、DC Testing Circuit 1

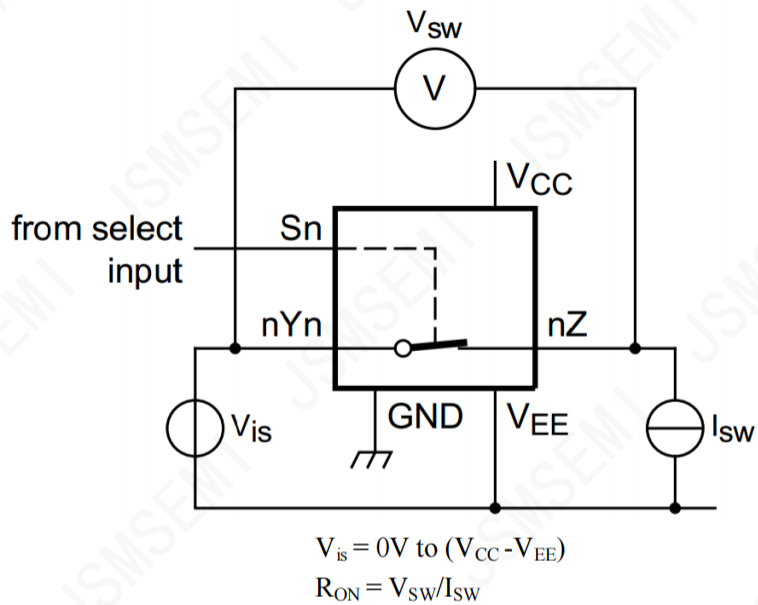
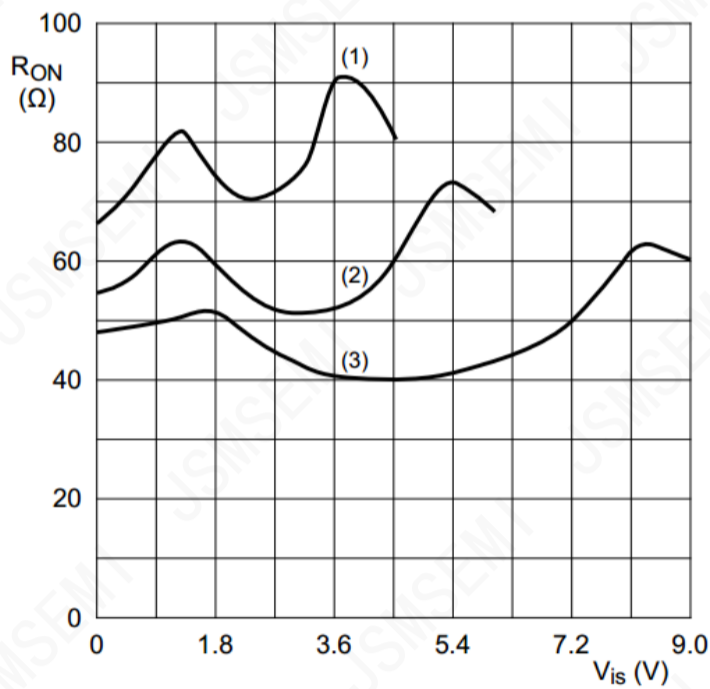


Figure 5. Test circuit for measuring R_{ON}



$V_{is} = 0V \text{ to } (V_{CC} - V_{EE})$

(1) $V_{CC} = 4.5V$

(2) $V_{CC} = 6V$

(3) $V_{CC} = 9V$

Figure 6. Typical R_{ON} as a function of input voltage V_{is}

4.2、DC Testing Circuit 2

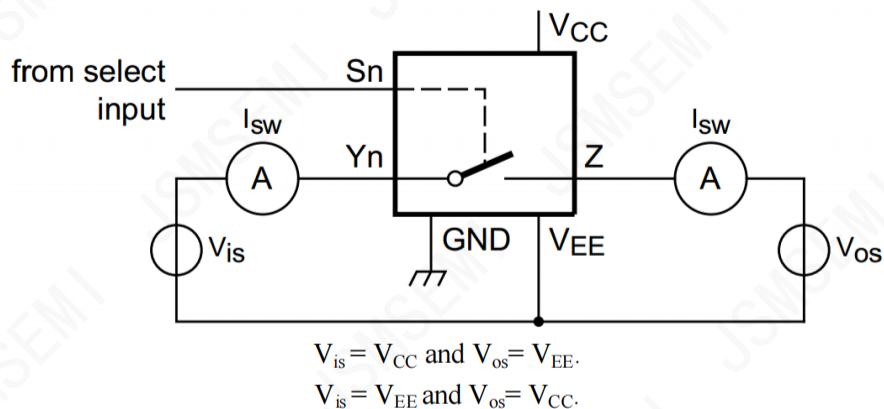


Figure 7. Test circuit for measuring OFF-state current

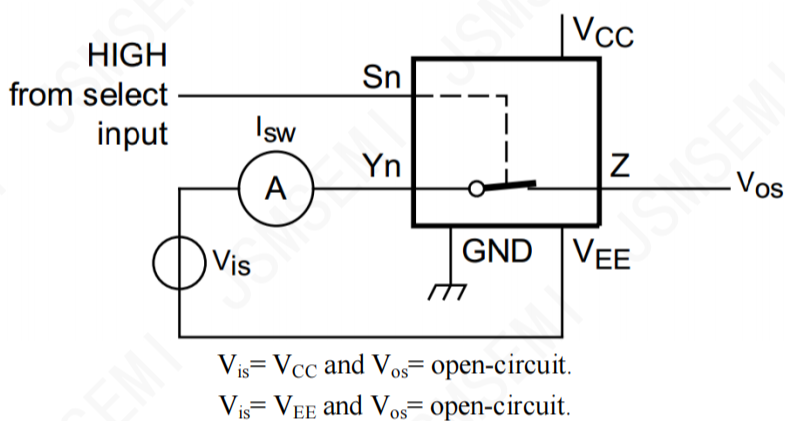


Figure 8. Test circuit for measuring ON-state current

4.3、AC Testing Waveforms

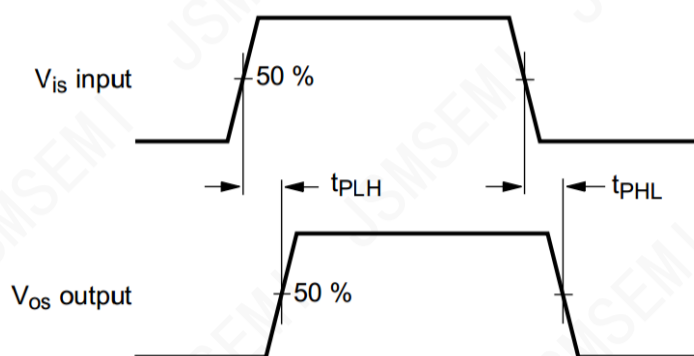
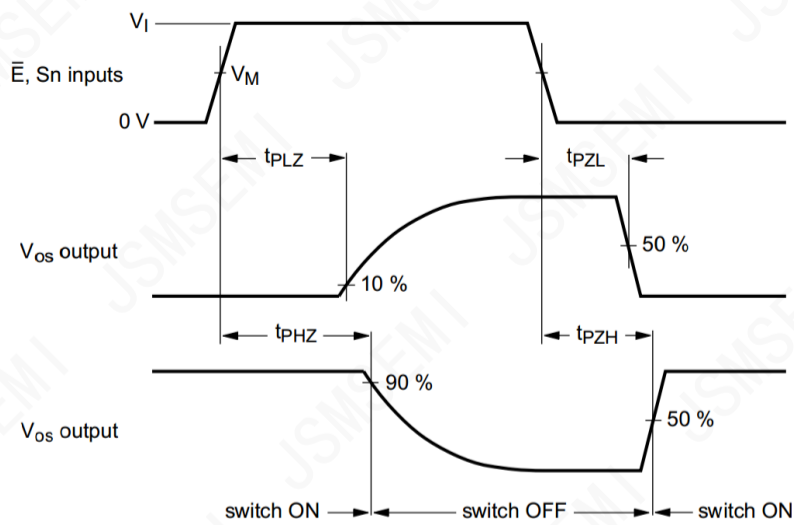


Figure 9. Input (V_{is}) to output (V_{os}) propagation delays



For 74HC4052: $V_M = 0.5 \times V_{CC}$.

Figure 10. Turn-on and turn-off times

4.4、AC Testing Circuit 1

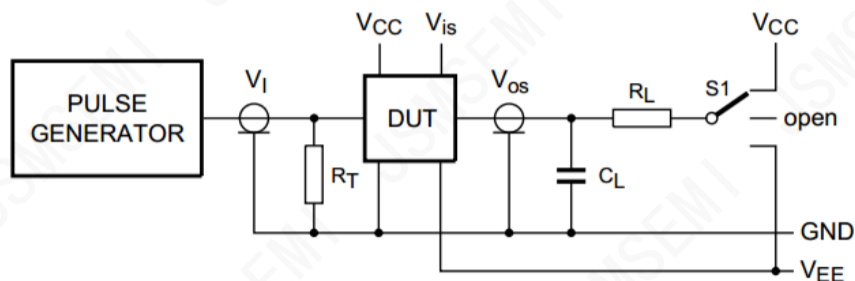
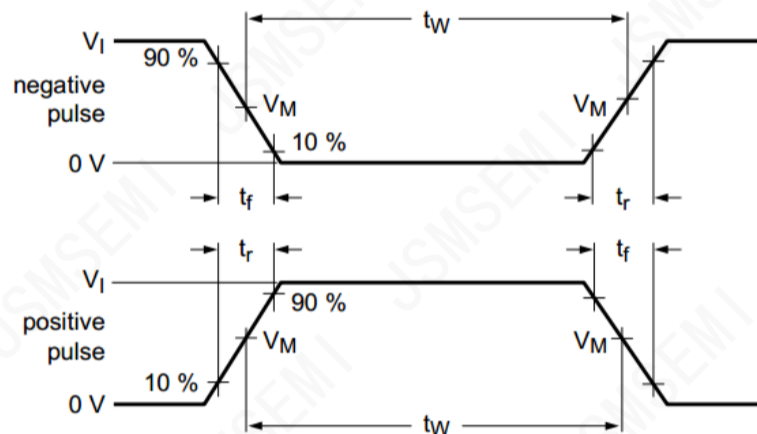


Figure 11. Test circuit for measuring switching times

Definitions for test circuit:

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

$S1$ = Test selection switch.

4.5、Test Data

Test	Input				Load		S1 position
	V _I	V _{is}	t _r , t _f		C _L	R _L	
			at f _{max}	other ^[1]			
t _{PHL} ,t _{PLH}	[2]	pulse	< 2ns	6ns	50pF	1kΩ	open
t _{PZH} , t _{PHZ}	[2]	V _{CC}	< 2ns	6ns	50pF	1kΩ	V _{EE}
t _{PZL} , t _{PLZ}	[2]	V _{EE}	< 2ns	6ns	50pF	1kΩ	V _{CC}

Note:

[1] $t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint to t_r and t_f with 50 % duty factor.

[2] V_I values:

For 74HC4052: $V_I = V_{CC}$.

4.6、AC Testing Circuit 2

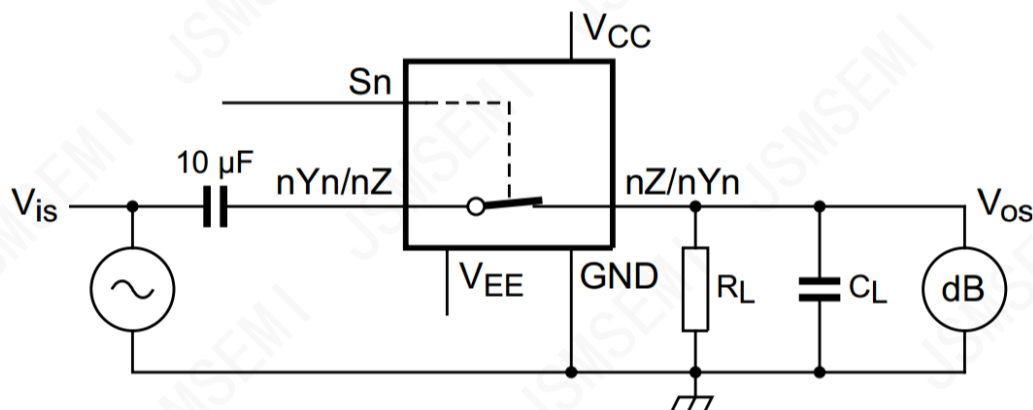
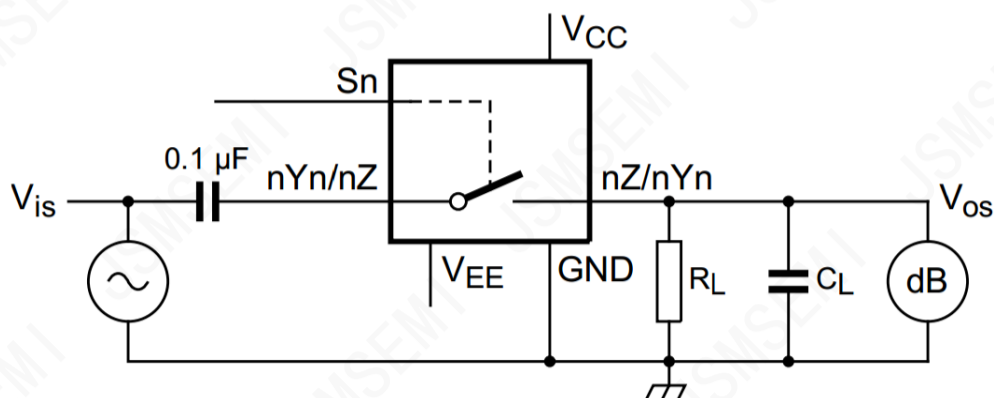
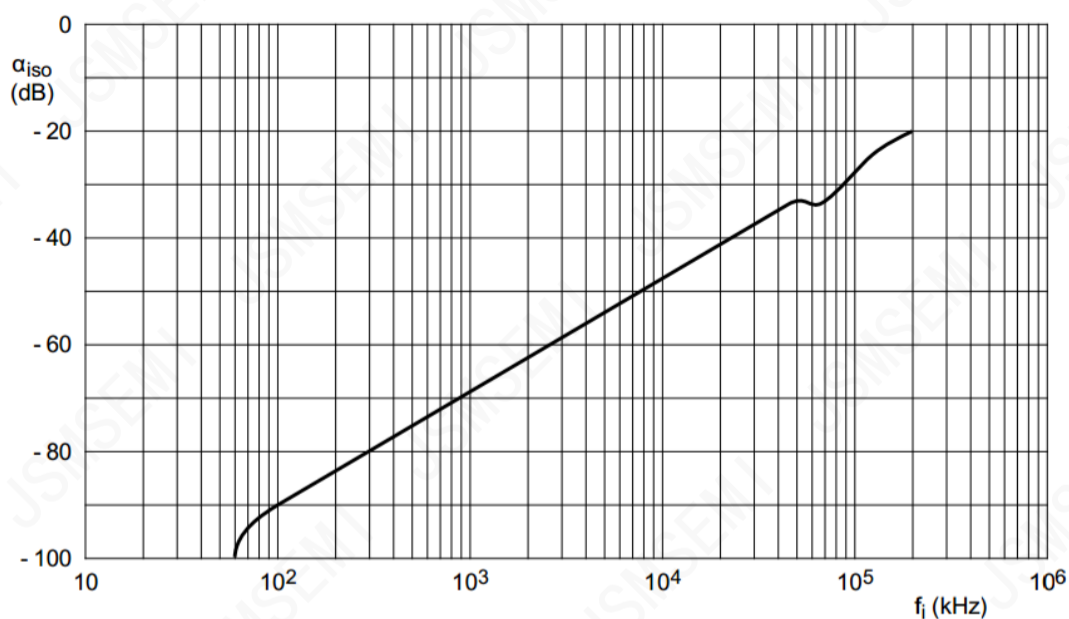


Figure 12. Test circuit for measuring sine-wave distortion



$V_{CC} = 4.5$ V; $GND = 0$ V; $V_{EE} = -4.5$ V; $R_L = 600 \Omega$; $R_S = 1$ k Ω .

a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Figure 13. Test circuit for measuring isolation (OFF-state)

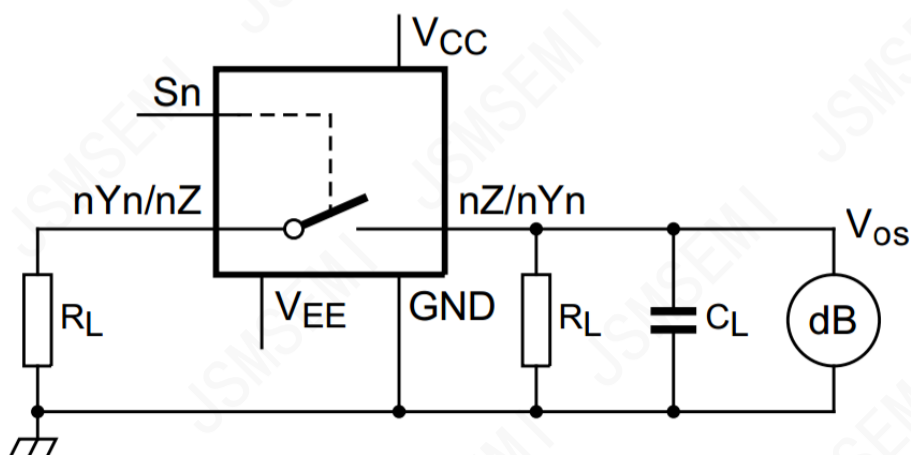
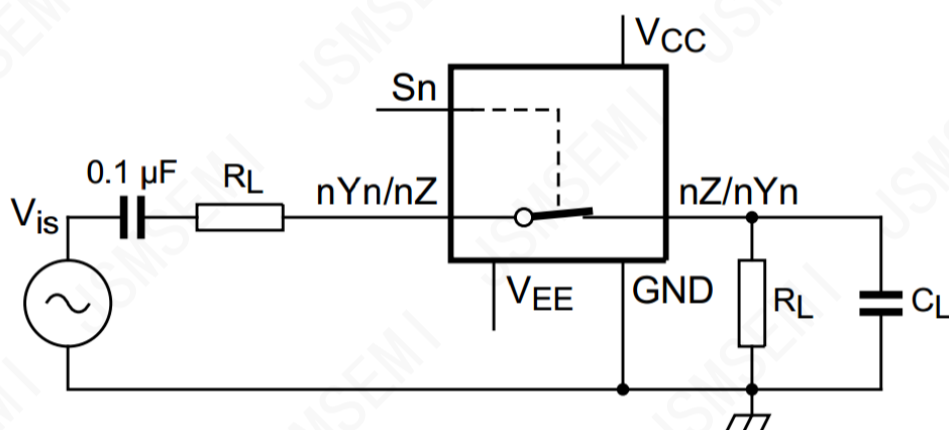


Figure 14. Test circuits for measuring crosstalk between any two switches/multiplexers

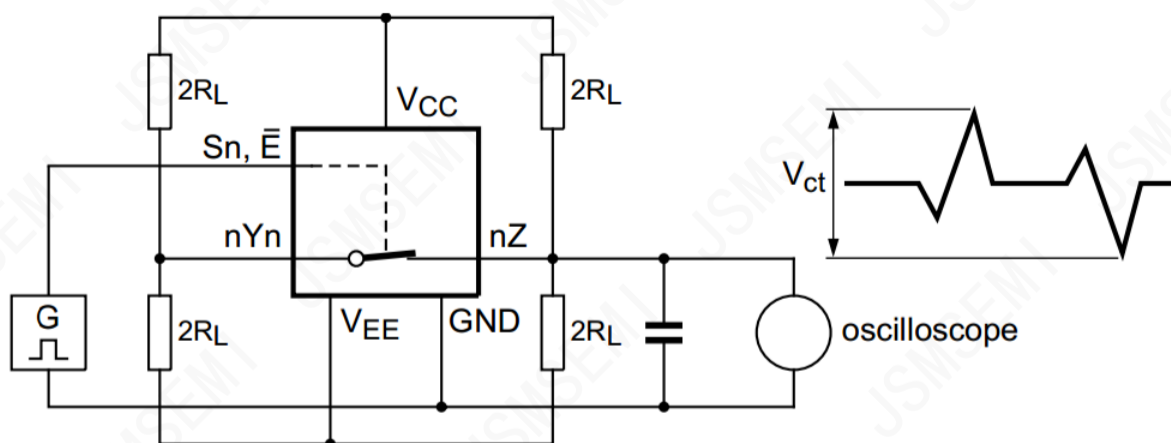
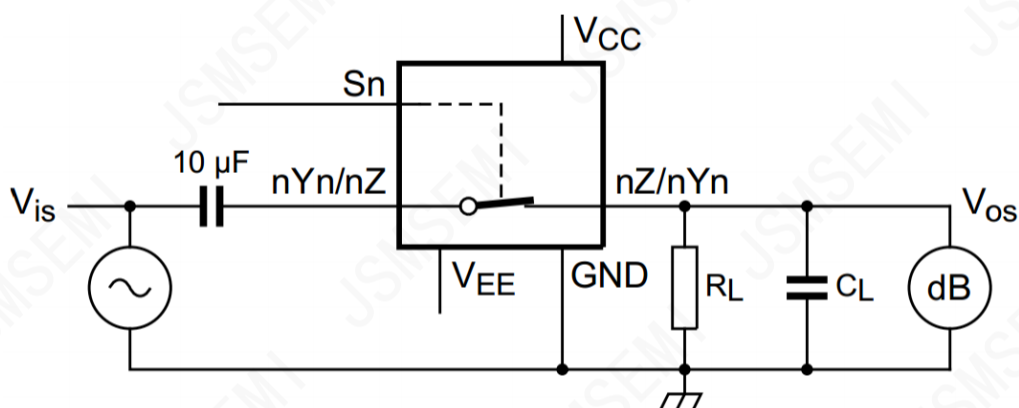
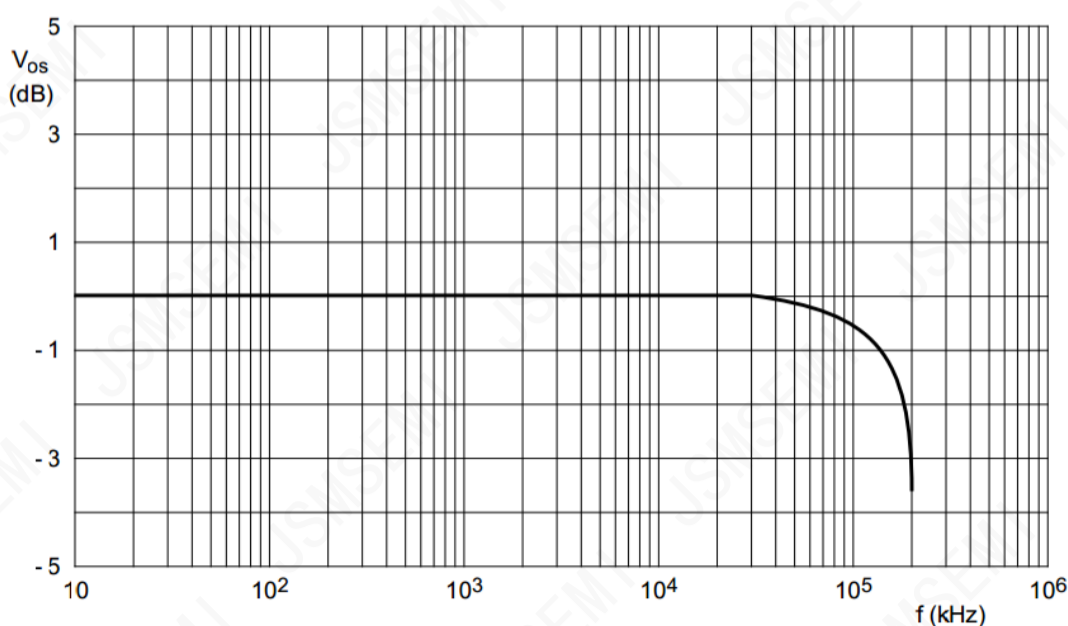


Figure 15. Test circuit for measuring crosstalk between control input and any switch



$$V_{CC} = 4.5 \text{ V}; \text{GND} = 0 \text{ V}; V_{EE} = -4.5 \text{ V}; R_L = 50 \text{ } \Omega; R_S = 1 \text{ k}\Omega$$

a. Test circuit

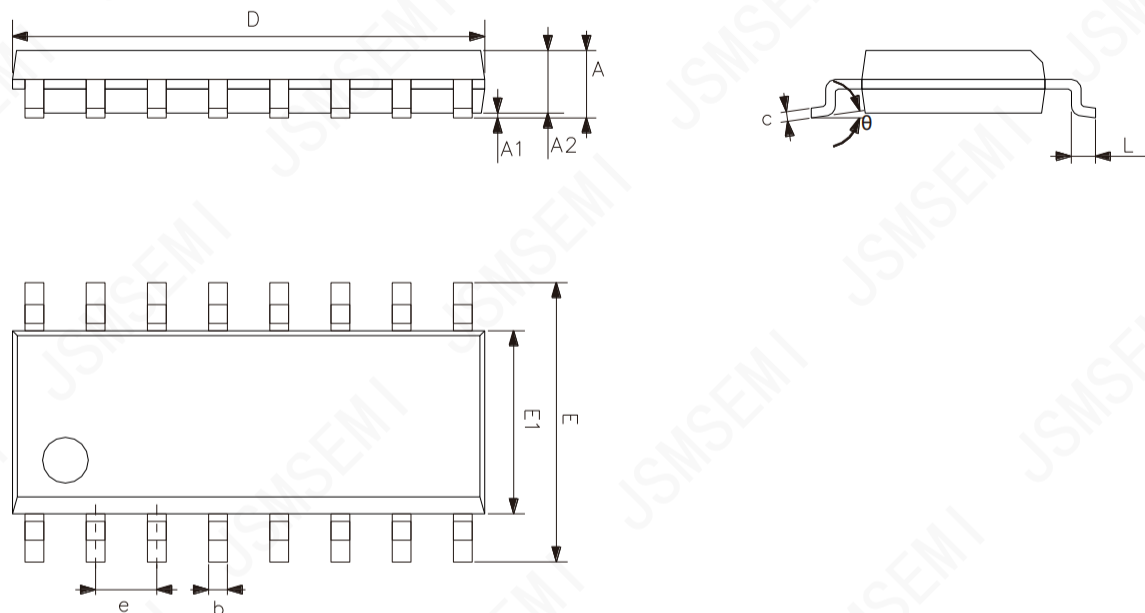


b. Typical frequency response

Figure 16. Test circuit for frequency response

5、Package Information

5.1、SOP16



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

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