Transient Voltage Suppressors for ESD Protection General Description

Specification Features:

- Ultra Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
  0.039″ x 0.024″ (1.00 mm x 0.60 mm)
- Low Body Height: 0.016″ (0.4 mm)
- Stand−off Voltage: 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000−4−2 Level 4 ESD Protection
- This is a Pb−Free Device

Mechanical Characteristics:

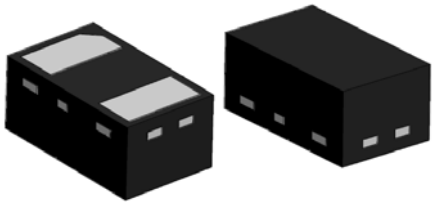
CASE: Void-free, transfer-molded, thermosetting plastic Epoxy Meets UL 94 V−0

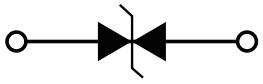
LEAD FINISH: 100% Matte Sn (Tin)

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

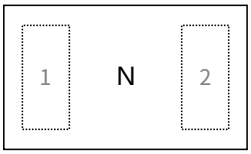
Device Meets MSL 1 Requirements

DFN1006





Package Outline



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000−4−2 (ESD) Contact Air		±10 ±15	kV
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C	P_D	150	mW
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature Range	T_J	−55 to +125	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

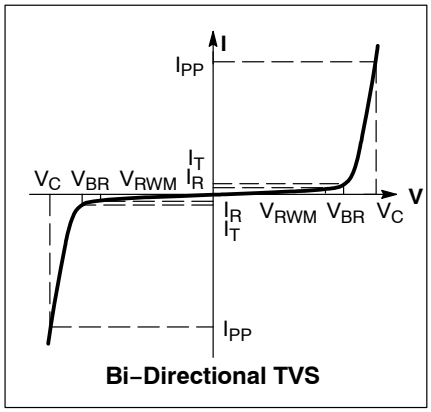
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 x 0.75 x 0.62 in.

ELECTRICAL CHARACTERISTICS
(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Typical Characteristics

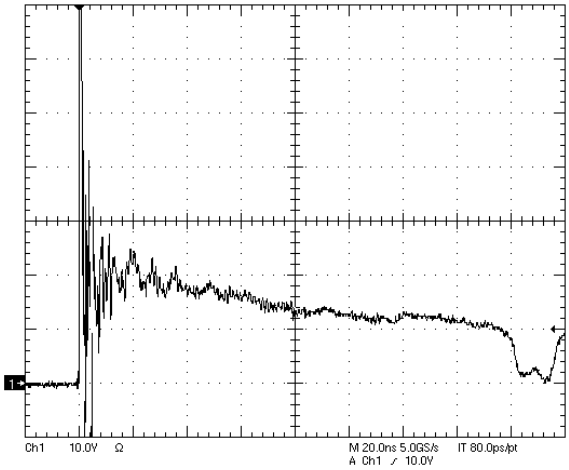


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

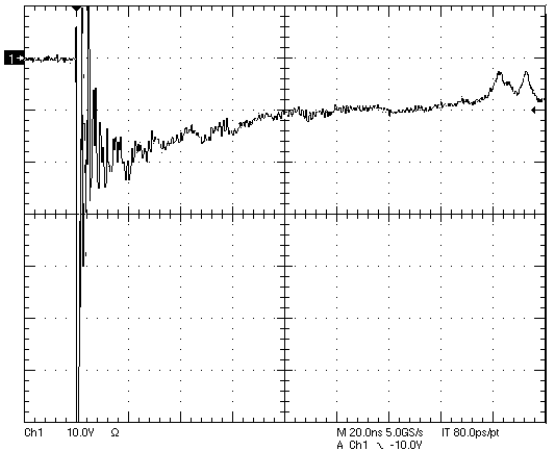


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

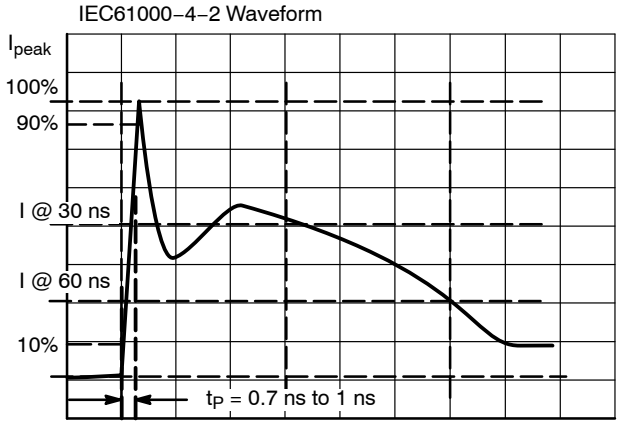


Figure 3. IEC61000−4−2 Spec

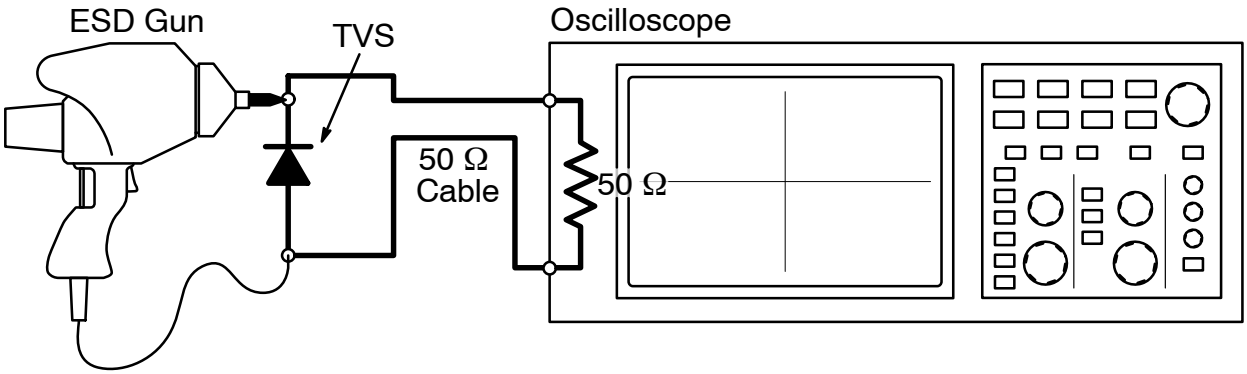


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

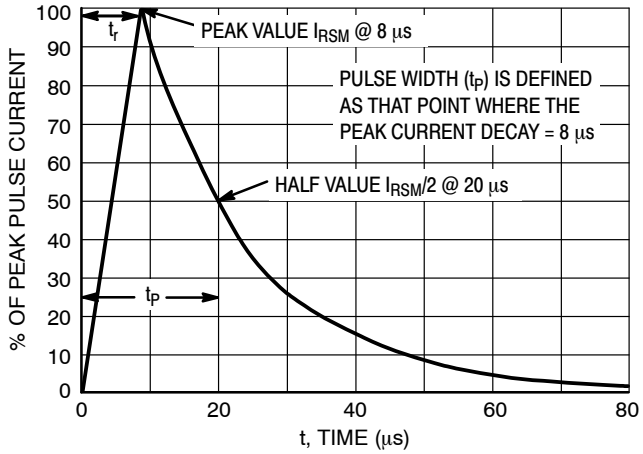
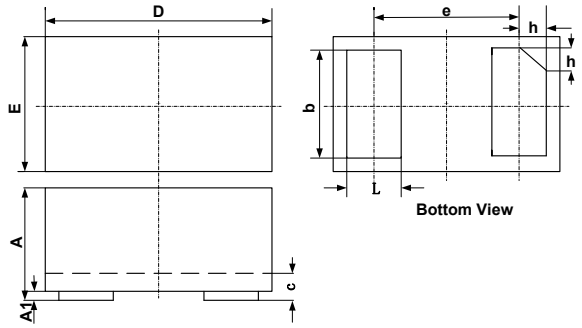


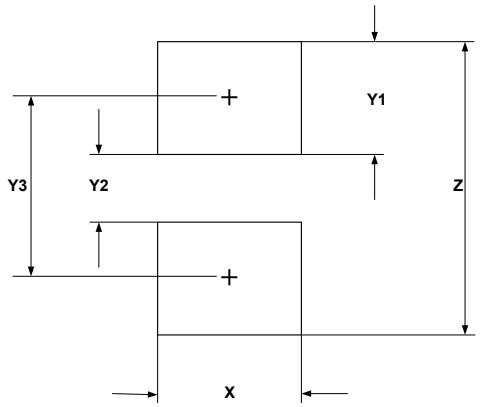
Figure 5. 8 X 20 μs Pulse Waveform

DFN1006-2L Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
c	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
e	0.65 BSC			0.026 BSC		
E	0.55	0.60	0.65	0.022	0.024	0.026
L	0.20	0.25	0.30	0.008	0.010	0.012
h	0.07	0.12	0.17	0.003	0.005	0.007

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
X	0.60	0.024
Y1	0.50	0.020
Y2	0.30	0.012
Y3	0.80	0.032
Z	1.30	0.052