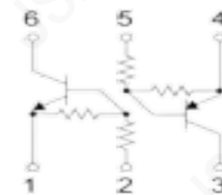
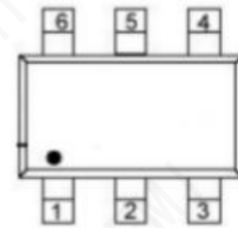


Description

The PUMD2,115-JSM is a dual digital transistor integrating NPN and PNP chips in an SOT-363 package. It features independent transistor elements to avoid interference, supports automatic mounting, and reduces both installation cost and space usage, delivering reliable switching performance for electronic circuits.



Features

- ◆ Integrates NPN and PNP chips in one package
- ◆ Independent transistor elements, no mutual interference
- ◆ Compatible with SOT-363 automatic mounting machines
- ◆ Cuts mounting cost and area by 50%
- ◆ Wide operating temperature range: -55~+150°C

Applications

- ◆ Switching circuits in consumer electronics (e.g., small appliances, wearables)
- ◆ Signal amplification in low-power electronic devices
- ◆ Driver circuits for LEDs and small motors
- ◆ Space-constrained PCB designs requiring dual-transistor functionality
- ◆ Industrial control systems with low-current switching needs

Maximum Ratings (TA=25°C)

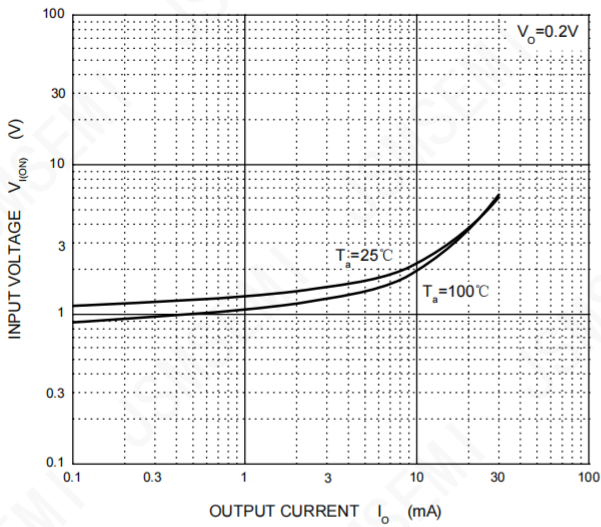
Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	50	V
Input voltage	V_{IN}	-10~40	V
Output current	I_O	30	mA
	$I_{C(MAX)}$	100	
Power dissipation	P_d	150	mW
Operation Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	°C

Electrical Characteristics (Ta=25°C unless otherwise specified)

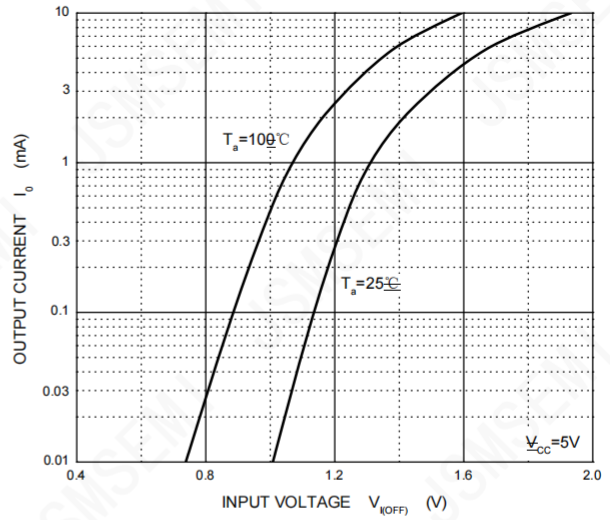
Parameter	Symbol	Min.	Typ	Max.	Unit	Conditions
Input voltage	$V_{I(off)}$	0.5			V	$V_{CC}=5V, I_O=100\mu A$
	$V_{I(on)}$			3		$V_O=0.2V, I_O=5mA$
Output voltage	$V_{O(on)}$		0.1	0.3	V	$I_O/I_I=10mA/0.5mA$
Input current	I_I			0.36	mA	$V_I=5V$
Output current	$I_{O(off)}$			0.5	μA	$V_{CC}=50V, V_I=0$
DC current gain	G_I	56				$V_O=5V, I_O=5mA$
Input resistance	R_I	15.4	22	28.6	K Ω	-
Resistance ratio	R_2/R_1	0.8	1	1.2		-
Transition frequency	f_T		250		MHz	$V_{CE}=10V, I_E=5mA, f=100MHz$

Typical Performance Curves

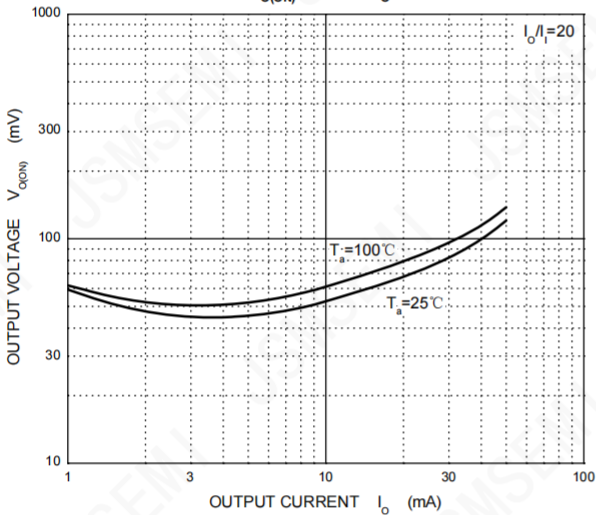
ON Characteristics



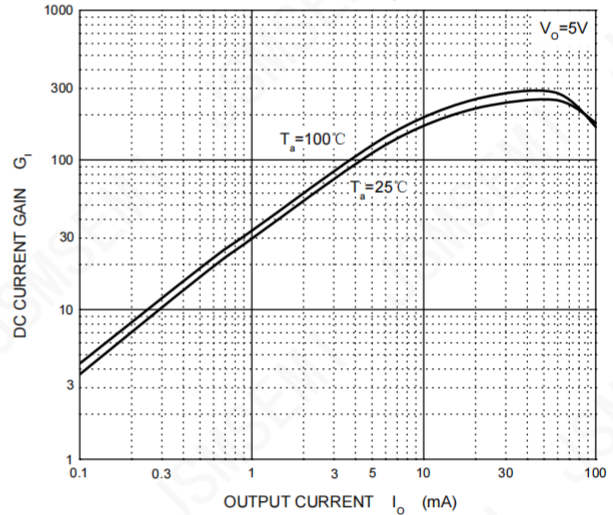
OFF Characteristics



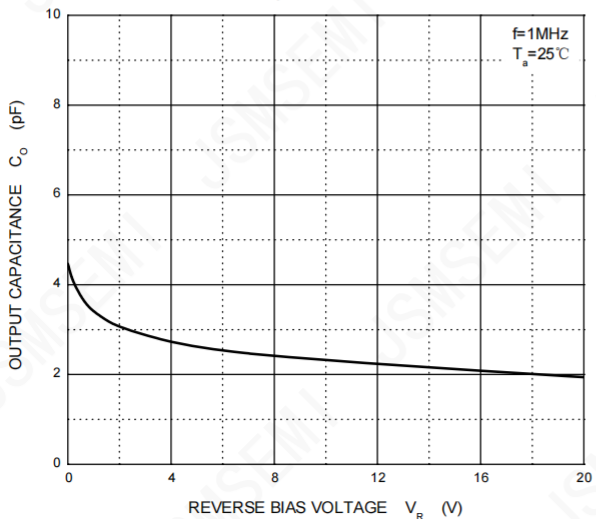
$V_{O(ON)} - I_O$



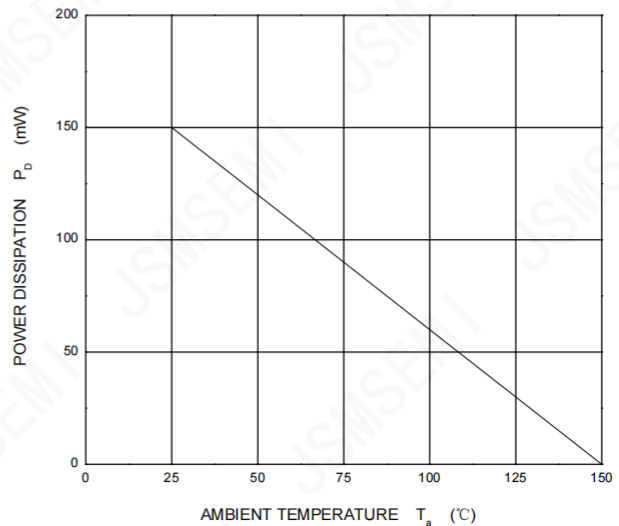
$G_I - I_O$

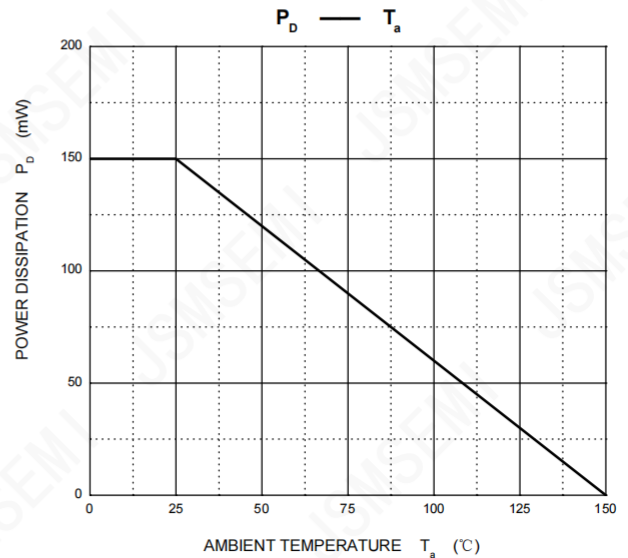
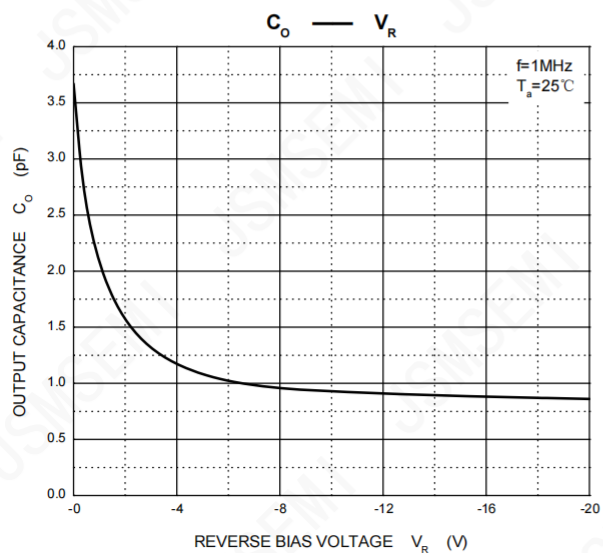
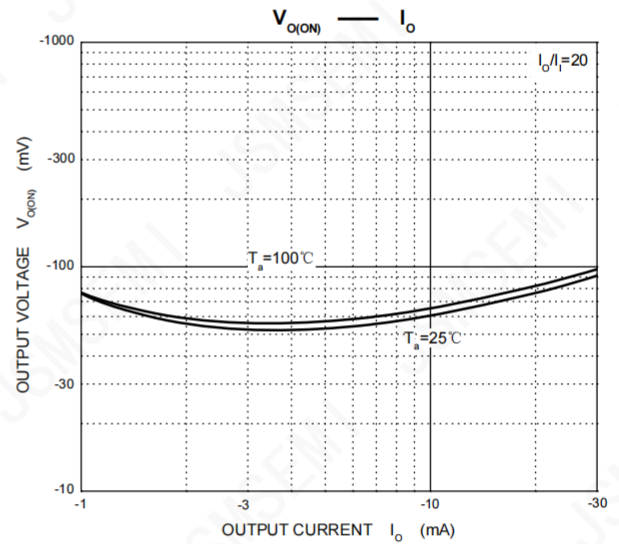
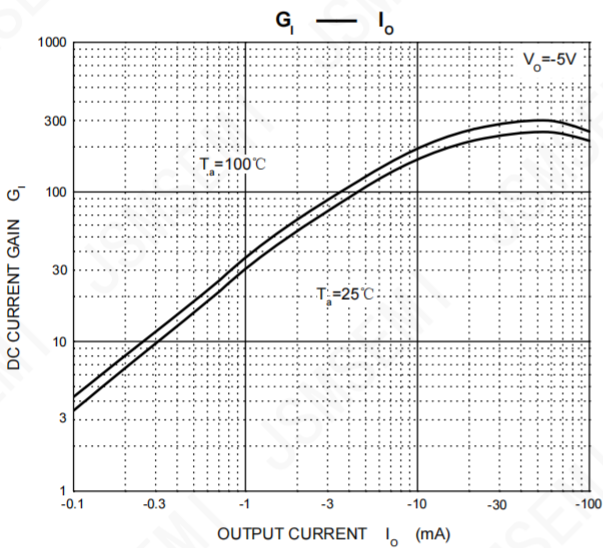
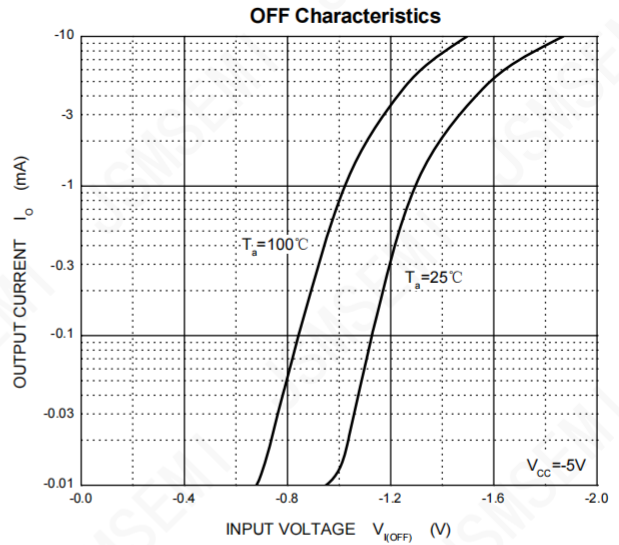
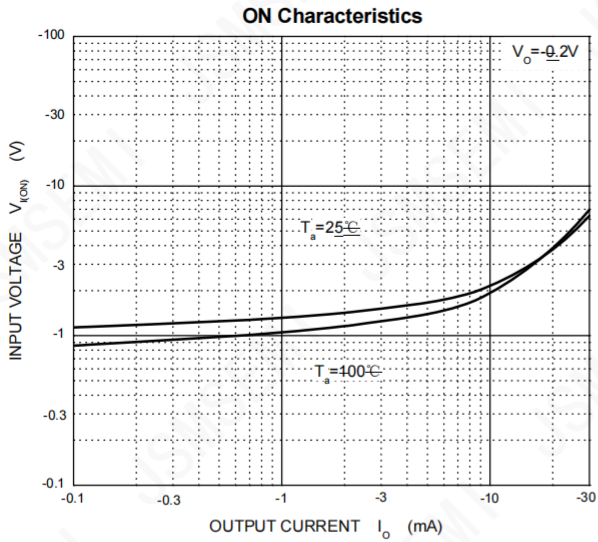


$C_O - V_R$

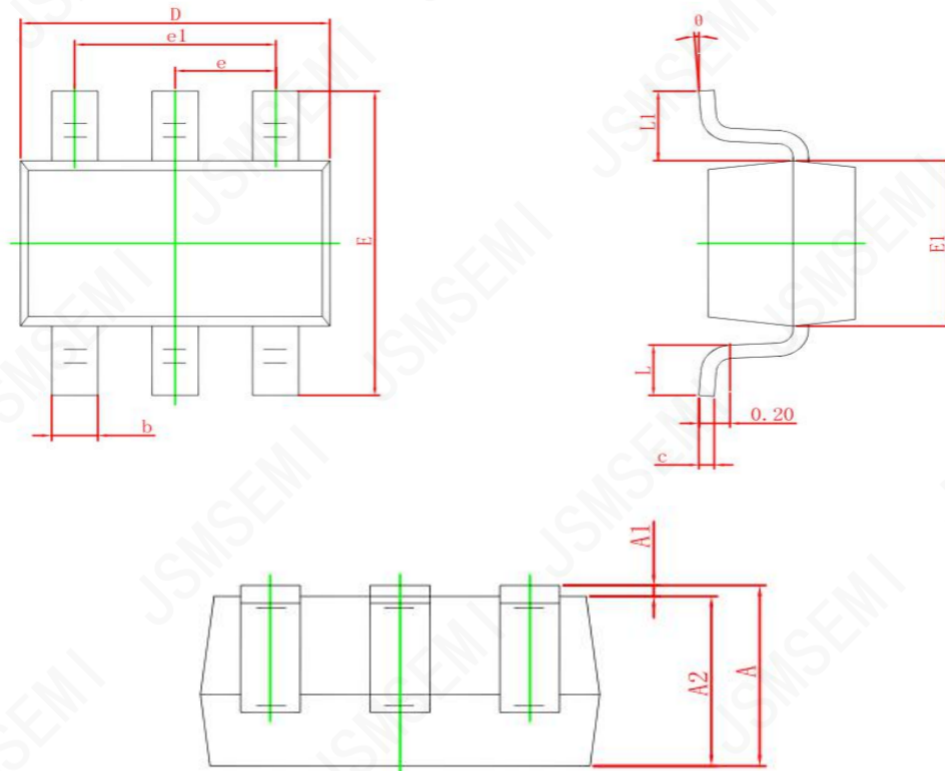


$P_D - T_a$





SOT-363 Package Outline Dimensions



Symbol	Dim in mm		
	Min	Nor	Max
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.90	0.95	1.00
b	0.15	0.25	0.35
c	0.08	0.12	0.15
D	2.05	2.10	2.25
E	2.15	2.30	2.45
E1	1.15	1.25	1.35
e	0.650TPY.		
e1	1.2	1.3	1.4
L	0.26	0.36	0.46
L1	0.525REF.		
θ	0°	4°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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