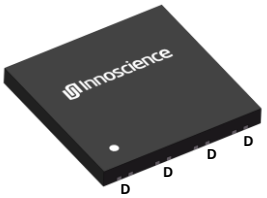
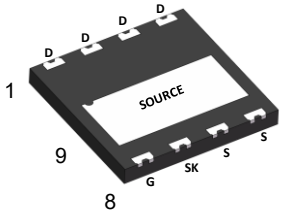
INN700D130D

1. General description

700V, 101mΩ typ., GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 8 mm × 8 mm size

2. Features

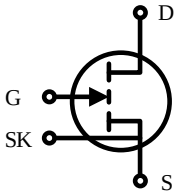




- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion



4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),typ.}$ @ V_{GS} = 6 V	101	mΩ
$R_{DS(on),max}$ @ V_{GS} = 6 V	130	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	2.65	nC
$I_{D,pulse}$	32	A
Q_{OSS} @ V_{DS} = 400 V	25.5	nC
Q_{rr} @ V_{DS} = 400 V	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1, 2, 3, 4	7	5, 6, 9

Table 3 Ordering information

Type/Ordering Code	Package	Product Code	Carrier	Package base Qty
INN700D130D	DFN8X8	70D130D	Tape & Reel	2500

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6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS, max}$	700	V	V_{GS} = 0 V, T_j = -55 °C to 150 °C
Drain source voltage transient [1]	$V_{DS, transient}$	800	V	V_{GS} = 0 V
Drain source voltage, pulsed [2]	$V_{DS, pulse}$	750	V	T_j = 25 °C; total time < 10 h
				T_j = 125 °C; total time < 1 h
Continuous current, drain source	I_D	17	A	T_c = 25 °C
Pulsed current, drain source [3]	$I_{D, pulse}$	32	A	T_c = 25 °C; V_{GS} = 6 V; t_{PULSE} = 10 µs
Pulsed current, drain source [3]	$I_{D, pulse}$	18	A	T_c = 125 °C; V_{GS} = 6 V; t_{PULSE} = 10 µs
Gate source voltage, continuous [4]	V_{GS}	-1.4 to +7	V	T_j = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS, pulse}$	-20 to +10	V	T_j = -55 °C to 150 °C; f = 100 kHz; open drain, t_{PULSE} = 50 ns, total time<50s
Power dissipation	P_{tot}	85	W	T_c = 25 °C
Operating temperature	T_j	-55 to +150	˚C	
Storage temperature	T_{stg}	-55 to +150	˚C	

1. $V_{DS, transient}$ is intended for non-repetitive events, t_{PULSE} < 200 µs.
2. $V_{DS, pulse}$ is intended for repetitive pulse, t_{PULSE} < 100 ns.
3. Limit was extracted from characterization test, not measured during production.
4. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10.

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA} [1]	66.72	°C/W	
Thermal resistance, junction-case	R_{thJC}	1.47	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	MSL3

1.R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

8. Electric characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.5	V	I_D = 14.3 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.5	-		I_D = 14.3 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	0.6	37.5	μA	V_{DS} = 700 V; V_{GS} = 0 V; T_j = 25 °C
		-	4	-		V_{DS} = 700 V; V_{GS} = 0 V; T_j = 125 °C
Gate-source leakage current	I_{GSS}	-	40	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	101	130	mΩ	V_{GS} = 6 V; I_D = 0.5 A; T_j = 25 °C
			101			V_{GS} = 6 V; I_D = 5 A; T_j = 25 °C
		-	202	-	mΩ	V_{GS} = 6 V; I_D = 5 A; T_j = 125 °C
Gate resistance	R_G	-	8	-	Ω	f = 5 MHz; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	101	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	36.5	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer Capacitance	C_{rss}	-	0.4	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	49	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	65	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	25.5	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V

1. $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.

2. $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2.65	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D= 5 A
Gate-source charge	Q_{GS}	-	0.22	-	nC	
Gate-drain charge	Q_{GD}	-	1.02	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.1	-	V	V_{DS} = 400 V; I_D= 5 A

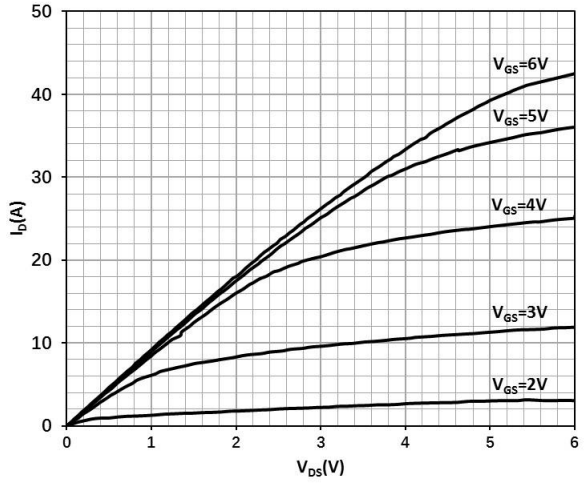
Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.4	-	V	V_{GS} = 0 V; I_S = 5 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	-	32	A	V_{GS} = 6 V; t_{PULSE} = 10 µs
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_S = 5 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

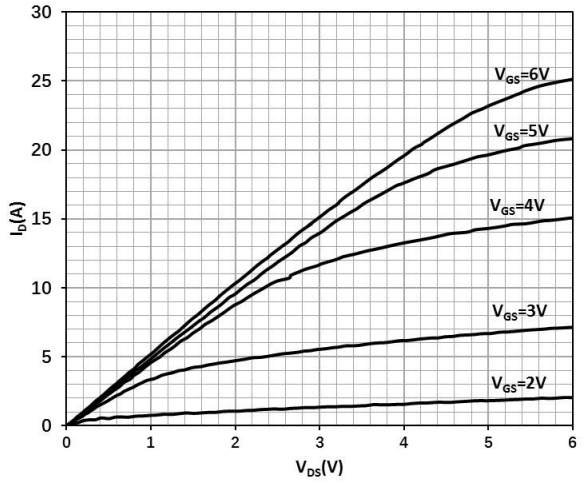
at T_j = 25 °C, unless specified otherwise

Figure 1 Typ. output characteristics



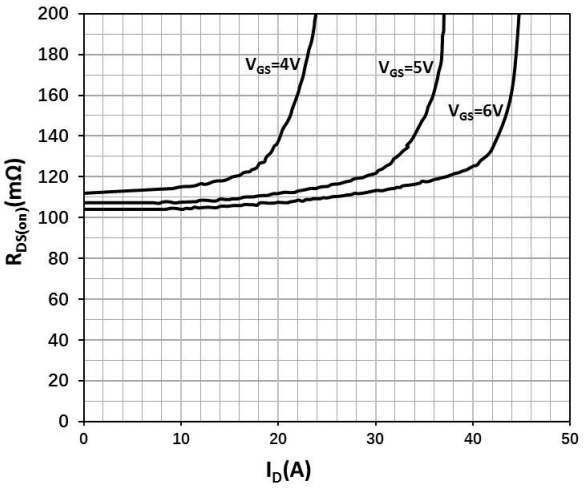
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C, T_{Pulse}=10us, Duty=0.001%

Figure 2 Typ. output characteristics



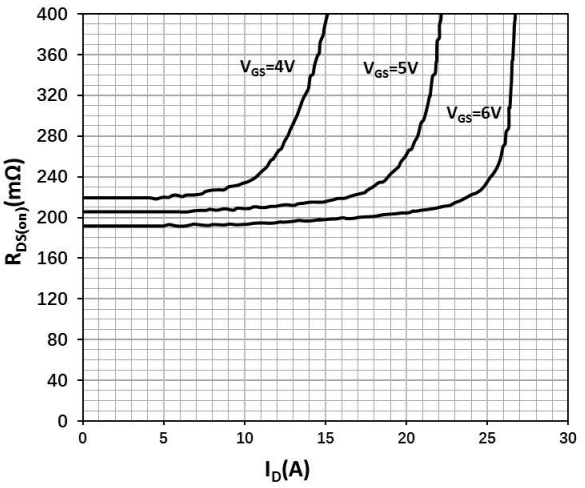
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C, T_{Pulse}=10us, Duty=0.001%

Figure 3 Typ. Drain-source on-state resistance



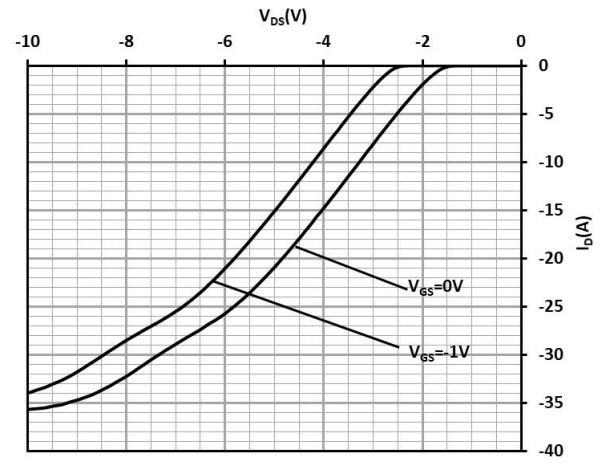
$R_{DS(on)} = f(I_D,V_{GS})$; T_j = 25 °C, T_{Pulse}=10us, Duty=0.001%

Figure 4 Typ. Drain-source on-state resistance



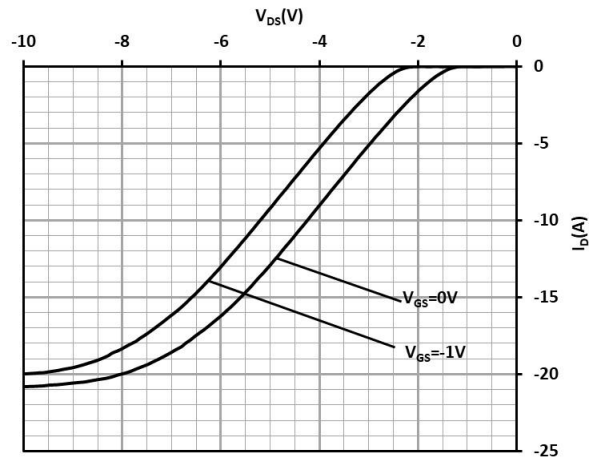
$R_{DS(on)} = f(I_D,V_{GS})$; T_j = 125 °C, T_{Pulse}=10us, Duty=0.001%

Figure 5 Typ. channel reverse characteristics



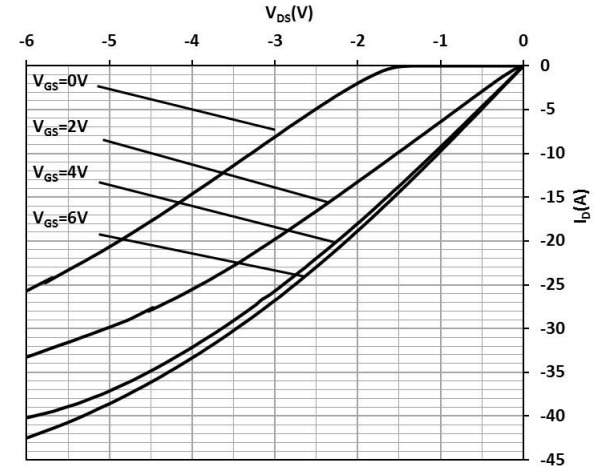
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C, T_{Pulse}=10us, Duty=0.001%

Figure 6 Typ. channel reverse characteristics



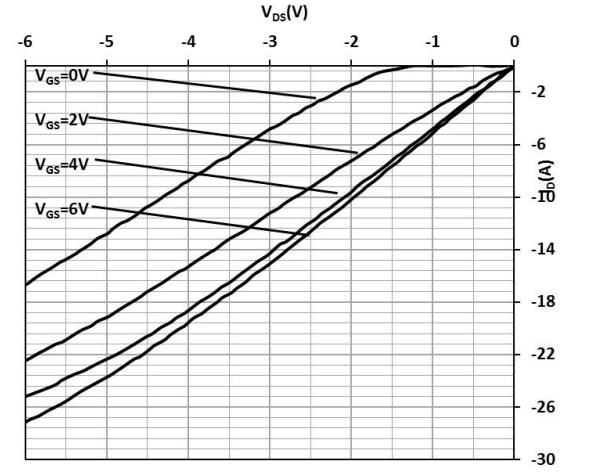
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C, T_{Pulse}=10us, Duty=0.001%

Figure 7 Typ. channel reverse characteristics



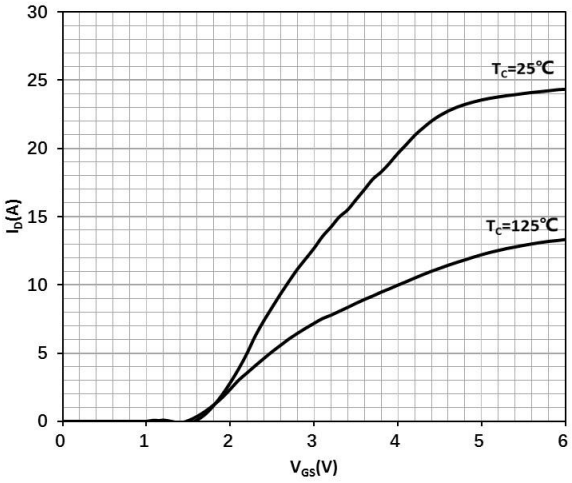
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C, T_{Pulse}=10us, Duty=0.001%

Figure 8 Typ. channel reverse characteristics



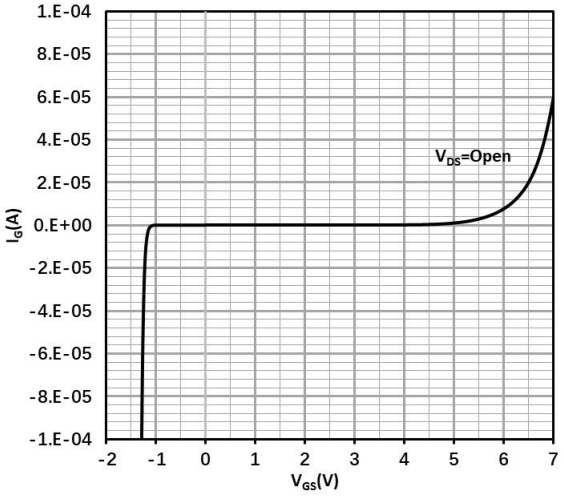
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C, T_{Pulse}=10us, Duty=0.001%

Figure 9 Typ. transfer characteristics



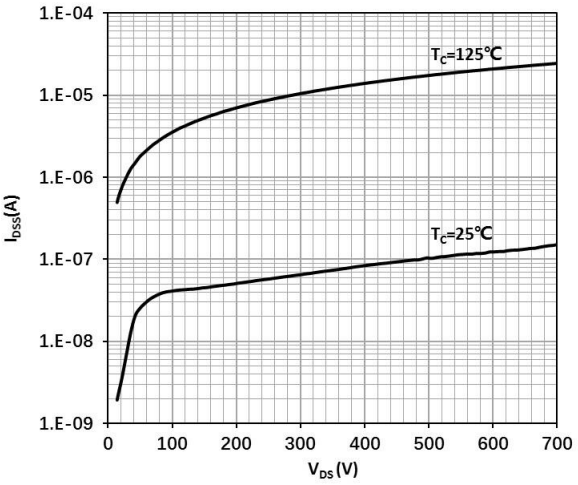
$I_D = f(V_{GS})$; V_{DS}= 3 V, T_{Pulse}=10us, Duty=0.001%

Figure 10 Typ. Gate-to-Source leakage



$I_G = f(V_{GS})$; I_G reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

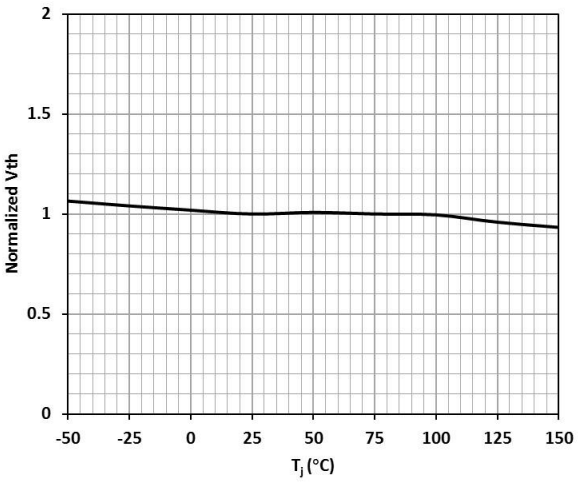
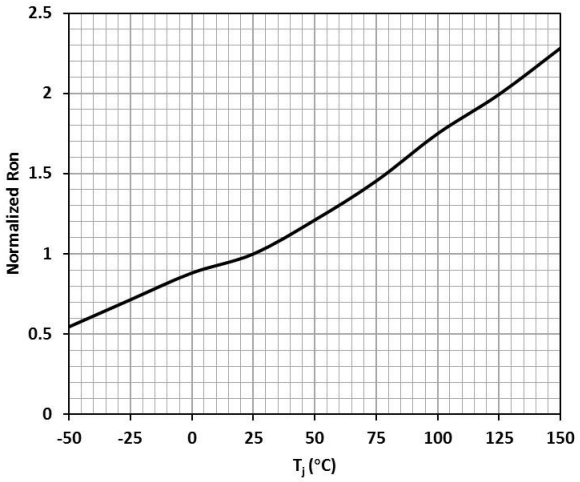
Figure 12 Gate threshold voltage	Figure 13 Drain-source on-state resistance
	
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 14.3mA	$R_{DS(on)} = f(T_j)$; I_D = 5 A; V_{GS}=6V, Duty=0.001%

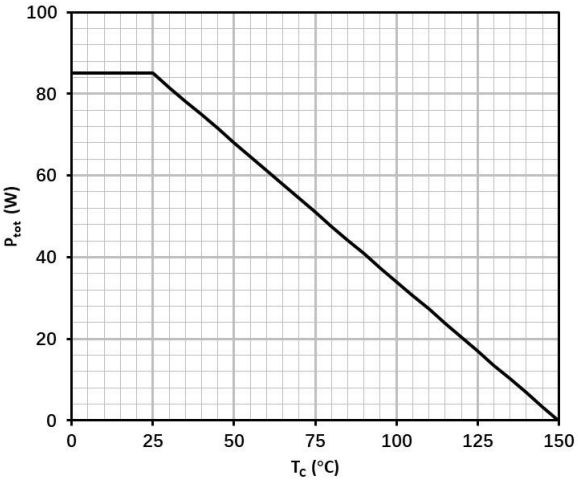
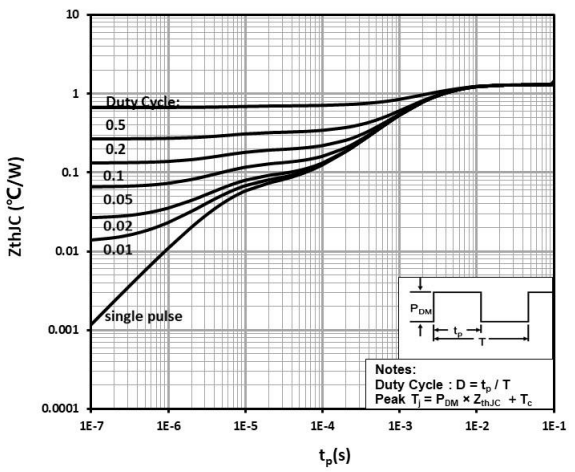
Figure 14 Power dissipation	Figure 15 Max.transient thermal impedance
	
$P_{tot} = f(T_C)$	$Z_{thJC} = f(t_P, D)$

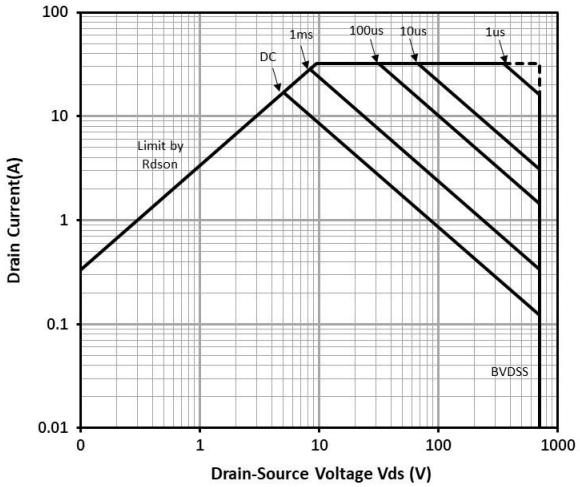
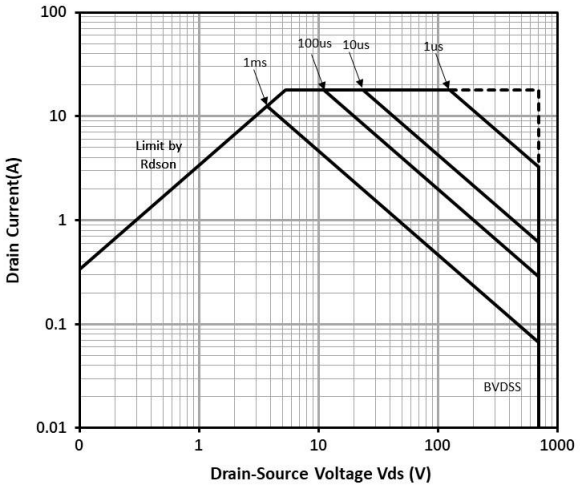
Figure 16 Safe operating area	Figure 17 Safe operating area
	
$I_D = f(V_{DS})$; $T_C = 25$ °C, Duty=0	$I_D = f(V_{DS})$; $T_C = 125$ °C, Duty=0

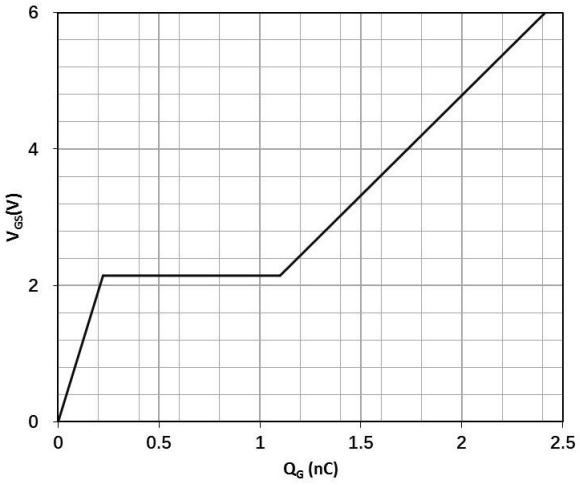
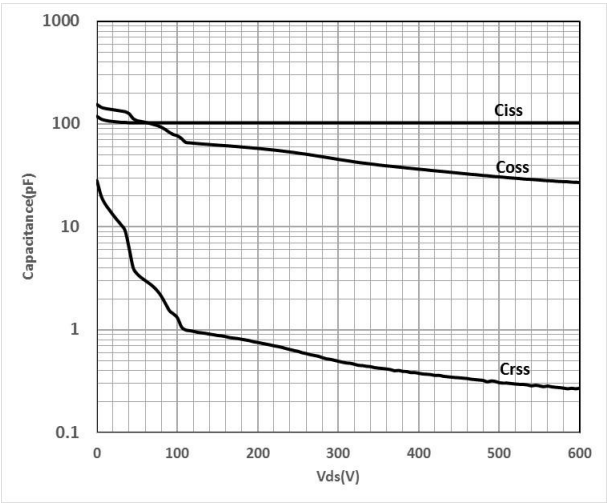
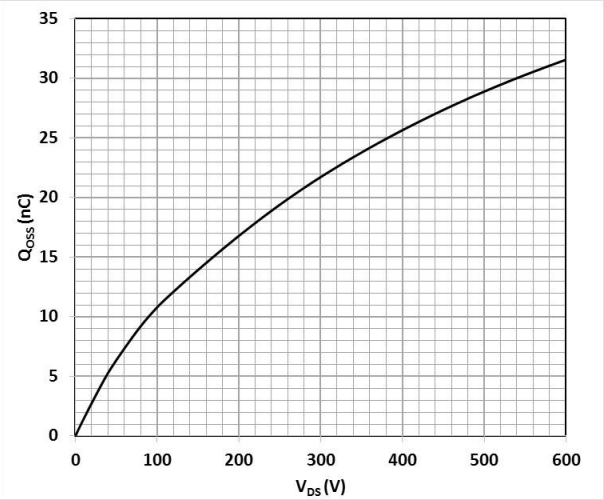
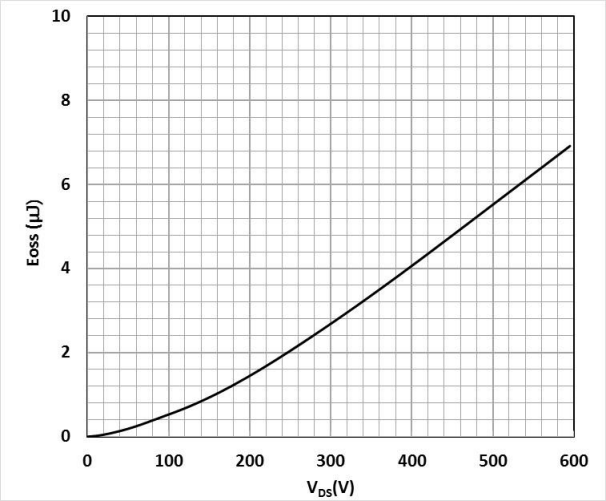
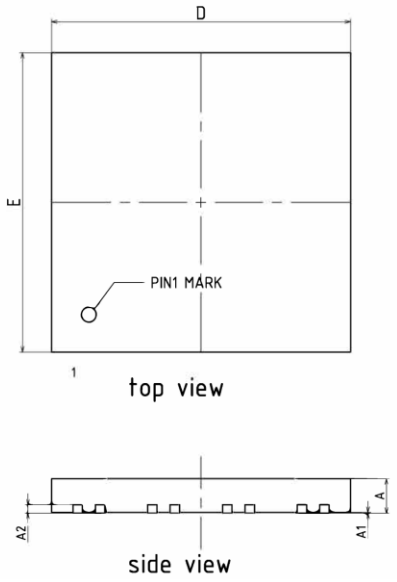
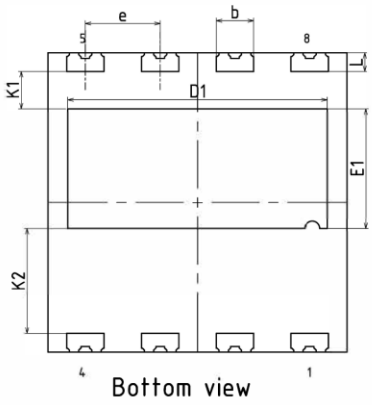
Figure 18 Typ. gate charge	Figure 19 Typ. capacitances
	
$V_{GS} = f(Q_G)$; $V_{DCLINK} = 400$ V; $I_D = 5$ A	$C_{XSS} = f(V_{DS})$; Freq. = 100 kHz

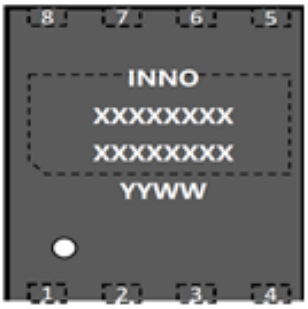
Figure 20 Typ. output charge	Figure 21 Typ. C_{OSS} stored Energy
	
Q_{OSS} = f(V_{DS}); Freq. = 100 kHz	E_{OSS} = f(V_{DS}); Freq. = 100 kHz

10. Package outlines





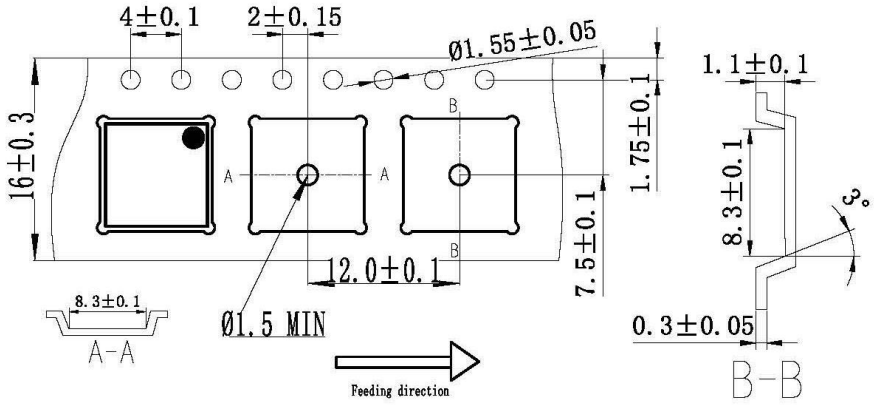
SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.203REF	
b	0.95	1.00	1.05
D	7.90	8.00	8.10
D1	6.84	6.94	7.04
E	7.90	8.00	8.10
E1	3.10	3.20	3.30
K1	0.90	1.00	1.10
K2	2.70	2.80	2.90
e		2.00 BSC	
L	0.40	0.50	0.60



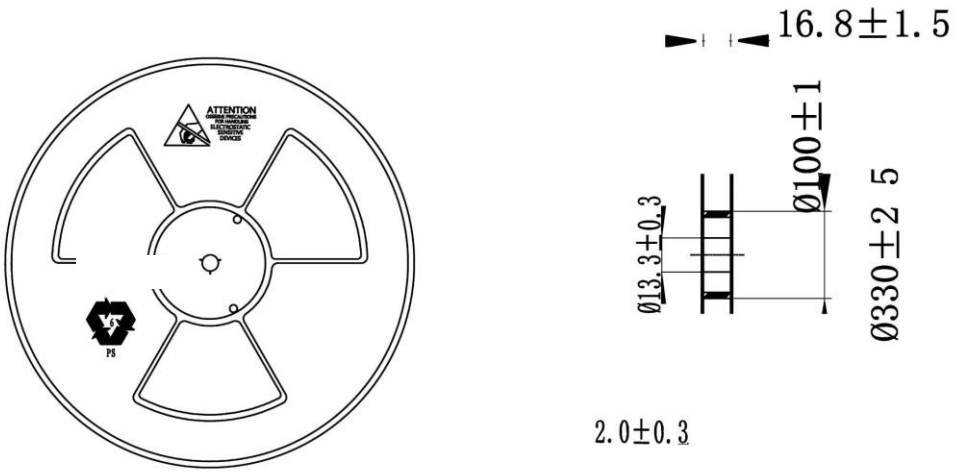
Row	Description	Example
Row1	Company name	INNO
Row2	Product code (In short)	XXXXXXXX
Row3	ASSY lot No.	XXXXXXXX
Row4	Date code	YYWW

Notes:
(1) Dimension and tolerance conform to ASME Y14.5-2009.
(2) All dimension are in millimeters.
(3) Lead coplanarity shall be 0.1 millimeters max.
(4) Complies with JEDEC MO-229.
(5) Drawing is not to scale.
(6) Dimensions do not include mold protrusion.
(7) Package outline exclusive of metal burr dimensions.

11. Reel information

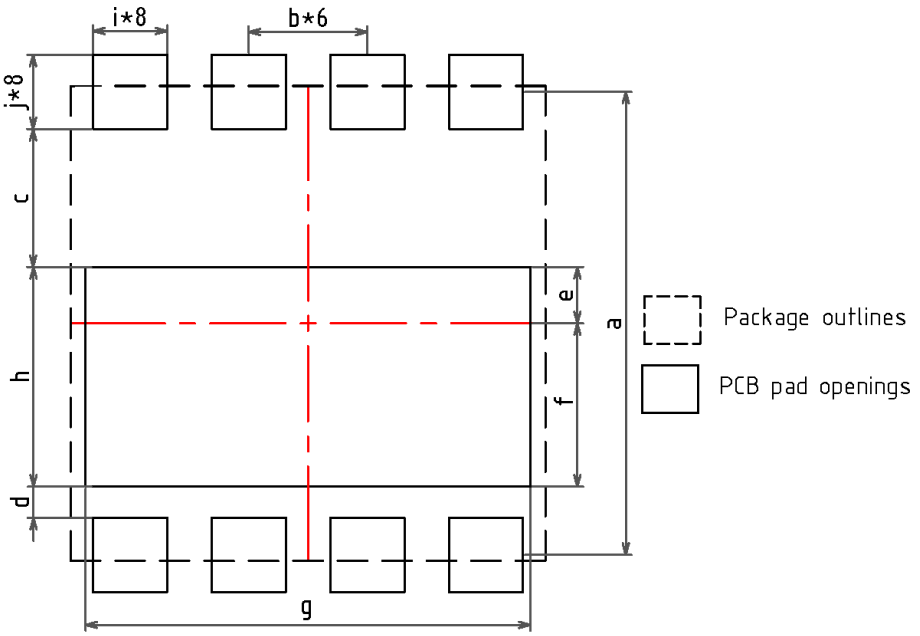


1.The cumulative error of any 10 sprocket holes shall not exceed ±0.2mm;
2.The materail thickness shall be mesured based on the edge of the carrier tape;
3. The unspecified tolerrance is ±0.1mm, and R<0.3mm is not specified
4. The unmarked demolding slope is 5°;
5. Surface resistivity: 1e5 Ω/△~1*11e11



1.The surface of tape should be smooth, clean, and free of injection molding defects, abd there should be no significant burrs;
2. Material surface resistivity: 1e5 Ω/△~10e11 Ω/△
3.Unspecified tolerrance :±0.3mm

12. Recommended PCB footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	7.800	f	2.750
b	2.000	g	7.500
c	2.325	h	3.700
d	0.525	i	1.400
e	0.950	j	1.250

Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale.

Important Notice

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