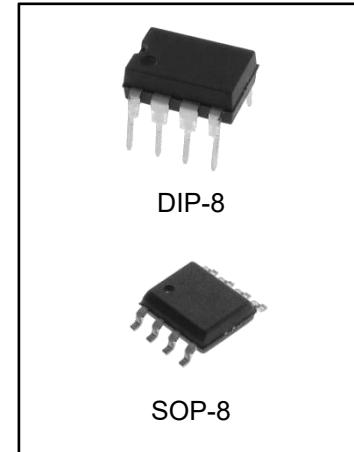


## 3.3-V RS-485 TRANSCEIVERS

### FEATURES

- Operates With a 3.3-V Supply
- Bus-Pin ESD Protection Exceeds 16 kV HBM
- 1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)
- Optional Driver Output Transition Times for Signaling Rates (1) of 1 Mbps, 10 Mbps, and 32 Mbps
- Meets or Exceeds the Requirements of ANSI TIA/EIA-485-A
- Bus-Pin Short Circuit Protection From -7 V to 12 V
- Low-Current Standby Mode . . . 1  $\mu$ A Typical
- Open-Circuit, Idle-Bus, and Shorted-Bus Failsafe Receiver
- Thermal Shutdown Protection
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications



### ORDERING INFORMATION

DEVICE	PACKAGE TYPE	MARKING	PACKING	PACKING QTY
HX65HVD10EIPG	DIP-8	HVD10EI	TUBE	2000pcs/box
HX65HVD11EIPG	DIP-8	HVD11EI	TUBE	2000pcs/box
HX65HVD12EIPG	DIP-8	HVD12EI	TUBE	2000pcs/box
HX65HVD10EIDRG	SOP-8	HVD10EI	REEL	2500pcs/reel
HX65HVD11EIDRG	SOP-8	HVD11EI	REEL	2500pcs/reel
HX65HVD12EIDRG	SOP-8	HVD12EI	REEL	2500pcs/reel
HX65HVD10EIDRG4	SOP-8	HVD10EI	REEL	4000pcs/reel
HX65HVD11EIDRG4	SOP-8	HVD11EI	REEL	4000pcs/reel
HX65HVD12EIDRG4	SOP-8	HVD12EI	REEL	4000pcs/reel

### DESCRIPTION

The HX65HVD10, HX65HVD11, and HX65HVD12, combine a 3-state differential line driver and differential input line receiver that operate with a single 3.3-V power supply. They are designed for balanced transmission lines and meet or exceed ANSI standard TIA/EIA-485-A and ISO 8482:1993.

These differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines.

The drivers and receivers have active-high and active-low enables respectively, that can be externally connected together to function as direction control.

Very low device standby supply current can be achieved by disabling the driver and the receiver.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or VCC = 0. These parts feature wide positive and negative common-mode voltage ranges, making them suitable for party-line applications.

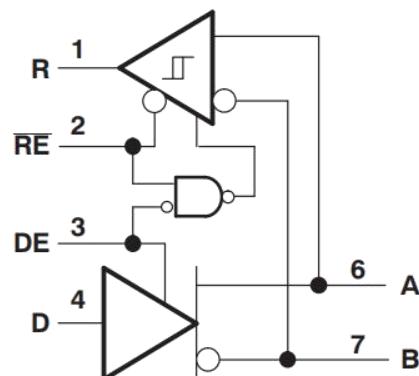
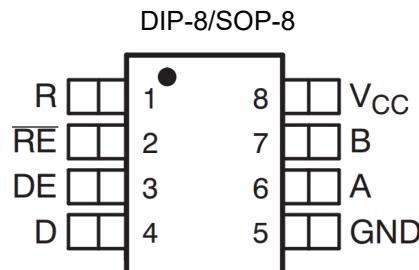
### APPLICATIONS

- Digital Motor Control
- Utility Meters

- Chassis-to-Chassis Interconnects
- Electronic Security Stations
- Industrial Process Control

- Building Automation
- Point-of-Sale (POS) Terminals and Networks

## PIN CONNECTION



(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1) (2)

		<b>UNIT</b>
V <sub>CC</sub>	Supply voltage range	-0.3 V to 6 V
Voltage range at A or B		-9 V to 14 V
Input voltage range at D, DE, R or RE		-0.5 V to V <sub>CC</sub> + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω, see Figure 11		-50 V to 50 V
I <sub>O</sub>	Receiver output current	-11 mA to 11 mA
Electrostatic discharge	Human body model <sup>(3)</sup>	±16 kV
	All pins	±4 kV
	Charged-device model <sup>(4)</sup>	±1 kV
Continuous total power dissipation		See Dissipation Rating Table
Electrical Fast Transient/Burst <sup>(5)</sup>	A, B, and GND	±4 kV
T <sub>J</sub>	Junction temperature	170°C
Lead Temperature (Soldering, 10 seconds)		245°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A and IEC 60749-26.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

(5) Tested in accordance with IEC 61000-4-4.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		3	3.6		V
V <sub>I</sub> or V <sub>IC</sub>	Voltage at any bus terminal (separately or common mode)		-7(1)	12		
V <sub>IH</sub>	High-level input voltage	D, DE, RE	2		V <sub>CC</sub>	
V <sub>IL</sub>	Low-level input voltage	D, DE, RE	0	0.8		
V <sub>ID</sub>	Differential input voltage	Figure 7	-12	12		
I <sub>OH</sub>	High-level output current	Driver		-60		mA
		Receiver		-8		
I <sub>OL</sub>	Low-level output current	Driver		60		mA
		Receiver		8		
R <sub>L</sub>	Differential load resistance		54	60		Ω
C <sub>L</sub>	Differential load capacitance		50			pF
Signaling rate		HVD10		32		Mbps
		HVD11		10		
		HVD12		1		
T <sub>J</sub> (2)	Junction temperature			145		°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) See thermal characteristics table for information regarding this specification.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -18 mA	-1.5			V
V <sub>OD</sub>	Differential output voltage <sup>(2)</sup>	I <sub>O</sub> = 0	2	V <sub>CC</sub>		V
		R <sub>L</sub> = 54 Ω, See Figure 1	1.5			
		V <sub>test</sub> = -7 V to 12 V, See Figure 2	1.5			
Δ V <sub>OD</sub>	Change in magnitude of differential output voltage	See Figure 1 and Figure 2	-0.2	0.2		V
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output voltage	See Figure 3		400		mV
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage		1.4	2.5		V
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage		-0.05	0.05		V
I <sub>OZ</sub>	High-impedance output current	See receiver input currents				
I <sub>I</sub>	Input current	D		-100	0	μA
		DE		0	100	
I <sub>OS</sub>	Short-circuit output current	-7 V ≤ V <sub>O</sub> ≤ 12 V	-250	250		mA
C <sub>(OD)</sub>	Differential output capacitance	V <sub>OD</sub> = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		16		pF
I <sub>CC</sub>	Supply current	RE at V <sub>CC</sub> , D & DE at V <sub>CC</sub> , No load	Receiver disabled and driver enabled	9	15.5	mA
		RE at V <sub>CC</sub> , D at V <sub>CC</sub> , DE at 0 V, No load	Receiver disabled and driver disabled (standby)	1	5	
		RE at 0 V, D & DE at V <sub>CC</sub> , No load	Receiver enabled and driver enabled	9	15.5	

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) For TA > 85°C, V<sub>CC</sub> is ±5%.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	HVD10 HVD11 HVD12		5	8.5	16
				18	25	40
				135	200	300
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	HVD10 HVD11 HVD12		5	8.5	16
				18	25	40
				135	200	300
t <sub>r</sub>	Differential output signal rise time	HVD10 HVD11 HVD12	R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF, See Figure 4	3	4.5	10
				10	20	30
				100	170	300
t <sub>f</sub>	Differential output signal fall time	HVD10 HVD11 HVD12		3	4.5	10
				10	20	30
				100	170	300
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )	HVD10 HVD11 HVD12			1.5	
					2.5	
					7	
t <sub>sk(pp)</sub> <sup>(2)</sup>	Part-to-part skew	HVD10 HVD11 HVD12			6	
					11	
					100	
t <sub>PZH</sub>	Propagation delay time, high-impedance-to-high-level output	HVD10 HVD11 HVD12			31	
					55	
					300	
t <sub>PHZ</sub>	Propagation delay time, high-level-to-high-impedance output	HVD10 HVD11 HVD12	R <sub>L</sub> = 110 Ω, RE at 0 V, See Figure 5		25	
					55	
					300	
t <sub>PZL</sub>	Propagation delay time, high-impedance-to-low-level output	HVD10 HVD11 HVD12			26	
					55	
					300	
t <sub>PLZ</sub>	Propagation delay time, low-level-to-high-impedance output	HVD10 HVD11 HVD12	R <sub>L</sub> = 110 Ω, RE at 0 V, See Figure 6		26	
					75	
					400	
t <sub>PZH</sub>	Propagation delay time, standby-to-high-level output		R <sub>L</sub> = 110 Ω, RE at 3 V, See Figure 5		6	μs
t <sub>PZL</sub>	Propagation delay time, standby-to-low-level output		R <sub>L</sub> = 110 Ω, RE at 3 V, See Figure 6		6	μs

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) t<sub>sk(pp)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

**RECEIVER ELECTRICAL CHARACTERISTICS**

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT		
V <sub>IT+</sub> Positive-going input threshold voltage	I <sub>O</sub> = -8 mA		-0.065	-0.01		V		
V <sub>IT-</sub> Negative-going input threshold voltage					-0.2	-0.1		
V <sub>hys</sub> Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )			35			mV		
V <sub>IK</sub> Enable-input clamp voltage	I <sub>I</sub> = -18 mA		-1.5			V		
V <sub>OH</sub> High-level output voltage	V <sub>ID</sub> = 200 mV, I <sub>OH</sub> = -8 mA, See Figure 7		2.4			V		
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -200 mV, I <sub>OL</sub> = 8 mA, See Figure 7		0.4			V		
I <sub>OZ</sub> High-impedance-state output current	V <sub>O</sub> = 0 or V <sub>CC</sub> RE at V <sub>CC</sub>		-1	1		µA		
I <sub>I</sub> Bus input current	V <sub>A</sub> or V <sub>B</sub> = 12 V		HVD11, HVD12, Other input at 0 V	0.05	0.11	mA		
	V <sub>A</sub> or V <sub>B</sub> = 12 V, V <sub>CC</sub> = 0 V			0.06	0.13			
	V <sub>A</sub> or V <sub>B</sub> = -7 V			-0.1	-0.05			
	V <sub>A</sub> or V <sub>B</sub> = -7 V, V <sub>CC</sub> = 0 V			-0.05	-0.04			
	V <sub>A</sub> or V <sub>B</sub> = 12 V		HVD10, Other input at 0 V	0.2	0.5	mA		
	V <sub>A</sub> or V <sub>B</sub> = 12 V, V <sub>CC</sub> = 0 V			0.25	0.5			
	V <sub>A</sub> or V <sub>B</sub> = -7 V			-0.4	-0.2			
	V <sub>A</sub> or V <sub>B</sub> = -7 V, V <sub>CC</sub> = 0 V			-0.4	-0.15			
I <sub>IH</sub> High-level input current, RE	V <sub>IH</sub> = 2 V		-30	0		µA		
I <sub>IL</sub> Low-level input current, RE	V <sub>IL</sub> = 0.8 V		-30	0		µA		
C <sub>ID</sub> Differential input capacitance	V <sub>ID</sub> = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		15			pF		
I <sub>CC</sub> Supply current	RE at 0 V, D & DE at 0 V, No load	Receiver enabled and driver disabled	4	8		mA		
	RE at V <sub>CC</sub> , D at V <sub>CC</sub> , DE at 0 V, No load	Receiver disabled and driver disabled (standby)	1	5		µA		
	RE at 0 V, D & DE at V <sub>CC</sub> , No load	Receiver enabled and driver enabled	9	15.5		mA		

(1) All typical values are at 25°C and with a 3.3-V supply.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	HVD10 HVD11 HVD12 HVD11 HVD12 HVD10 HVD11 HVD12 HVD10 HVD11 HVD12	12.5	20	25	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output		12.5	20	25	
$t_{PLH}$ Propagation delay time, low-to-high-level output		30	55	70	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output		30	55	70	ns
$t_{sk(p)}$ Pulse skew ( $ t_{PHL} - t_{PLH} $ )			1.5		ns
			4		
			4		
$t_{sk(pp)}$ (2) Part-to-part skew			8		ns
			15		
			15		
$t_r$ Output signal rise time	$C_L = 15 \text{ pF}$ , See Figure 8	1	2	5	ns
$t_f$ Output signal fall time		1	2	5	
$t_{PZH}$ (1) Output enable time to high level	$C_L = 15 \text{ pF}$ , DE at 3 V, See Figure 9		15		ns
$t_{PZL}$ (1) Output enable time to low level			15		
$t_{PHZ}$ Output disable time from high level			20		
$t_{PLZ}$ Output disable time from low level			15		
$t_{PZH}$ (2) Propagation delay time, standby-to-high-level output	$C_L = 15 \text{ pF}$ , DE at 0, See Figure 10		6		$\mu\text{s}$
$t_{PZL}$ (2) Propagation delay time, standby-to-low-level output			6		

(1) All typical values are at 25°C and with a 3.3-V supply

(2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## PARAMETER MEASUREMENT INFORMATION

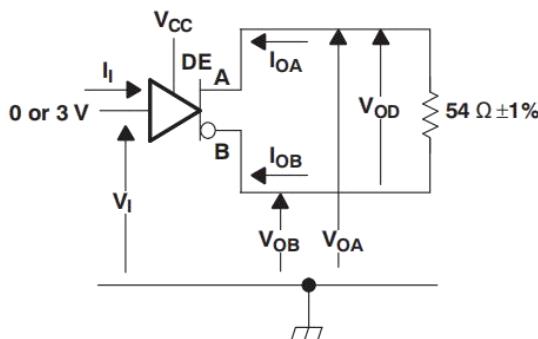


Figure 1. Driver VOD Test Circuit and Voltage and Current Definitions

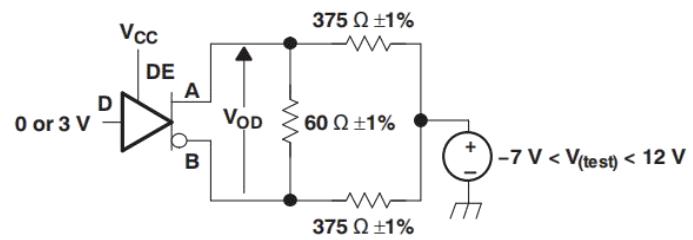
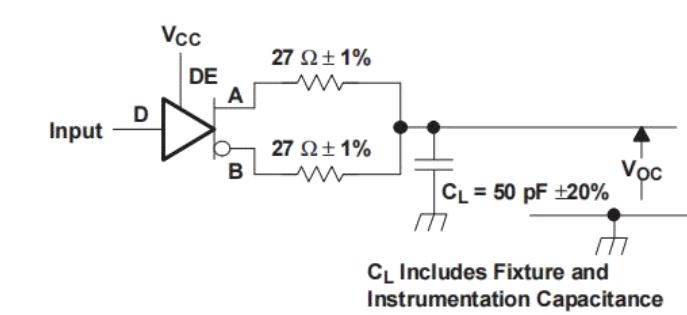


Figure 2. Driver VOD With Common-Mode Loading Test Circuit



Input: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_o = 50 \Omega$

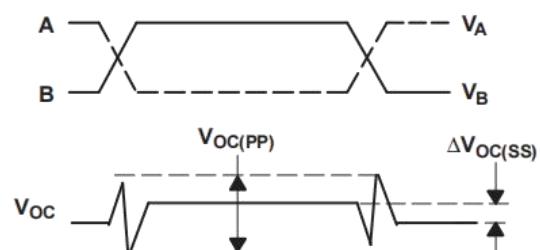
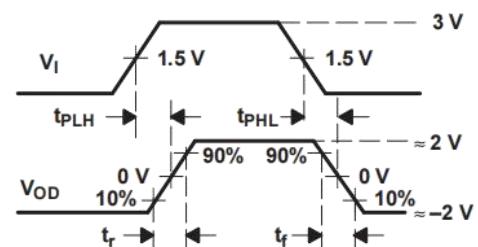
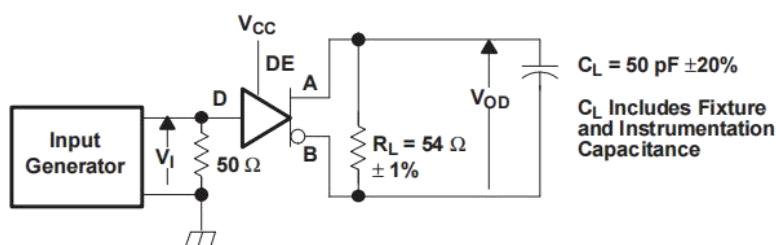
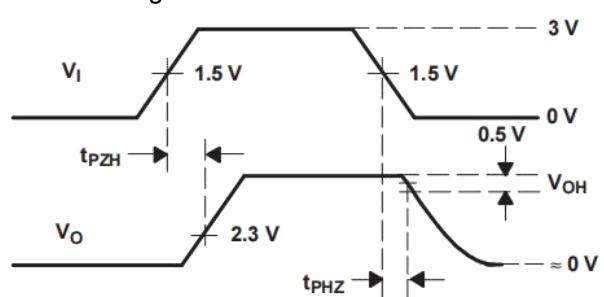
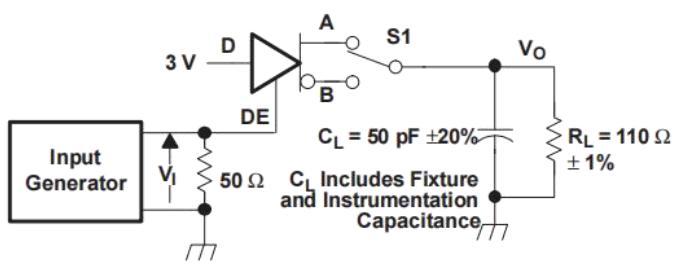


Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



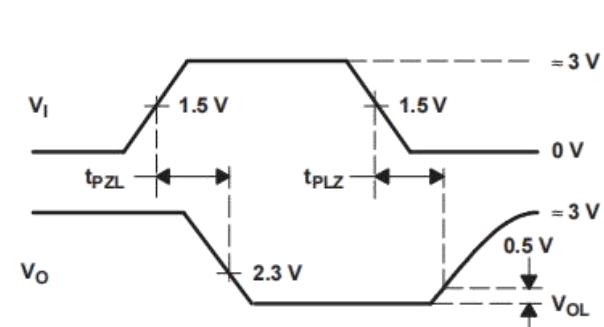
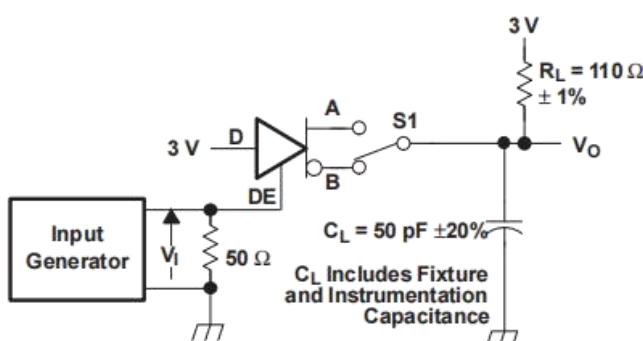
Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_o = 50 \Omega$

Figure 4. Driver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_o = 50 \Omega$

Figure 5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_o = 50 \Omega$

Figure 6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

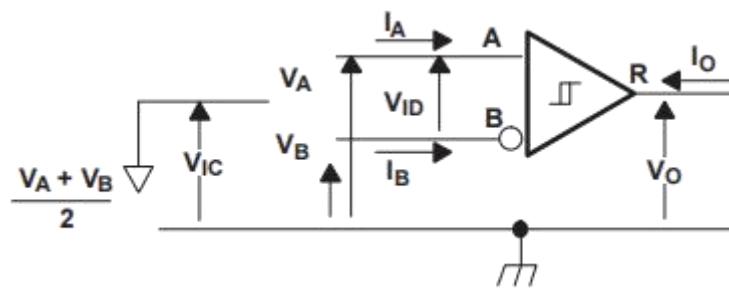
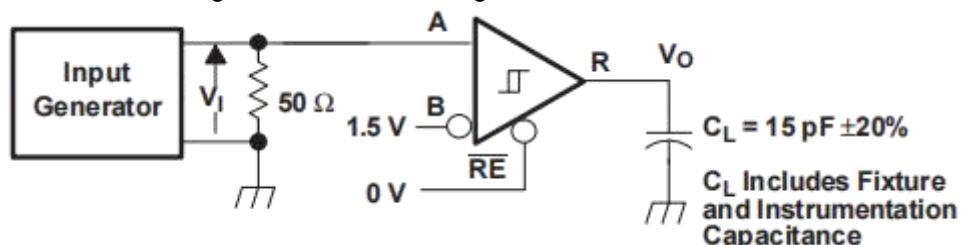


Figure 7. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_o = 50 \Omega$

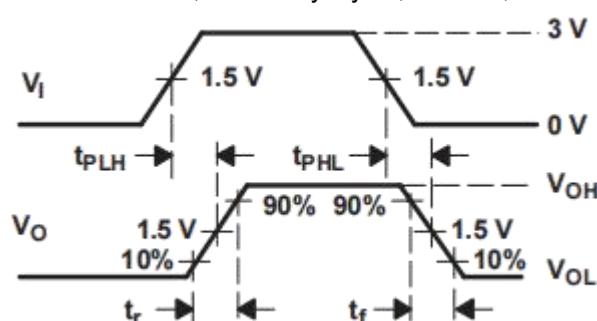
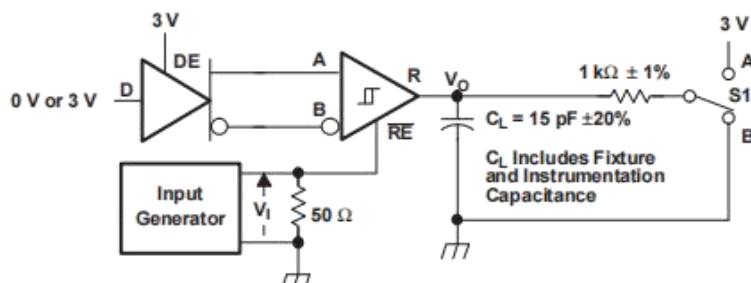


Figure 8. Receiver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_o = 50 \Omega$

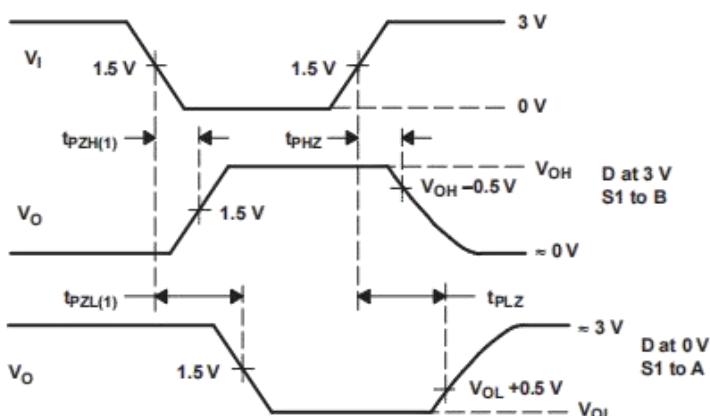


Figure 9. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

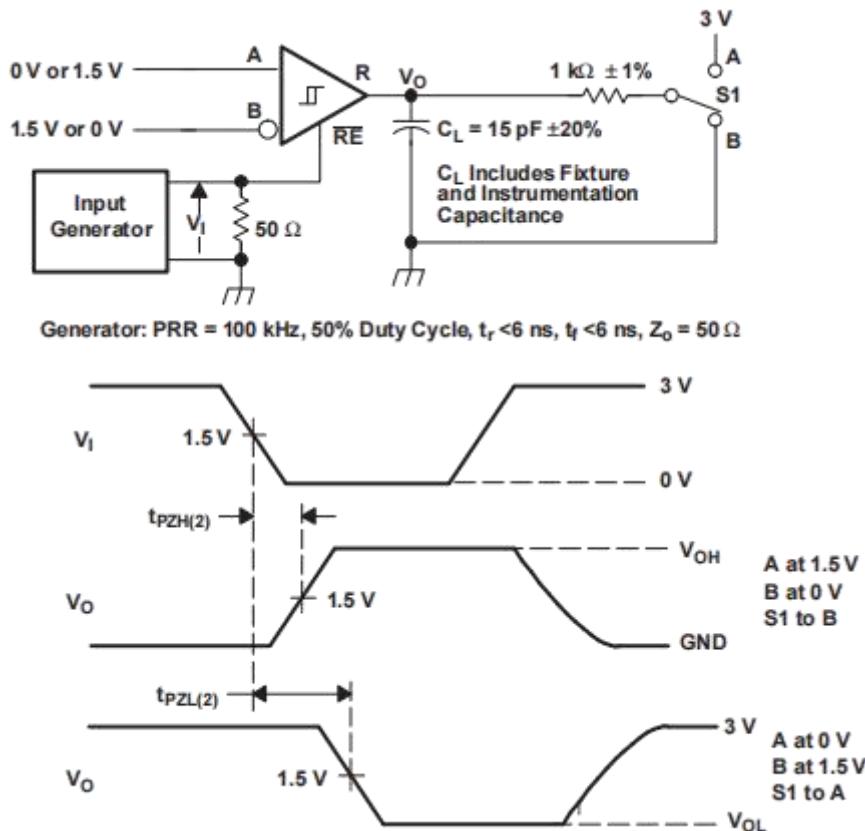
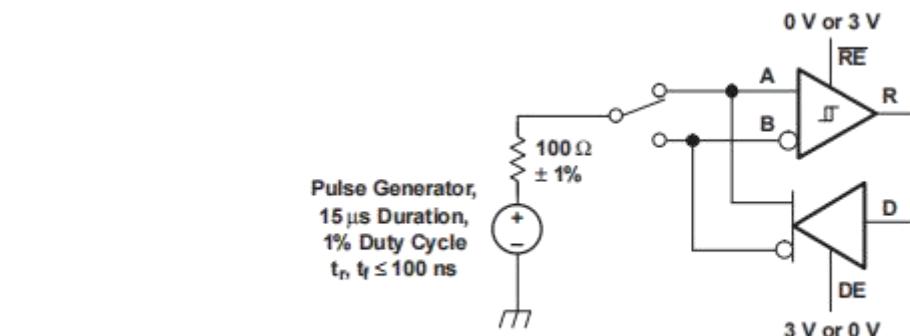


Figure 10. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 11. Test Circuit, Transient Over Voltage Test

**PARAMETER MEASUREMENT INFORMATION (continued)**
**FUNCTION TABLES**
**Table 1. DRIVER(1)**

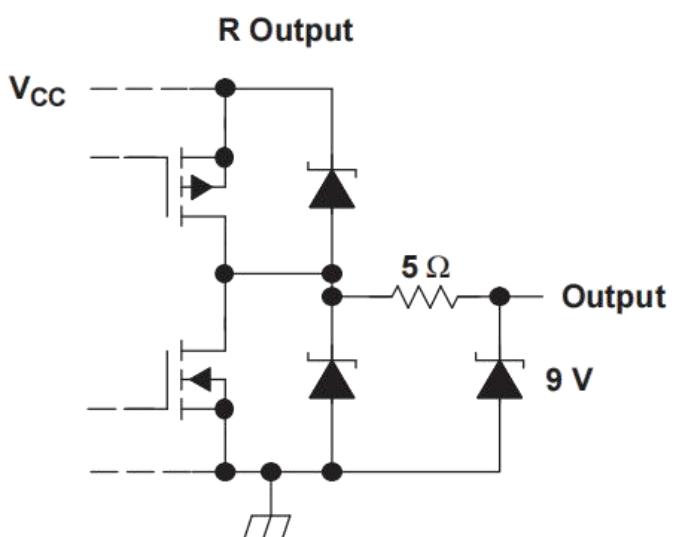
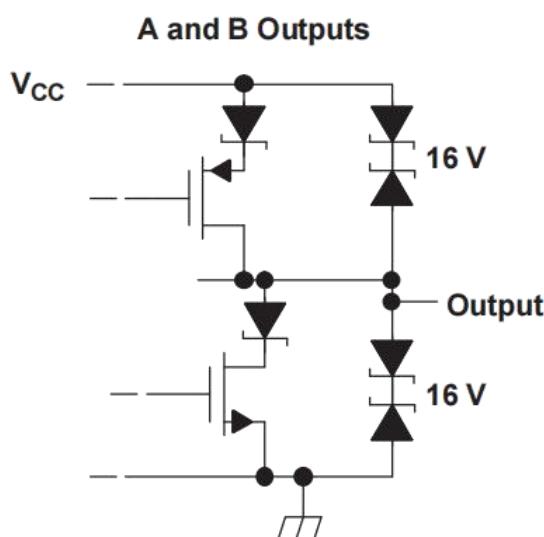
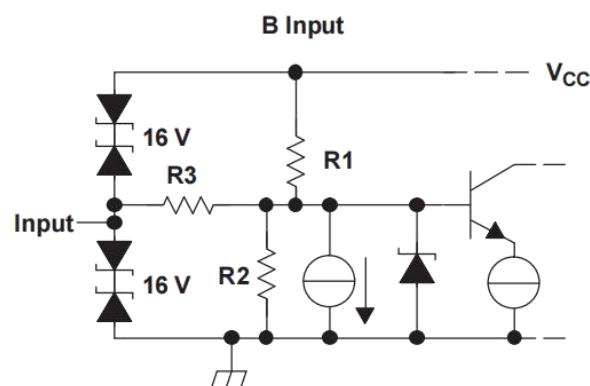
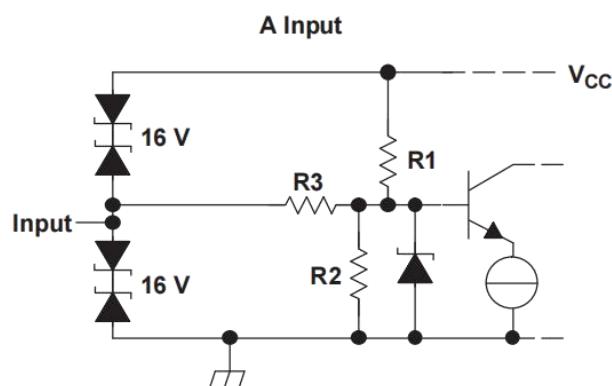
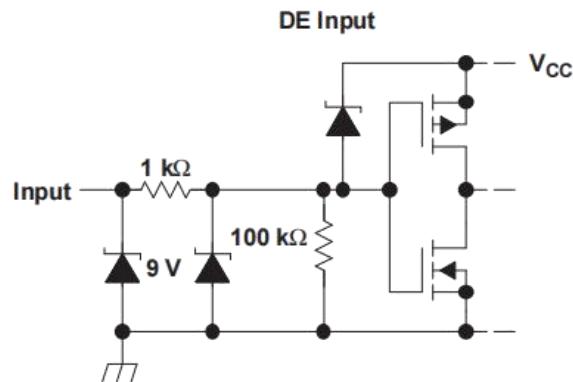
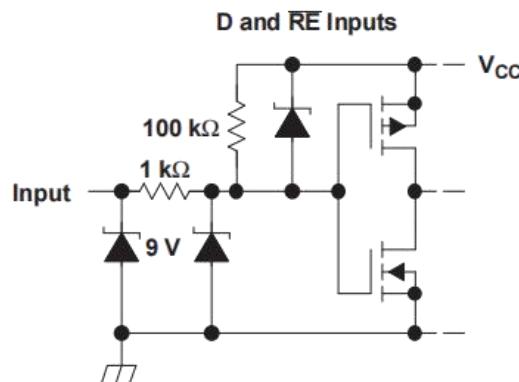
		OUTPUTS	
INPU TD	ENABLE DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

**Table 2. RECEIVER(1)**

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLERE	OUTPUTR
$V_{ID} \leq -0.2 \text{ V}$	L	L
$-0.2 \text{ V} < V_{ID} < -0.01 \text{ V}$	L	?
$-0.01 \text{ V} \leq V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short circuit	L	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

**EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**


	R1/R2	R3
HX65HVD10	9 kΩ	45 kΩ
HX65HVD11	36 kΩ	180 kΩ
HX65HVD12	36 kΩ	180 kΩ

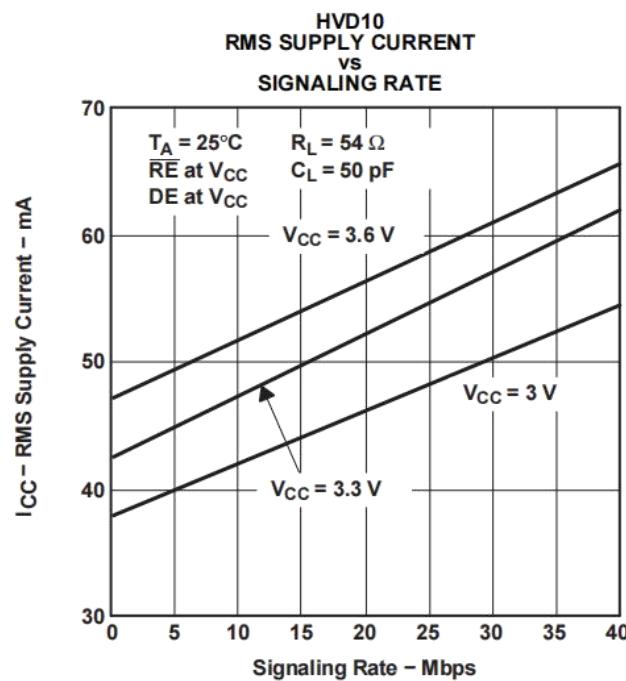
**TYPICAL CHARACTERISTICS**


Figure 12.

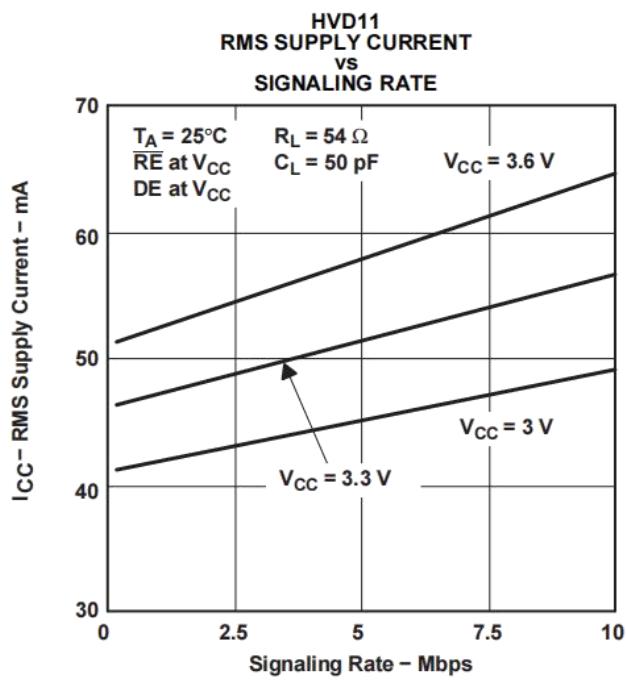


Figure 13.

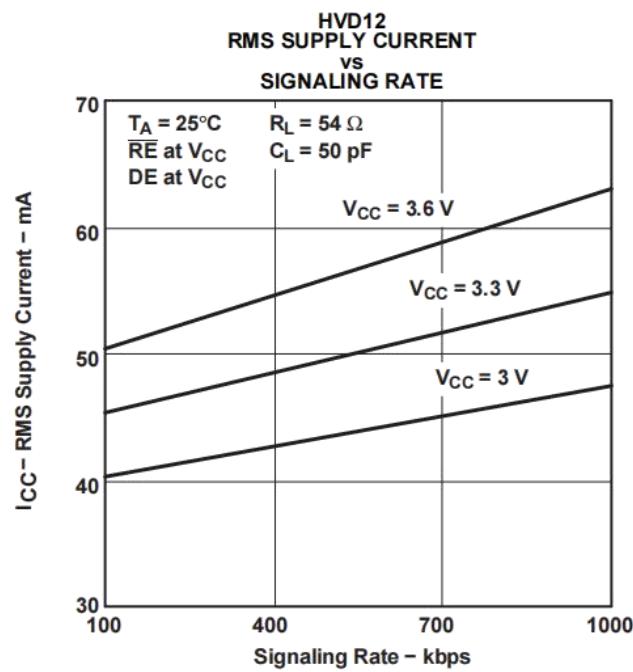


Figure 14.

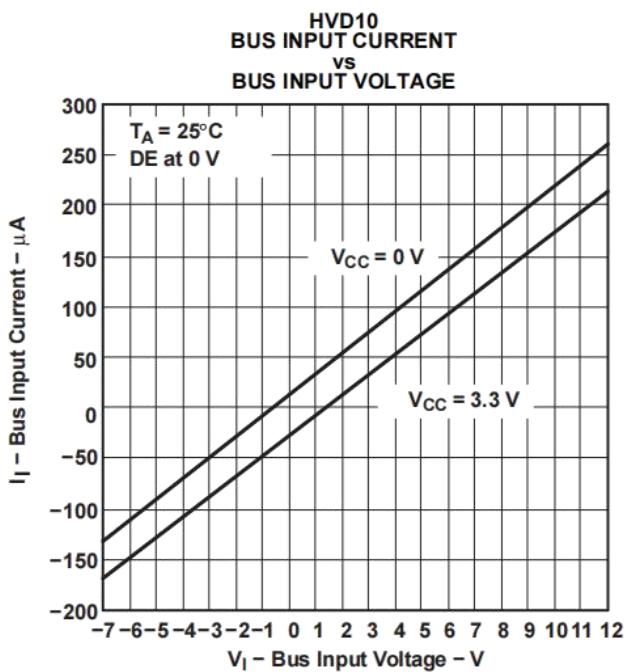


Figure 15.

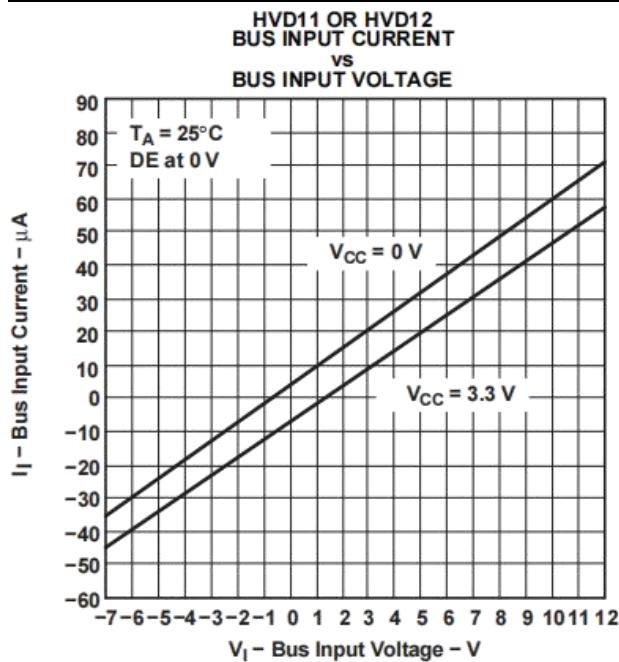


Figure 16.

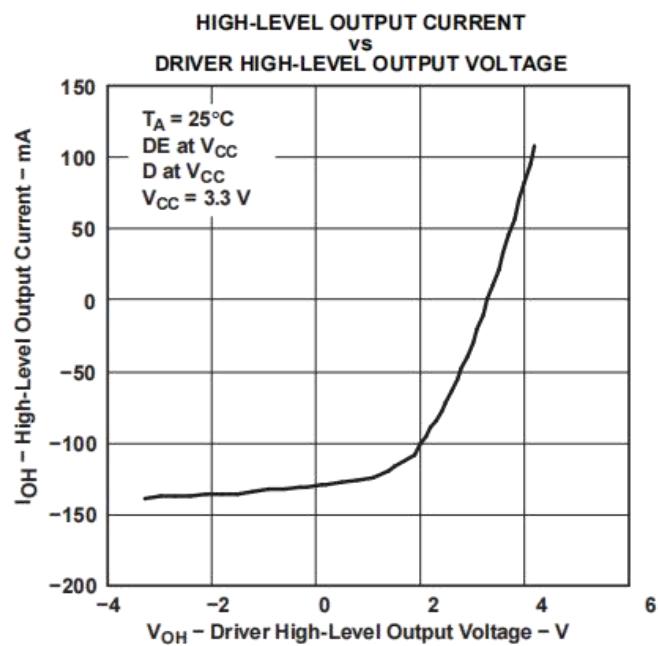


Figure 17.

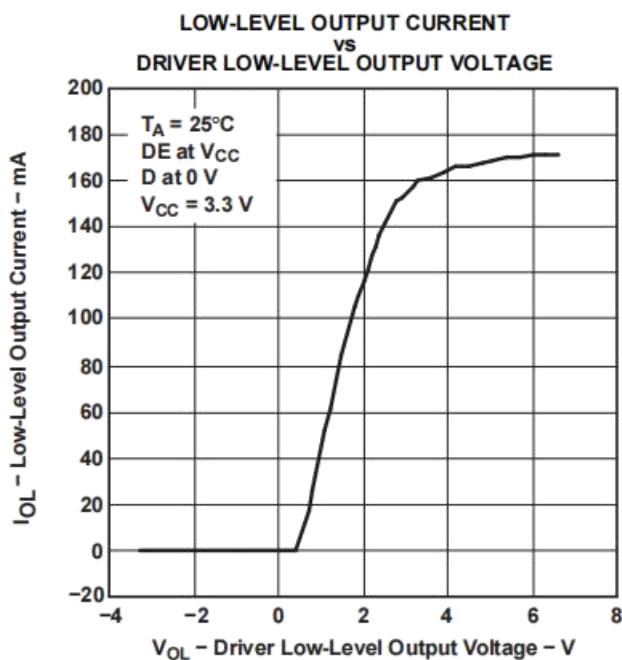


Figure 18.

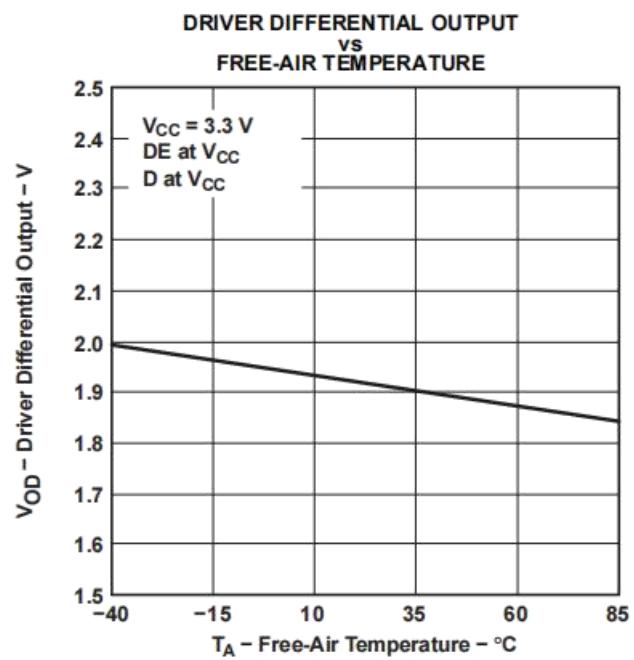


Figure 19.

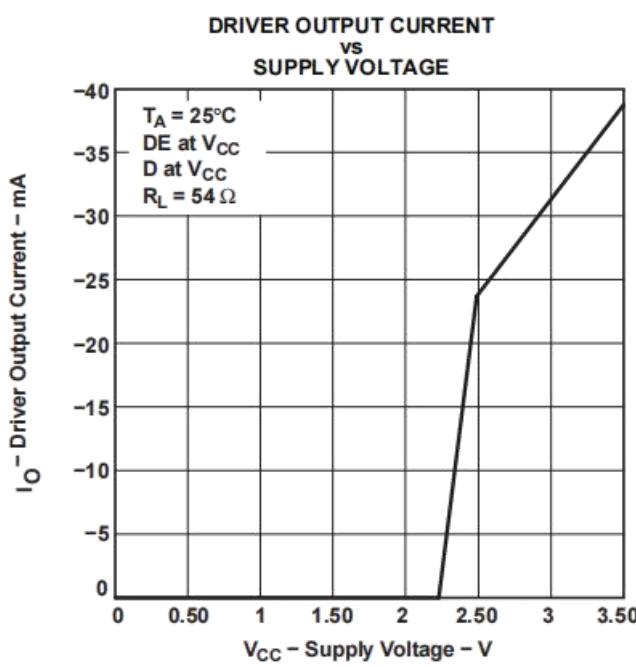


Figure 20.

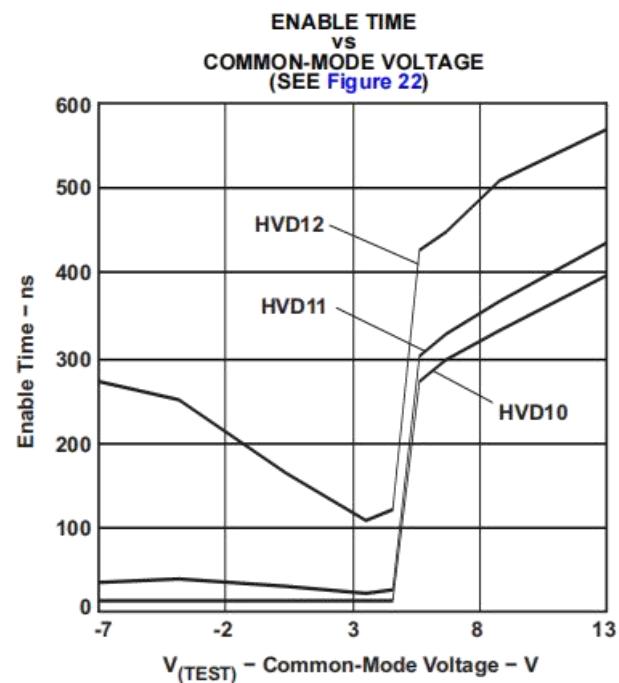


Figure 21.

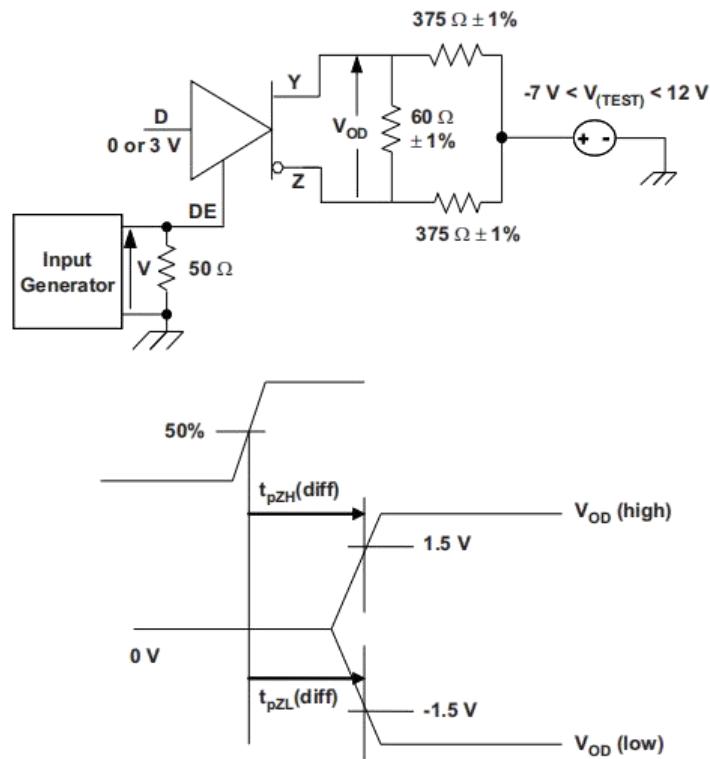
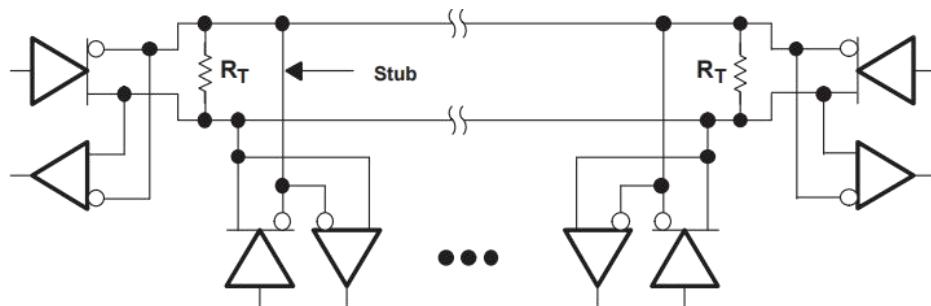


Figure 22. Driver Enable Time From DE to VOD

The time t<sub>PZL</sub>(x) is the measure from DE to VOD(x). VOD is valid when it is greater than 1.5 V.

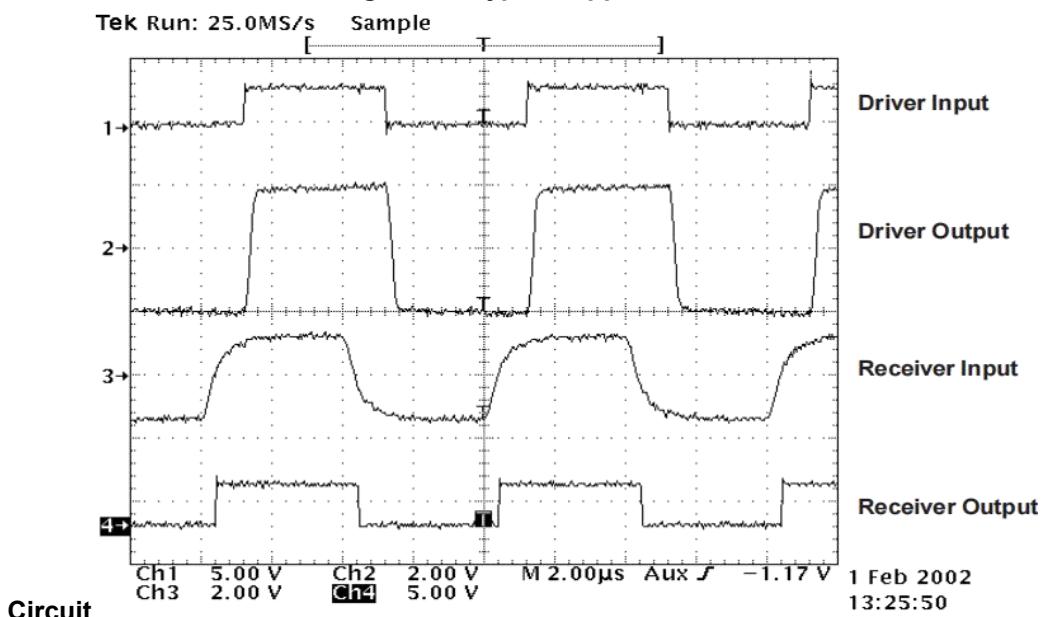
## APPLICATION INFORMATION



Device	Number of Devices on Bus
HVD10	64
HVD11	256
HVD12	256

NOTE: The line should be terminated at both ends with its characteristic impedance ( $RT = ZO$ ). Stub lengths off the main line should be kept as short as possible.

**Figure 23. Typical Application**



**Figure 24. HVD12 Input and Output Through 2000 Feet of Cable**

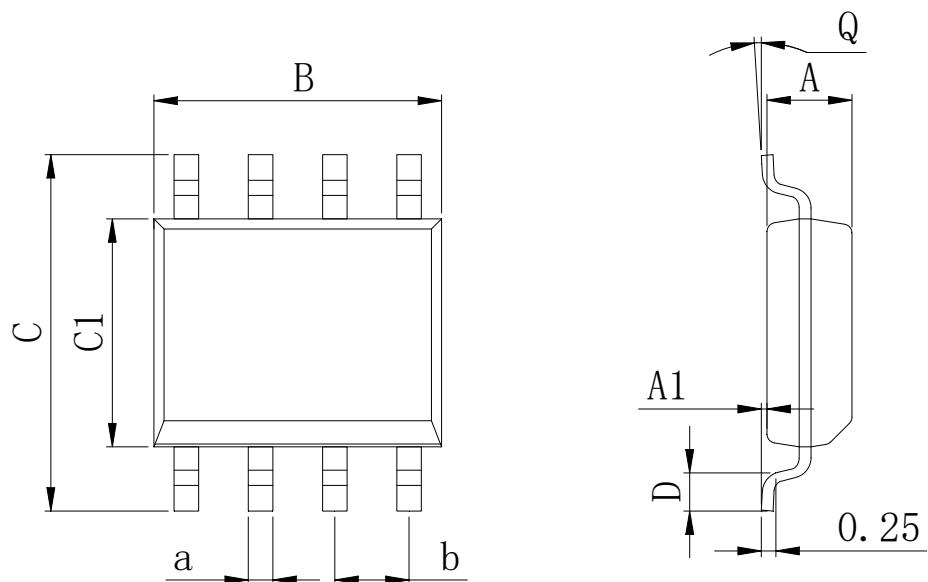
An example application for the HVD12 is illustrated in Figure 23. Two HVD12 transceivers are used to communicate data through a 2000 foot (600 m) length of Commscope 5524 category 5e+ twisted pair cable. The bus is terminated at each end by a 100- $\Omega$  resistor, matching the cable characteristic impedance. Figure 24 illustrates operation at a signaling rate of 250 kbps.

## LOW-POWER STANDBY MODE

When both the driver and receiver are disabled (DE low and RE high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

## Physical Dimensions

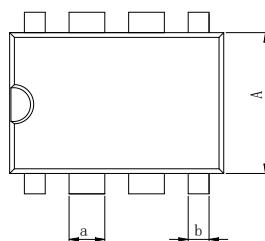
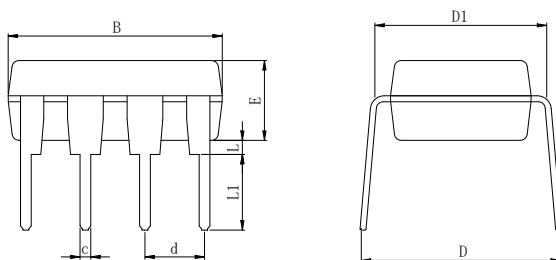
SOP-8



Dimensions In Millimeters(SOP-8)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

DIP-8



Dimensions In Millimeters(DIP-8)

Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

## Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2016-1	New	1-18
V1.1	2023-7	Update encapsulation type、Update Lead Temperature	1、2

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