

Features

- The plastic package carries UL Flammability Classification 94V-0
- For surface mounted applications
- Low reverse leakage
- Built-in strain relief, ideal for automated placement
- High forward surge current capability
- High temperature soldering guaranteed: 260°C/10 seconds at terminals



Mechanical Characteristics

- Case: SOD-123FL package molded plastic body over passivated chip
- Terminals: Solder plated, solderable per MIL-STD-750, Method 2026
- Polarity: Color band denotes cathode end
- Mounting Position: Any

Absolute Maximum Ratings and Electrical Parameters (TA=25°C unless otherwise specified)

PARAMETER		SYMBOL	1N4001	UNIT
Maximum repetitive peak reverse voltage		V_{RRM}	50	V
Maximum RMS voltage		V_{RMS}	35	V
Maximum DC blocking voltage		V_{DC}	50	V
Maximum average forward rectified current		I_{AV}	1	A
Peak forward surge current (NOTE1)		I_{FSM}	30	A
Maximum instantaneous forward voltage at 1A		V_F	1.1	V
Maximum DC reverse current at rated DC blocking voltage	$T_A=25\text{ }^{\circ}\text{C}$	I_R	5	uA
	$T_A=100\text{ }^{\circ}\text{C}$	I_{RT}	50	uA
Typical junction capacitance (NOTE 2)		C_J	15	pF
Typical Thermal Resistance Junction to Ambient (NOTE3)		$R_{\theta JA}$	90	$^{\circ}\text{C/W}$
Typical Thermal Resistance Junction to Lead (NOTE3)		$R_{\theta JL}$	30	$^{\circ}\text{C/W}$
Operating Temperature Range		T_J	-55 to 150	$^{\circ}\text{C}$
Storage Temperature Range		T_{STG}	-55 to 150	$^{\circ}\text{C}$

Note1: 8.3ms single half sine-wave superimposed on rated load

Note2: Measured at 1MHz and applied reverse voltage of 4.0V DC.

Note3: PCB. mounted with 3x3mm copper pad areas

Rating And Characteristic Curves (TA=25°C unless otherwise noted)

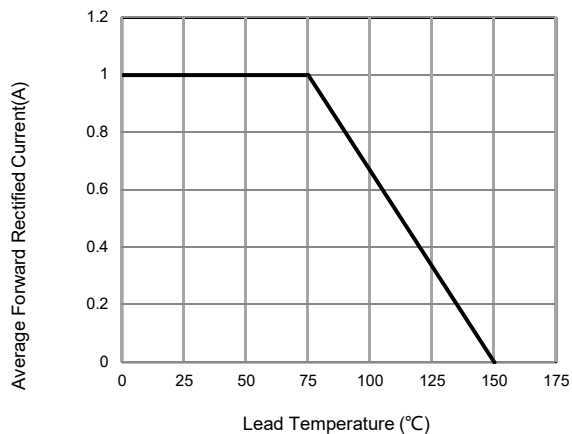


Fig. 1 - Forward Current Derating Curve

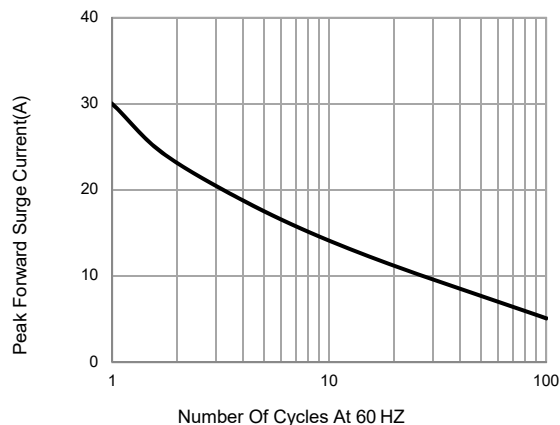


Fig. 2 - Maximum Non-Repetitive Peak Forward Surge Current

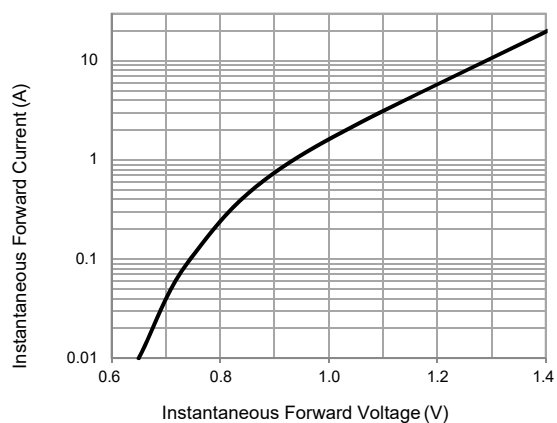


Fig. 3 - Typical Instantaneous Forward Characteristics

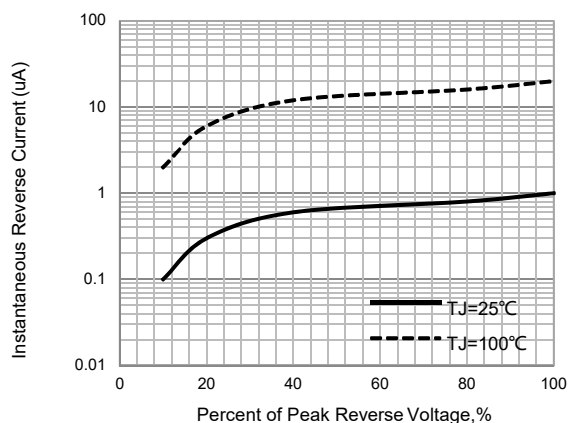


Fig. 4 - Typical Reverse Characteristics

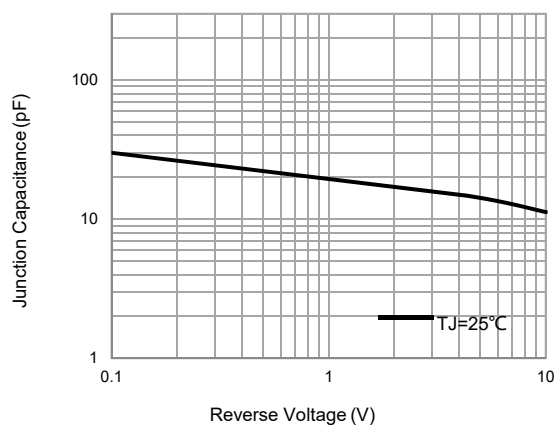


Fig. 5 - Typical Junction Capacitance

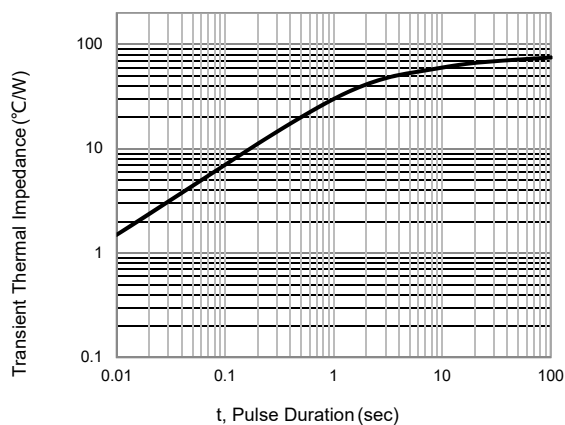


Fig. 6 - Typical Transient Thermal Impedance

PACKAGE OUTLINE

