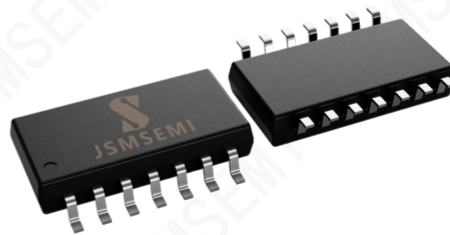


General Description

The SN74LVC04ADR-JSM is a hex buffer with open-drain outputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments. Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.



Features and Benefits

- Wide supply voltage range from 1.2 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low power dissipation
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.5 V to 5.5 V)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 6000 V
 - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

Function Diagram

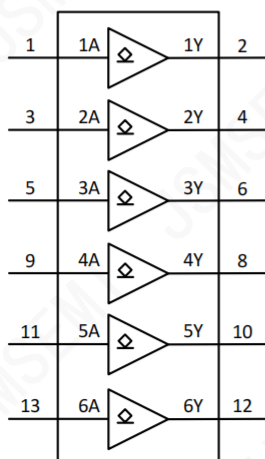


Fig. 1. Logic symbol

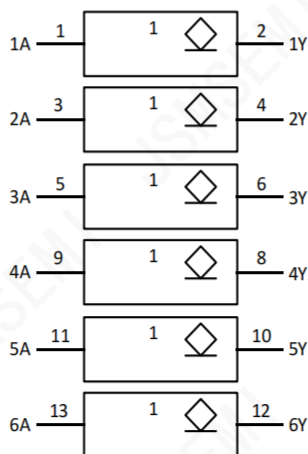


Fig. 2. IEC logic symbol

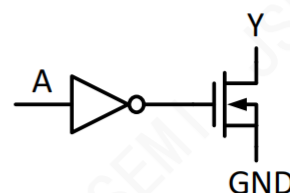


Fig. 3. Logic diagram (one gate)

Pinning Information

Pinning

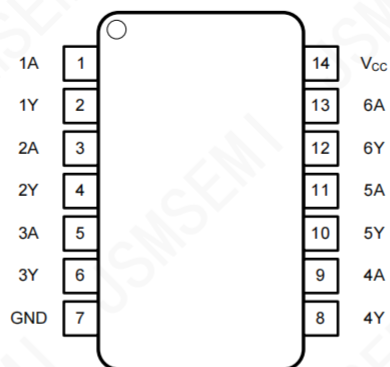


Fig. 4. Top view pin configuration SOP

Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	Data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	Data output
GND	7	Ground (0V)
V _{CC}	14	Supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input nA	Output nY
L	L
H	Z

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	input voltage	[1]	-0.5	6.5	V
I_{OK}	output clamping current	$V_O < 0$ V	-50		mA
V_O	output voltage	Active mode [1]	-0.5	6.5	V
		Power-down mode; $V_{CC} = 0$ V [1]	-0.5	6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}		50	mA
I_{CC}	supply current			100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C		500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
		functional	1.2		V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	5.5	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
T_{amb}	ambient temperature		-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	0	10	ns/V

Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	1.08			1.08		V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65V_{CC}$			$0.65V_{CC}$		V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7			1.7		V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0			2.0		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7V_{CC}$			$0.7V_{CC}$		V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$			0.12		0.12	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$			$0.35V_{CC}$		$0.35V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$			0.7		0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$			0.8		0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			$0.3V_{CC}$		$0.3V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = 100\mu\text{A}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$			0.10		0.10	V
		$I_O = 4\text{ mA}$; $V_{CC} = 1.65\text{ V}$			0.45		0.70	V
		$I_O = 8\text{ mA}$; $V_{CC} = 2.3\text{ V}$			0.30		0.45	V
		$I_O = 12\text{ mA}$; $V_{CC} = 2.7\text{ V}$			0.40		0.60	V
		$I_O = 24\text{ mA}$; $V_{CC} = 3.0\text{ V}$			0.55		0.80	V
		$I_O = 32\text{ mA}$; $V_{CC} = 4.5\text{ V}$			0.55		0.80	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND}$; $V_{CC} = 0\text{ V to }5.5\text{ V}$		± 0.1	± 5		± 20	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$; $V_O = 5.5\text{ V or GND}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$		± 0.1	± 10		± 20	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}$; $V_I\text{ or }V_O = 5.5\text{ V}$		± 0.1	± 10		± 20	μA
I_{CC}	supply current	$V_{CC} = 1.65\text{ V to }5.5\text{ V}$; $V_I = V_{CC}\text{ or GND}$; $I_O = 0\text{ A}$;		0.01	10		40	μA
ΔI_{CC}	additional supply current	per input pin ; $V_{CC} = 2.3\text{ V to }5.5\text{ V}$; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$		0.2	500		5000	μA
C_I	input capacitance	$V_{CC} = 3.3\text{ V}$; $V_I = \text{GND to }V_{CC}$		4				pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$.

Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 5						
		$V_{CC} = 1.2\text{ V}$		28.3				ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	3.5	8.5	16.5	3.5	17	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.0	4.8	8.0	2.0	9.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	3.5	5.5	1.5	6.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.9	4.5	1.0	5.0	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 5						
		$V_{CC} = 1.2\text{ V}$		25.3				ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	3.5	7.7	14.5	3.5	15	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.0	5.0	7.5	2.0	8.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	3.5	5.5	1.5	6.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.4	3.5	1.0	4.0	ns
C_{PD}	power dissipation capacitance	per buffer ; $V_I = \text{GND to } V_{CC}$ [2]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		3.3				pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		3.4				pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$		3.9				pF
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		4.8				pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 3.3\text{ V}$ and 5.0 V respectively.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

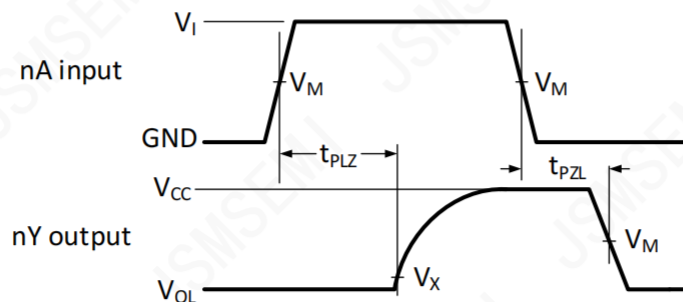
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Waveforms and test circuit



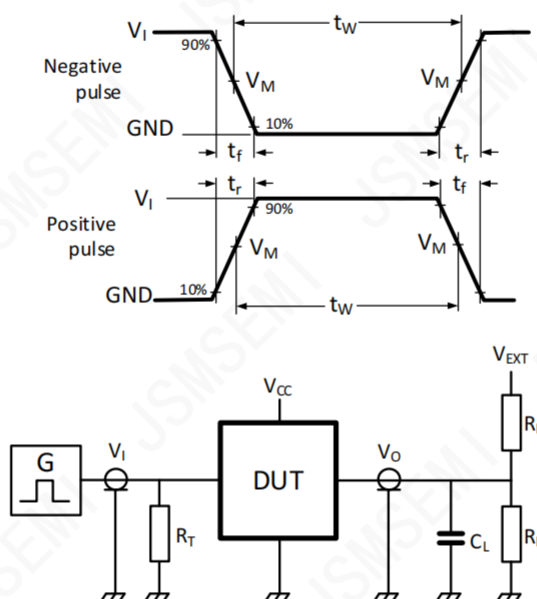
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The input nA to output nY propagation delays

Table 8. Measurement points

Supply voltage	Input	Output	
V_{CC}	V_M	V_X	V_M
1.2 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$0.5V_{CC}$
1.65 V to 1.95 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$0.5V_{CC}$
3.0 V to 3.6 V	1.5 V	$V_{OL} + 0.3 V$	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

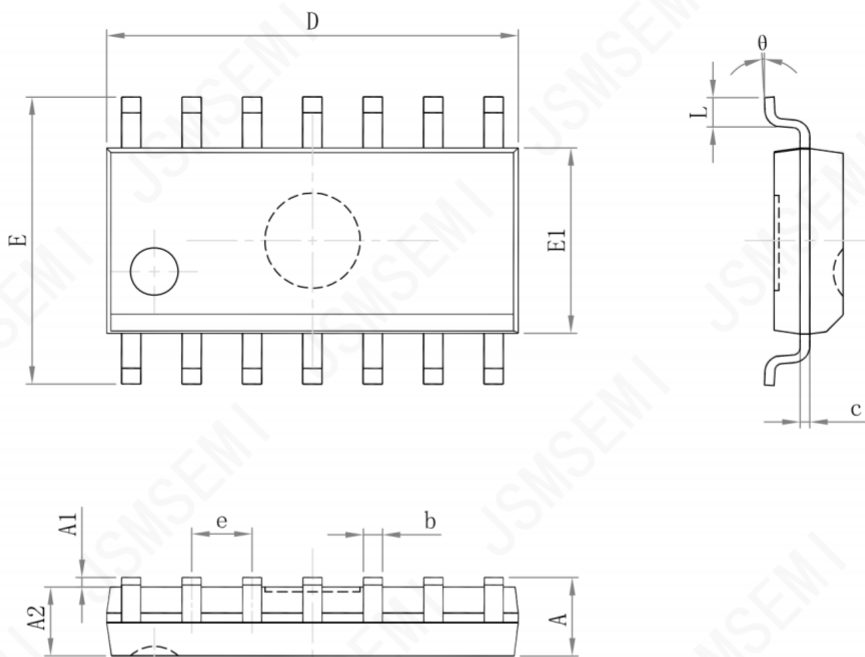
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLZ}, t_{PZL}
1.2V	V_{CC}	$\leq 2.0 \text{ ns}$	15 pF	500 Ω	$2 \times V_{CC}$
1.65 V to 1.95 V	V_{CC}	$\leq 2.0 \text{ ns}$	15 pF	500 Ω	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$\leq 2.0 \text{ ns}$	15 pF	500 Ω	$2 \times V_{CC}$
3.0 V to 3.6 V	3 V	$\leq 2.0 \text{ ns}$	15 pF	500 Ω	6.0 V
4.5 V to 5.5 V	V_{CC}	$\leq 2.0 \text{ ns}$	15 pF	500 Ω	$2 \times V_{CC}$

Package Outline

SOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	—	1.750	—	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	—	0.049	—
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER' S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

JSMSEMI All Rights Reserved. Information and data in this document are owned by JSMSEMI wholly and may not be edited, reproduced, or redistributed in any way without the express written consent from JSMSEMI.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com