

General Description

The 74HC1G04GV,125-JSM is single inverters. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

The device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

Features and Benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 200 mA
- Symmetrical output impedance
- Balanced propagation delays
- Input levels: CMOS level
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 7000 V
 - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

Function Diagram

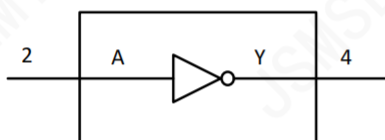


Fig. 1. Logic symbol

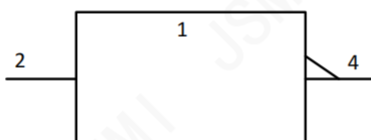


Fig. 2. IEC logic symbol

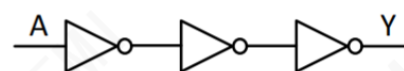


Fig. 3. Logic diagram

Ordering Information

Order number	Package	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
74HC1G04GV,125-JSM	SOT-753	-40 to 125°C	3	T&R,3000	Rohs

Pinning Information

Pinning

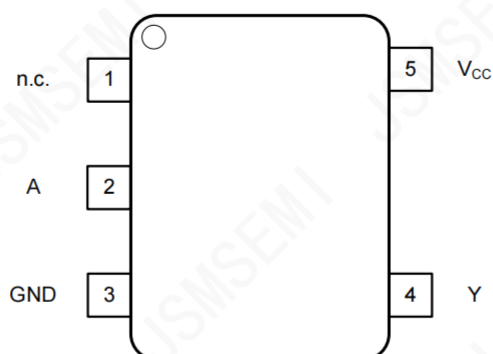


Fig. 4. Top view pin configuration SOT-753

Pin description

Symbol	Pin	Description
n.c.	1	Not connected
A	2	Data input
GND	3	Ground (0V)
Y	4	Data output
V _{cc}	5	Supply voltage

Functional Description

H = HIGH voltage level; L = LOW voltage level.

Input	Output
A	Y
L	H
H	L

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
V_I	input voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$	-20		mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]		± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$		± 25	mA
I_{CC}	supply current			75	mA
I_{GND}	ground current		-75		mA
P_{tot}	total power dissipation	$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$		250	mW
T_{stg}	storage temperature		-65	150	$^{\circ}\text{C}$

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	74HC1G04GV,125-JSM			Unit
			Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0		5.5	V
V_O	output voltage		0		V_{CC}	V
T_{amb}	ambient temperature		-40	25	125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			100	ns/V
		$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$			20	ns/V

Static Characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC1G04GV,125-JSM								
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5			1.5		V
		V _{CC} = 3.0 V	2.1			2.1		V
		V _{CC} = 5.5 V	3.85			3.85		V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V			0.5		0.5	V
		V _{CC} = 3.0 V			0.9		0.9	V
		V _{CC} = 5.5 V			1.65		1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0		1.9		V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0		2.9		V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5		4.4		V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.48	2.93		2.40		V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.80	4.39		3.70		V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 50 μA; V _{CC} = 2.0 V		0	0.1		0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V		0	0.1		0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V		0	0.1		0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V		0.05	0.44		0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V		0.07	0.44		0.55	V
I _I	input leakage current	V _I = 5.5 V or GND ; V _{CC} = 0 V to 5.5 V		±0.01	±1.0		±2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND ; I _O = 0 A ; V _{CC} = 5.5 V		0.01	10		40	μA
C _I	input capacitance			3.5				pF

Dynamic Characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
74HC1G04GV,125-JSM								
t _{pd}	propagation delay	A to Y; see Fig. 5 [2]						
		V _{CC} = 3.0 V to 3.6 V, C _L = 15 pF	1.0	4.3	9.5	1.0	10.0	ns
		V _{CC} = 4.5 V to 5.5 V, C _L = 15 pF	1.0	3.1	6.5	1.0	7.0	ns
C _{PD}	power dissipation capacitance	C _L = 15 pF ; f = 1MHz ; V _I = GND to V _{CC} ; [3]		20				pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 3.3\text{ V}$ and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

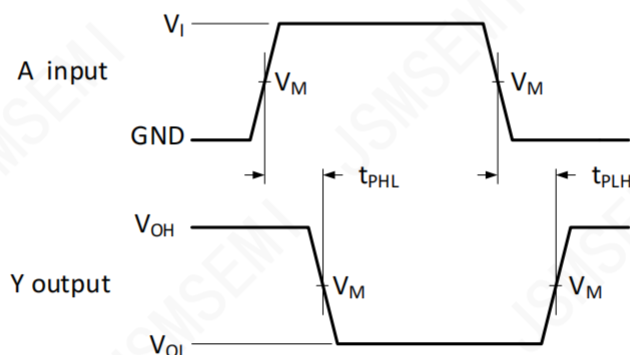
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

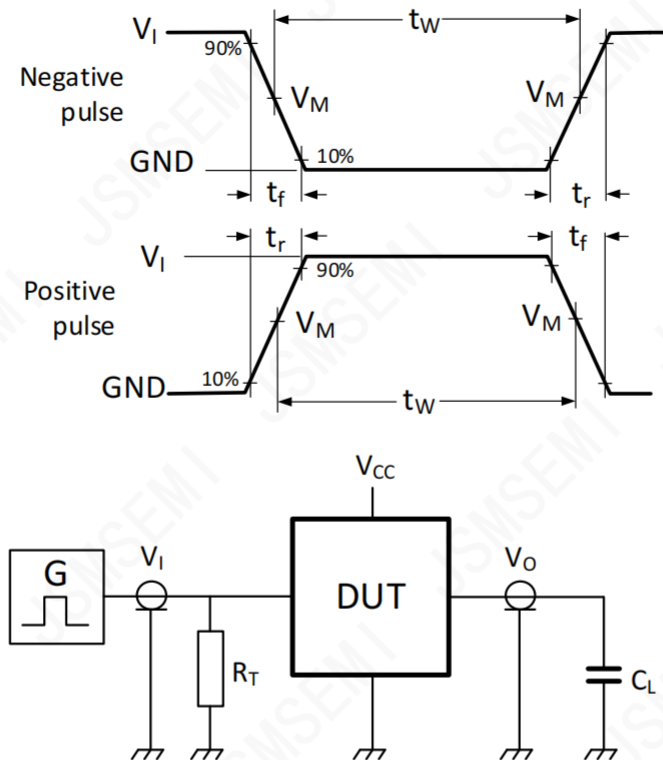
Waveforms and test circuit



V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The input A to output Y propagation delays

Type	Input		Output
	V_I	V_M	V_M
74HC1G04GV,125-JSM	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

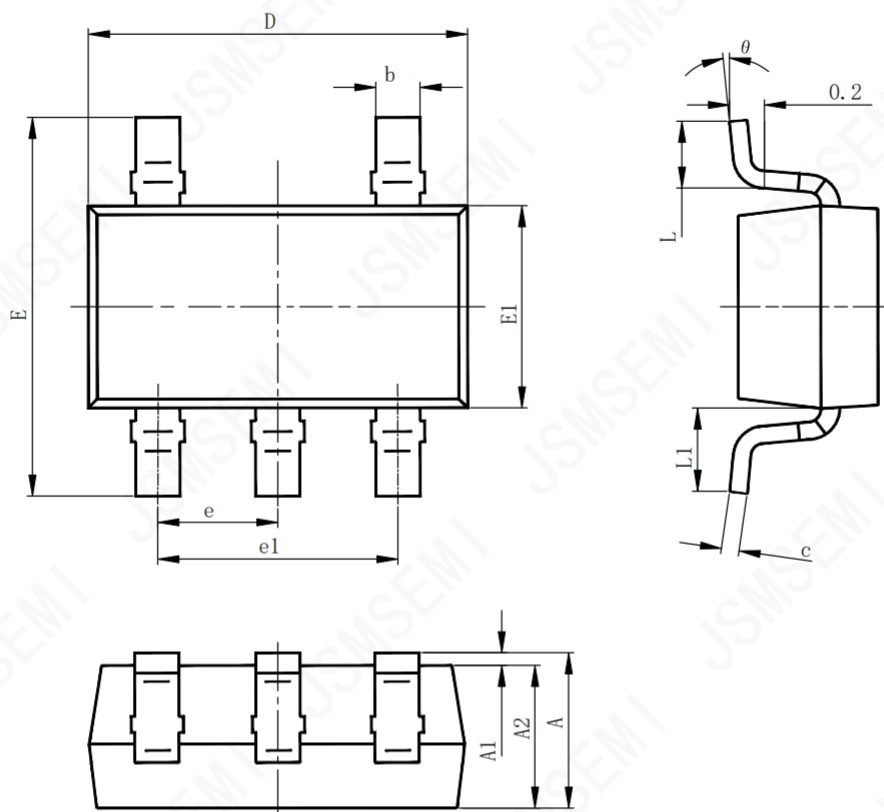
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

Type	Input	Load
	$t_r = t_f$	C_L
74HC1G04GV,125-JSM	$\leq 2.5 \text{ ns}$	15 pF

Package Outline

SOT-753



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

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