100V 0.5A Synchronous Buck Converter with Ultra-low I_Q

1 FEATURES

- Wide Input Range: 6.5V-100V
- Constant On-Time Control Mode
- 0.5A Continuous Output Current
- 30uA Ultra-low Quiescent Current (GBI1A01)
- Integrated 530mΩ High-Side and 230mΩ Low-Side Power MOSFETs
- 1.2V ± 1.0% Feedback Reference Voltage
- Adjustable Switching Frequency 100kHz-300kHz
- 3ms Internal Soft-start Time and PG Pin
- PSM Mode at Light Load (GBI1A01)
- FPWM Mode at Light load (GBI1A00)
- Protections with Input UVLO, OT and OCP
- Internal VCC Bias Regulator and Boot diode
- Available in a 4.9mm x 3.9mm eSOP-8L Package

2 APPLICATIONS

- BMS (E-Bike, Electric Tools)
- Telecom and Automotive Systems
- Motor Drivers and Drones
- General Purpose Wide Vin Regulation

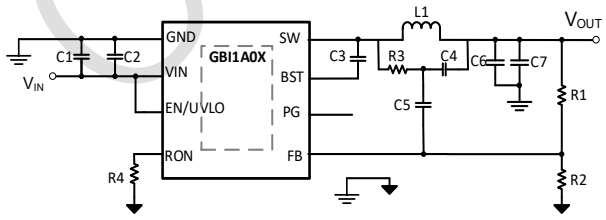
3 ORDERING INFORMATION

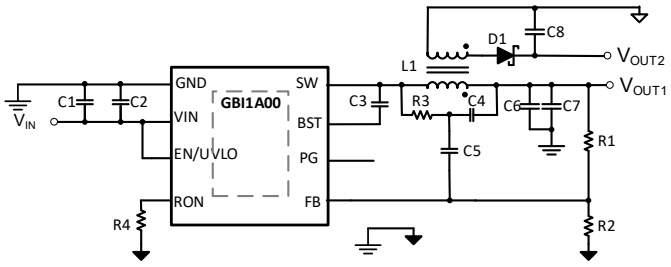
TYPE	MARKING	PACKAGE
GBI1A00SMAR	1A00	eSOP-8L
GBI1A01SMAR	1A01	eSOP-8L

4 DISCRIPTION

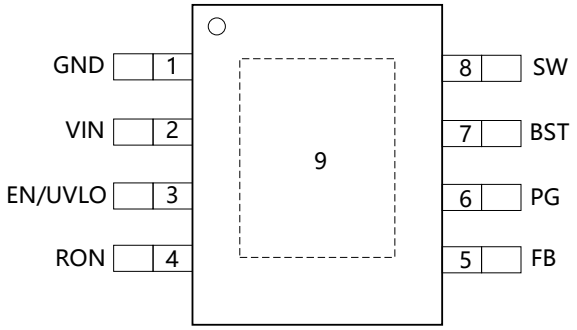
The GBI1A00 and GBI1A01 is a 6.5V-100V input, 0.5A output synchronous buck converter. A constant on-time (COT) control architecture provides excellent load and line transient response. Additional features of the GBI1A00 and GBI1A01 include peak and valley overcurrent protection, integrated VCC bias supply and bootstrap diode, precision enable and input UVLO, thermal shutdown protection with automatic recovery. An open-drain power good indicator provides sequencing, fault reporting, and output voltage monitoring. GBI1A01 works with ultra-low IQ in PSM mode to achieve high light-load efficiency. GBI1A00 works in FPWM mode operation and can be used for isolated voltage output applications.

5 TYPICAL APPLICATIONS





6 PIN CONFIGURATION AND FUNCTIONS



Top View: GBI1A00 and GBI1A01 eSOP-8L

PIN OUT		I/O	PIN FUNCTION
NAME	NO.		
1	GND	G	Ground connection for internal circuits.
2	VIN	P/I	Power supply input. Must be locally bypassed.
3	EN/UVLO	I	Precision enable and undervoltage lockout (UVLO) set pin. If the EN/UVLO voltage is less than 1.5 V, the converter is shutdown and all functions disabled. If the EN/UVLO voltage is larger than 1.5 V, the buck starts-up. This pin cannot be floating.
4	RON	I	On-time programming pin. A resistor between this pin and GND sets the buck switch on-time.
5	FB	I	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT node to FB pin and from FB pin to GND to set up output voltage.
6	PG	O	Power good indicator. This pin is an open-drain output pin. Connect to a source voltage through an external pullup resistor between 10 kΩ to 100 kΩ, the recommended max pull up voltage is 15V.
7	BST	P/I	Power supply for the high-side power MOSFET gate driver. Must connect a ceramic capacitor between BST pin and SW pin, prefer a high-quality 10-nF 50-V X7R ceramic capacitor.
8	SW	P	Switching node of the buck converter. Connect to the power inductor.
9	Thermal Pad	—	No internal electrical connection, must be grounded in PCB layout with a large copper plane to reduce thermal resistance.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature unless otherwise noted

DESCRIPTION	PARAMETER	MIN	MAX	UNIT
Input voltage	VIN, EN to GND	–0.3	105	V
	FB, RON to GND	–0.3	6.5	
Bootstrap capacitor	External BST to SW capacitance	2.2	100	nF
Output voltage	BST to GND	–0.3	111	V
	BST to SW	–0.3	6	
	SW to GND	–1.5	105	
	SW to GND (20-ns transient)	–3	106	
	PG to GND	–0.3	17	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

7.2 ESD Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)		±2000	V
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(1)		±500	V

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

7.3 Recommended Operating Conditions

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	6		100	V
V_{SW}	Switch node voltage			100	V
$V_{EN/UVLO}$	Enable voltage			100	V
I_{LOAD}	Load current		0.5	0.55	A
F_{SW}	Switching frequency			300	kHz

C_{BST}	External BST to SW capacitance		10		nF
t_{ON}	Programmable on-time	200		10000	ns
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

PARAMETER	THERMAL METRIC	eSOP-8L	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W

7.5 Electrical Characteristics

V_{IN}=48V $V_{EN/UVLO}$=2V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Supply Current						
V_{IN}	Operating input voltage		6.5		100	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		6.35	6.8	V
	Hysteresis			350		mV
I_{SD}	VIN shutdown current	V_{EN} = 0 V		5.3	11.5	µA
$I_{Q-SLEEP}$	VIN sleep current	V_{FB} = 1.5 V, Iload=0A, Non-switching(GBI1A11)		30	99	µA
		V_{FB} = 1.5 V, Iload=0A, Non-switching(GBI1A10)		422	658	uA
Power MOSFETS						
$R_{DSON-HS}$	High-side MOSFET R_{DSON}	I_{SW} = –100 mA		530		mΩ
$R_{DSON-LS}$	Low-side MOSFET R_{DSON}	I_{SW} = 100 mA		230		mΩ
EN/UVLO						
$V_{EN-RISING}$	Buck enable threshold	$V_{EN/UVLO}$ rising	1.37	1.5	1.65	V
$V_{EN-FALLING}$	Buck enable threshold	$V_{EN/UVLO}$ falling	1.28	1.4	1.52	V
Feedback and Current Limits						
V_{REF}	FB regulation voltage	V_{FB} falling	1.188	1.2	1.212	V
I_{LIM_HSD}	HSD switch current limit		0.69	0.75	0.84	A

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{LIM_LSD}	LSD switch current limit		0.44	0.55	0.65	A
I_{LIM_NEG}	Negative current limit	GBI1A00	-1.2	-2.3	-3.0	A
Timing and Soft Start						
t_{ON1}	On-time1	V_{VIN} = 7 V, R_{RON} = 75 kΩ		4200		ns
t_{ON3}	On-time2	V_{VIN} = 12 V, R_{RON} = 75 kΩ		2600		ns
T_{SS}	Soft-start time	10% to 90% output	1.45	3	4.78	ms
PG (Power Good)						
V_{TH_PG}	PG threshold	V_{FB} rising (good)	92	95	98	%
		V_{FB} falling (fault)	87	90	93	%
I_{LK_PG}	PG leakage current	V_{PG}=6V		10		nA
V_{PG_L}	PG low level output voltage	I_{PG_pullup}=2mA, V_{FB}=1V		0.06	0.11	V
Bootstrap						
$V_{BST-UVLO}$	Gate drive UVLO	V_{BST} rising		3.5	3.97	V
Protections						
T_{SD}	Thermal shutdown threshold			160		°C
	Hysteresis			25		°C

7.6 Typical Characteristics

V_{IN}=48V, T_A= 25°C, unless otherwise noted.

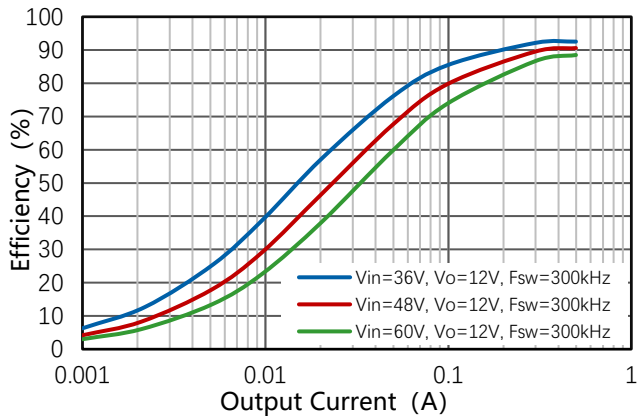


Figure 7-1. Power Efficiency GBI1A00

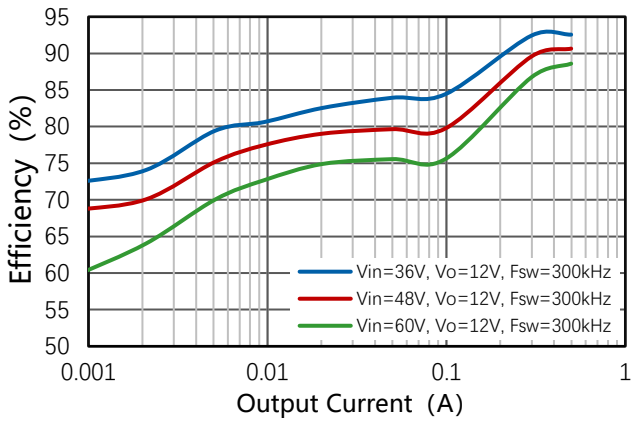


Figure 7-2. Power Efficiency GBI1A01

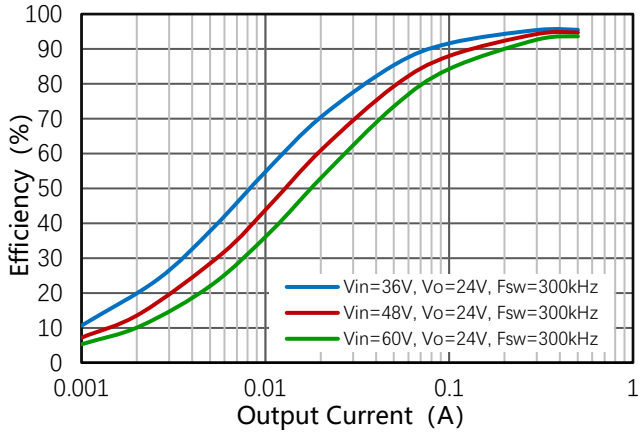


Figure 7-3. Power Efficiency GBI1A00

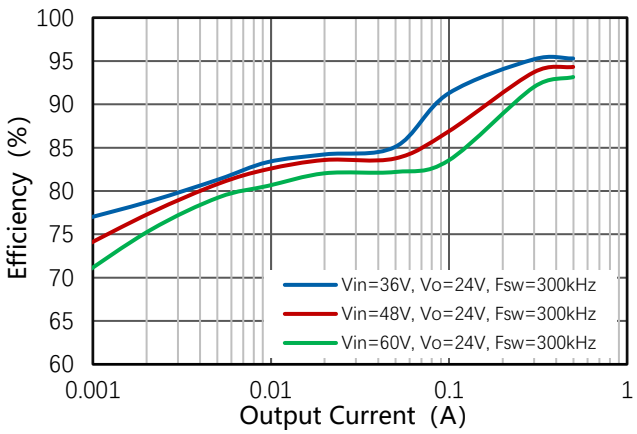


Figure 7-4. Power Efficiency GBI1A01

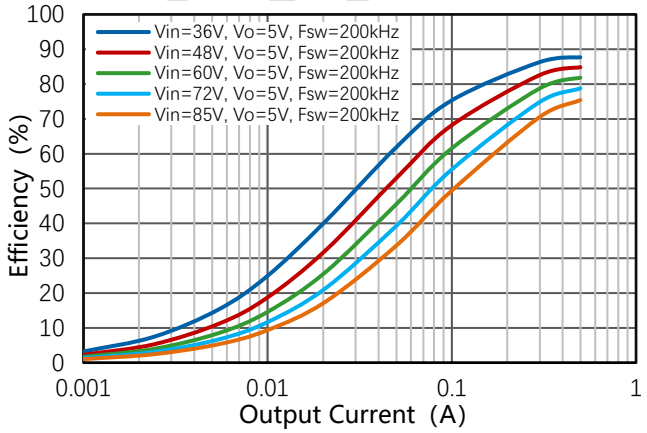


Figure 7-5. Power Efficiency GBI1A00

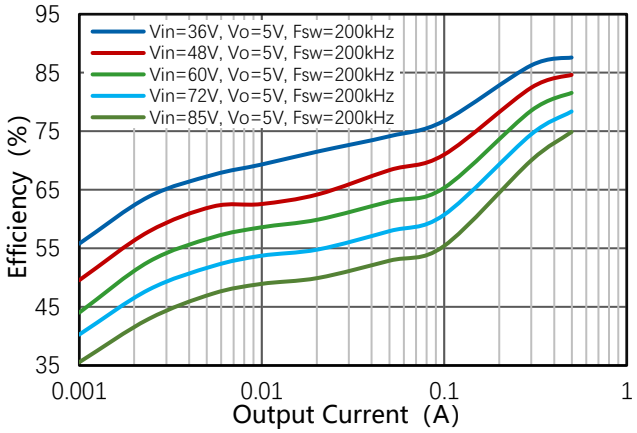


Figure 7-6. Power Efficiency GBI1A01

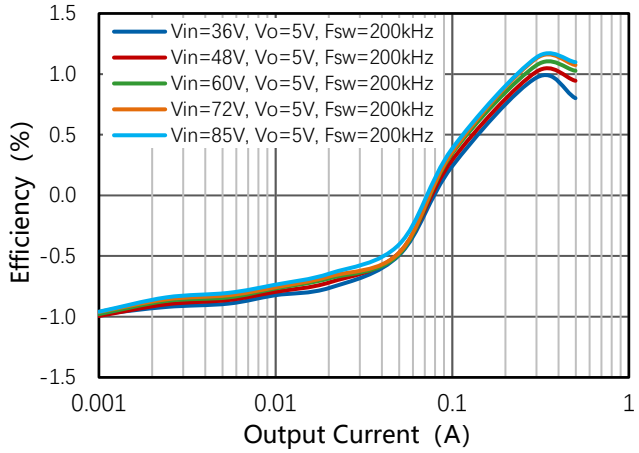


Figure 7-7. Load Regulation GBI1A10

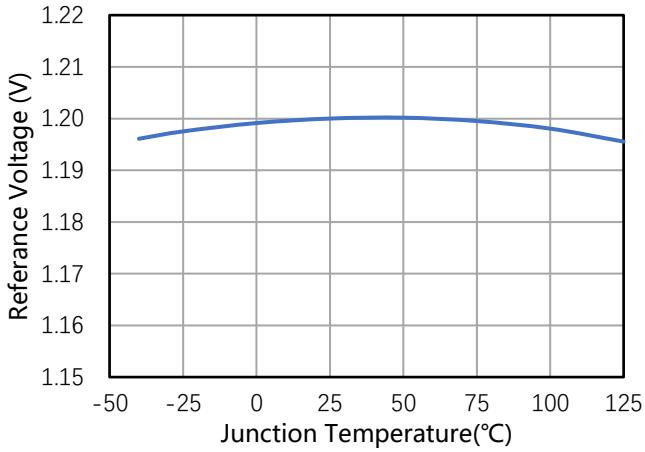


Figure 7-8. V_{FB} vs Junction Temperature

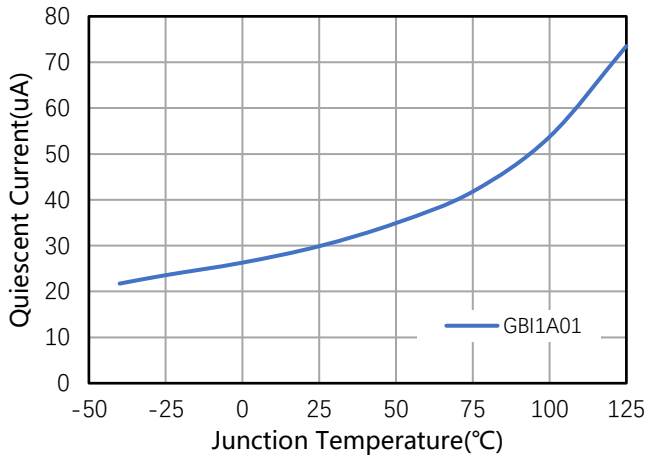


Figure 7-9. IQ Current vs Junction Temperature

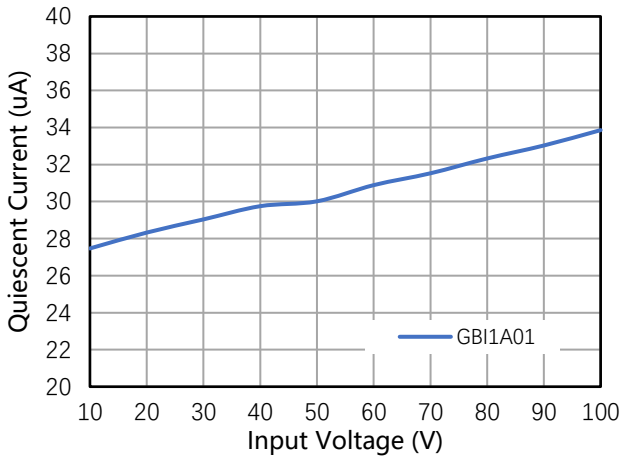


Figure 7-10. IQ Current vs Input Voltage

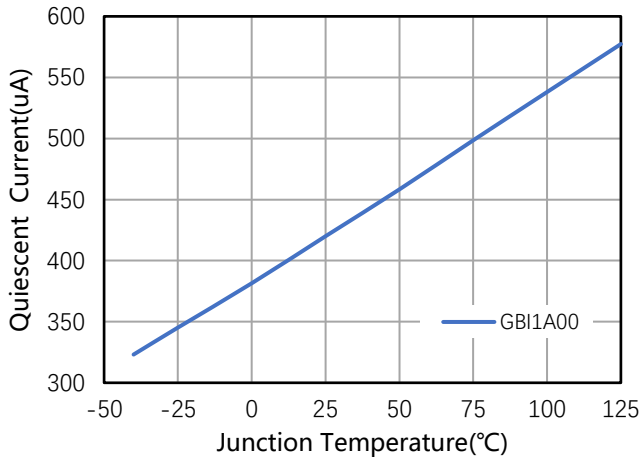


Figure 7-11. IQ Current vs Junction Temperature

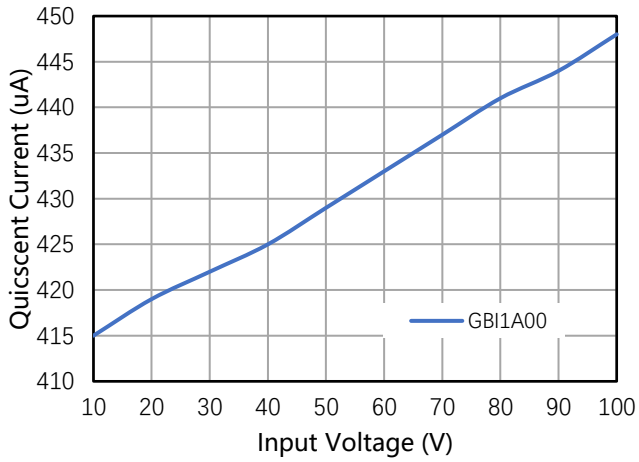


Figure 7-12. IQ Current vs Input Voltage

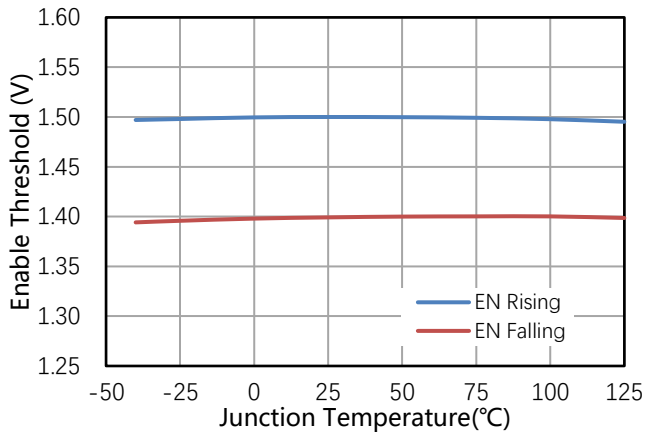


Figure 7-13. EN Threshold vs Junction Temperature

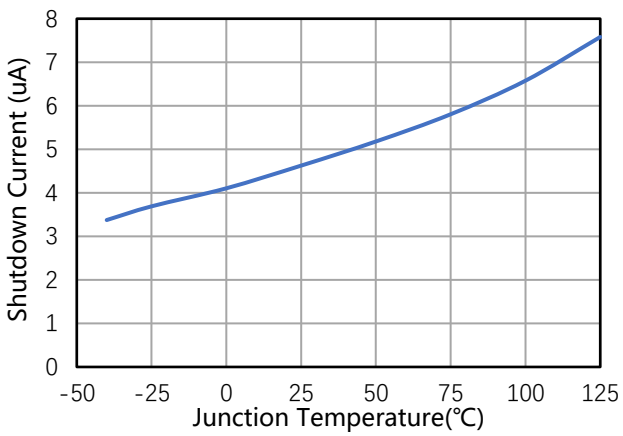


Figure 7-14. Shutdown Current vs Junction Temperature

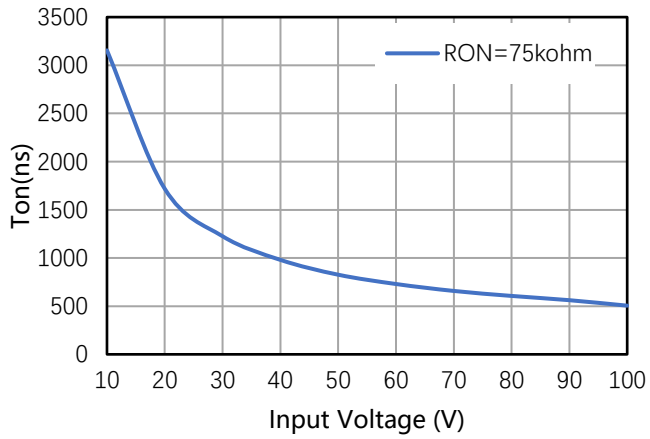


Figure 7-15. COT On-Time vs Input Voltage

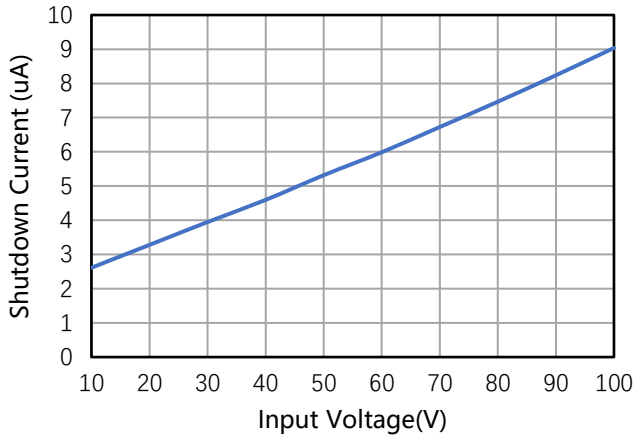


Figure 7-16. Shutdown Current vs Input Voltage

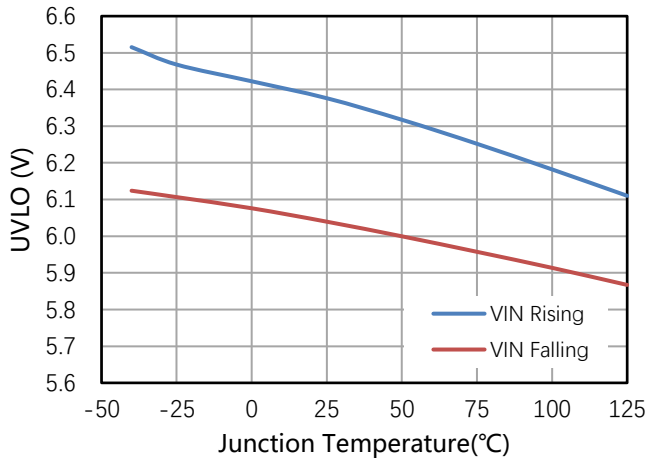


Figure 7-17. Input UVLO vs Junction Temperature

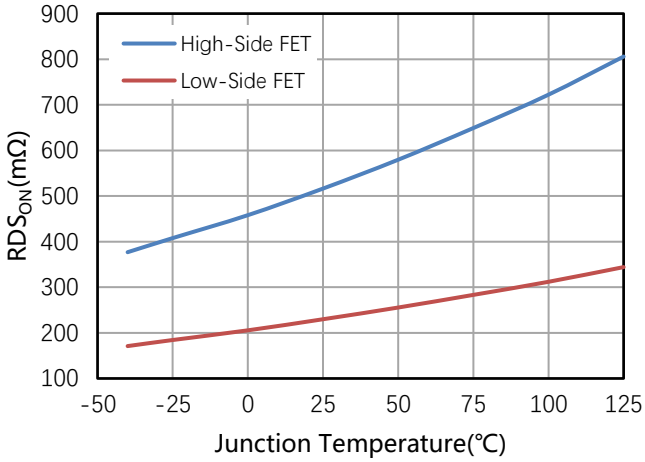


Figure 7-18. On Resistance vs Junction Temperature

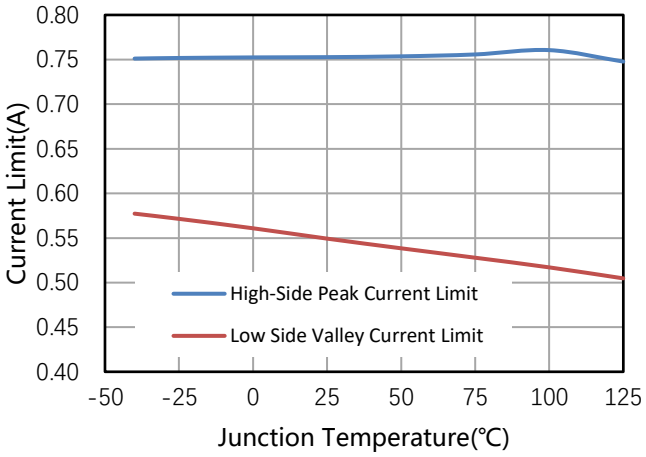


Figure 7-19. Current limit vs Junction Temperature (Normal operation)

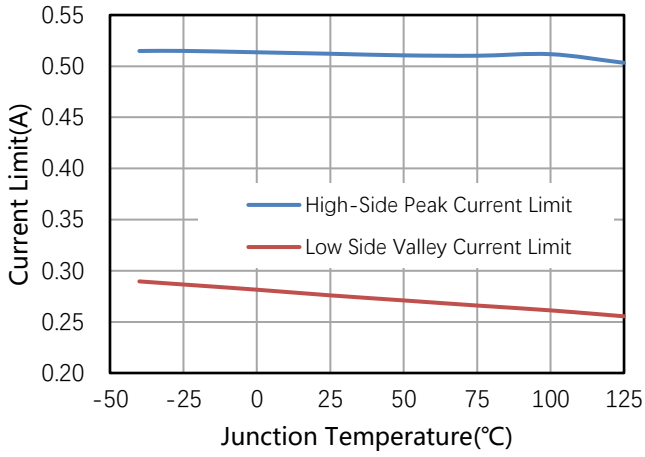


Figure 7-20. Current limit vs Junction Temperature (Hard-short condition)

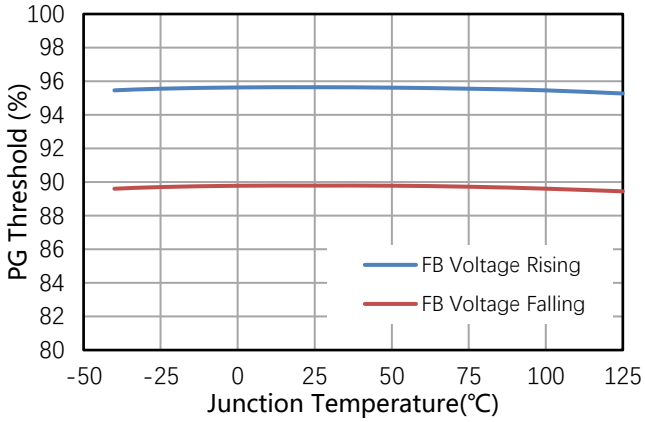


Figure 7-21. PG Threshold vs Junction Temperature

8 FUNCTION BLOCK DIAGRAM

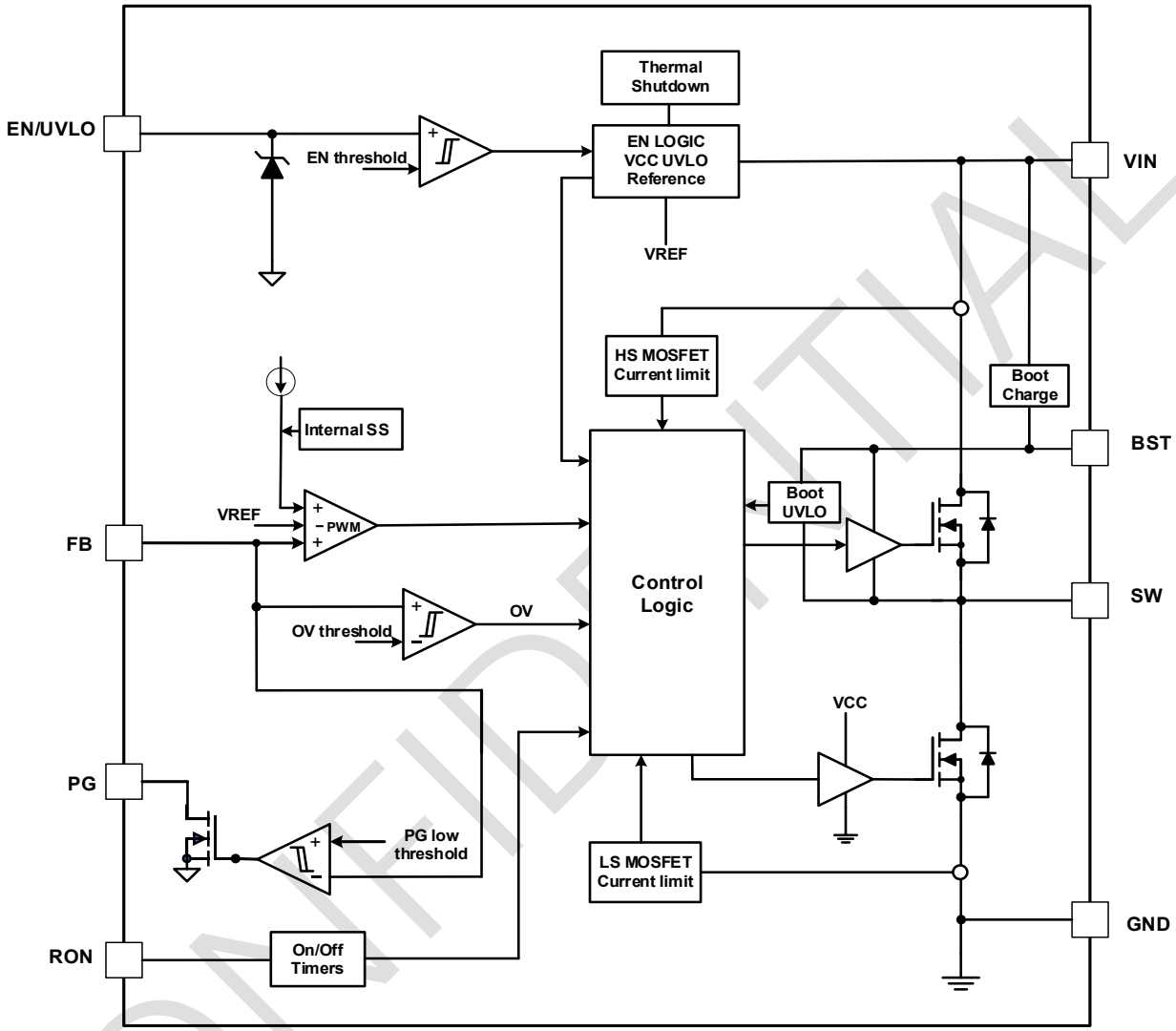


Figure 8-1 GBI1A00 and GBI1A01 Functional Block Diagram

9 DETAILED DESCRIPTION

9.1 Overview

The GBI1A00 and GBI1A01 are an easy-to-use, highly efficient synchronous step-down buck converter with a wide input voltage of 6 V to 100 V, delivering up to 0.5 A DC load current. With integrated high-side and low-side power MOSFETs, the GBI1A00 and GBI1A01 are designed with constant on-time (COT) control architecture, this constant on-time (COT) converter is ideal for low-noise, high current, and fast load transient requirements, operating with a predictive on-time switching pulse.

The GBI1A00 and GBI1A01 implements a smart peak and valley current limit detection circuit to ensure robust protection during output short circuit conditions. Control loop compensation is not required for this regulator, reducing design time and external component count.

For GBI1A01, at light loads the device transitions into an ultra-low IQ mode to maintain high efficiency and prevent draining battery cells connected to the input when the system is on standby. For GBI1A00, at light loads the device still works in CCM mode which achieves the lower output voltage ripple at full loading range.

The GBI1A00 and GBI1A01 incorporate additional features for comprehensive system requirements, including an open-drain Power Good circuit for power-rail sequencing and fault reporting, internally-fixed soft start, monotonic start-up into pre-biased loads, precision enable for programmable line undervoltage lockout (UVLO), smart cycle-by-cycle current limit for optimal inductor sizing, and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications.

The GBI1A00 and GBI1A01 are available in the 8-pin e-SOP package.

9.2 Control Mode Architecture

The GBI1A00 and GBI1A01 adopt a constant on time (COT) control architecture providing fast load transient response. The COT control mode sets a fixed on-time t_{ON} of the high-side FET using a timing resistor R_{RON}, and is inversely proportional to the input voltage, VIN. The inverse relationship with VIN results in a nearly constant frequency as VIN is varied.

Calculate the on-time using Equation 1.

$$t_{ON}(us) = \frac{R_{RON}(k\Omega)}{2.5 \times V_{IN}(V)} \quad (1)$$

After expiration of t_{ON}, the high side MOFET turns off and the low-side MOSFET turns on after dead time passes, until the feedback voltage is lower than the reference voltage of 1.2 V, the low side MOSFET turns off and high side MOSFET turns on again after dead time passes. To set a CCM specific switching frequency, the R_{RON} resistor is selected as below Equation 2.

$$R_{RON}(k\Omega) = \frac{V_{OUT}(V) \times 2500}{F_{SW}(kHz)} \quad (2)$$

Select R_{RON} for a minimum on-time (at maximum VIN) greater than 200 ns for proper operation. In addition to this minimum on-time, the maximum frequency for this device is limited to 300kHz.

9.3 Light Load Operation

The GBI1A00 and GBI1A01 integrate both high-side and low-side power MOSFETs. For GBI1A01, at light loads the device works in pulse skip mode to maintain high efficiency and prevent draining battery cells connected to the input when the system is in standby. For GBI1A00, at light loads the device still works in CCM mode which achieves the lower output voltage ripple at full loading range.

The GBI1A01 operates in a pulse-skipping mode during light load conditions. When the inductor valley current reaches zero, the low-side MOSFET turns off. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. This mode leads to a reduction in the average switching frequency at light loads, switching losses and FET gate driver losses, both of which are proportional to switching frequency, are significantly reduced at very light loads and efficiency is improved.

9.4 External Ripple Injection

For constant on time (COT) control mode, in order to maintain stability, the PWM comparator requires a minimal ripple voltage in feedback node that is in phase with the inductor current during the off-time. Furthermore, this ripple voltage in feedback node during the off-time must be large enough to dominate any noise present at the feedback node. The minimum recommended ripple voltage is 30 mV. There are 3 different methods for generating voltage ripple at the feedback node.

9.4.1 Recommended Ripple Injection Circuit

Type-3 ripple generation circuit is recommended to generate the minimum ripple requirement for COT control mode stable. This circuit is suited for applications where low output voltage ripple is critical. As shown in Figure 9-1, an RC network consisting of R_r and C_r, and the switch node voltage to generate a triangular ramp which is in-phase with the inductor current, and AC-coupled into the feedback node with capacitor C_b.

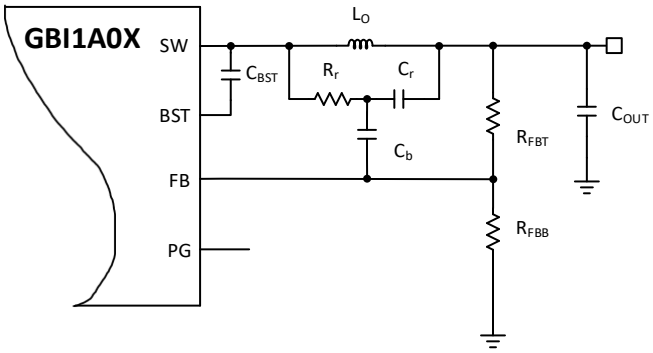


Figure 9-1. Type-3 Ripple Generation Circuit

Equation 3, 4 and 5 are used to determine the external component choice.

$$C_r \geq \frac{10}{F_{SW} \times (R_{FBT} \,||R_{FBB})} \tag{3}$$

$$R_r C_r \leq \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{30mV} \tag{4}$$

$$C_b \geq \frac{t_{settling}}{3 \times R_{FBT}} \tag{5}$$

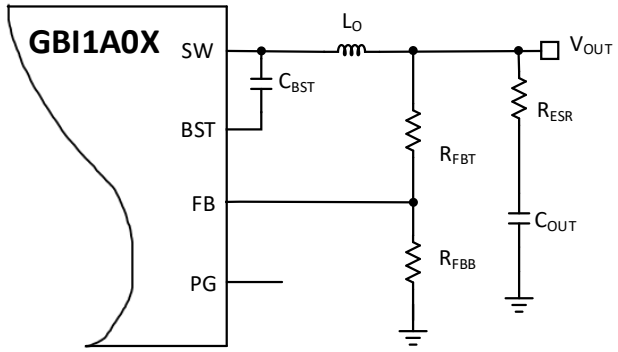
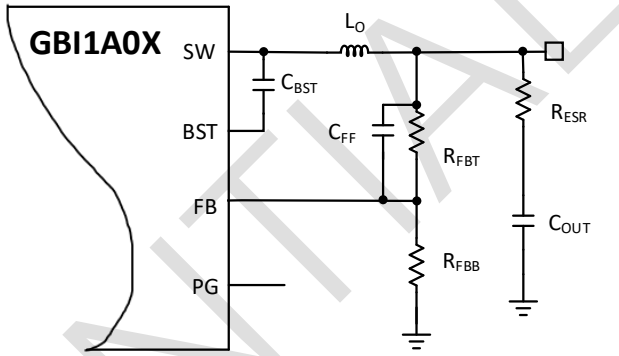
Where

- $t_{settling}$ is desired load transient response settle time
- t_{ON} is the HSFET on time determined by R_{RON}

9.4.2 Other Ripple Injection Circuits

There are other two ripple injection circuits shown in table 1.

Table 9-1. Ripple Injections Circuits with Larger Output Ripple

Type-1	Type-2
	
$R_{ESR} \geq \frac{30mV \times V_{OUT}}{R_{FBT} \times \Delta I_L}$ (6)	$C_{FF} \geq \frac{V_{OUT}}{2\pi \times F_{SW} \times (R_{FBT} \,\|\|\, R_{FBB})}$ (8)
$R_{ESR} \geq \frac{V_{OUT}}{2 \times V_{IN} \times F_{SW} \times C_{OUT}}$ (7)	$R_{ESR} \geq \frac{V_{OUT}}{2 \times V_{IN} \times F_{SW} \times C_{OUT}}$ (9)
	$R_{ESR} \geq \frac{30mV}{\Delta I_L}$ (10)

The type-1 ripple generation circuit uses a single resistor, R_{ESR} in series with the output capacitor or uses a larger ESR output capacitor. The generated voltage ripple has two components, capacitive ripple caused by the inductor ripple current charging and discharging the output capacitor and resistive ripple caused by the inductor ripple current flowing into the output capacitor and through series resistance R_{ESR}. The capacitive ripple component is out of phase with the inductor current and does not decrease monotonically during the off-time. The resistive ripple component is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at VOUT for stable operation. Equation (6) and Equation (7) are used to calculate the value of the R_{ESR}.

The type-2 ripple generation circuit adds a feedforward capacitor C_{FF} based on type-1 ripple generation circuit, which makes the output voltage ripple AC-coupled to the feedback node directly, and the output voltage ripple to feedback node are reduced by a factor of V_{OUT} / $V_{FBT.}$ Equation (8), Equation (9) and Equation (10) are used to calculate the value of the R_{ESR} and C_{FF}.

As shown in table 1, both type-1 and type-2 method have an additional R_{ESR} is series with the output capacitor, which leads the output voltage ripple is higher than the type -3 method.

9.5 Internal Soft Start

To avoid the current surges during start-up, the GBI1A00 and GBI1A01 employs an internal soft-start circuit which allows the output voltage reaches a target point gradually, followed by the internal reference ramp. The soft-start time is internally set to 3 ms.

9.6 Internal VCC Regulator and Bootstrap Capacitor

The GBI1A00 and GBI1A01 integrate an internal linear regulator with a nominal output of 5 V, and no need for an external capacitor to stabilize the linear regulator. The internal VCC regulator provides the power to the MOSFET driver and logic circuits.

An external bootstrap capacitor between BST pin and SW pin powers high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off. It is required to select a high-quality 10nF 50-V X7R ceramic bootstrap capacitor as specified in the Absolute Maximum Ratings.

The floating supply (BST to SW) UVLO threshold is 3.7V rising and hysteresis of 200mV. When the converter operates with high duty cycle or prolongs in sleep mode for a certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 3.5V, BOOT UVLO occurs.

9.7 Enable/Undervoltage Lockout (EN/UVLO)

The EN/UVLO pin of GBI1Ax is a high voltage pin which can be connected to VIN directly to start-up the device. If the EN/UVLO voltage is lower than 1.5 V (typical), the converter is in shutdown status and all functions disabled. If the EN/UVLO voltage is higher than 1.5 V, the buck starts-up.

For Under Voltage Lock Out (UVLO) function control, connect an external resistor divider (RL and RH) shown in Figure 9-2 from VIN to EN/UVLO pin. The VIN UVLO rising and falling threshold can be calculated by Equation 11 and Equation 12 respectively.

$$V_{rise} = 1.5 \times (1 + \frac{R_H}{R_L}) \quad (11)$$

$$V_{fall} = 1.4 \times (1 + \frac{R_H}{R_L}) \quad (12)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

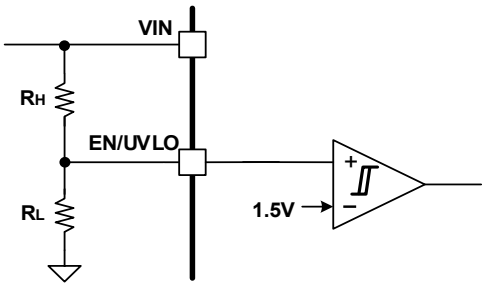


Figure 9-2. System UVLO by EN divider

When using the GBI1A01, for achieving higher light load efficiency, it is recommended to select R_H and R_L in the range of 1 MΩ for most applications.

9.8 Power Good (PG)

The Power good (PG) pin is an open-drain output to indicate when the output voltage is within the regulation level. When the FB voltage exceeds 95% of the internal reference VREF, the internal PG switch turns off and PG can be pulled high by the external pullup. If the FB voltage falls below 90% of VREF, an internal PG switch turns on and PG is pulled low to indicate that the output voltage is out of regulation. A 10 kΩ-100 kΩ pullup resistor is recommended to pull the voltage up to 15V or less. The rising edge of PG has a built-in deglitch delay of about 5 µs.

9.9 Output Voltage Setup

The GBI1A00 and GBI1A01 regulate the internal reference voltage at 1.2V with ±1.5% tolerance over the operating temperature and voltage range.

The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 13 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the value is higher, the regulator will be more noise sensitive. R_{FB_BOT} in the range of 10kΩ to 100kΩ is recommended for most application.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{1.2V} - 1\right) * R_{FB\_BOT} \quad (13)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

9.10 Overcurrent and Short Circuit Protection

The GBI1A00 and GBI1A01 integrates the cycle-by-cycle overcurrent protections, both inductor peak and valley current are sensed during each cycle. At every switching cycle, the current sensed in the high-side MOSFET is compared to the current limit threshold I_{peak} Limit. As shown in Figure 9-3, if the peak current in the high-side MOSFET is larger than 0.75 A (typical), the high-side MOSFET turns off immediately and the low-side MOSFET turns on. The fold-back valley current limit I_{valley} Limit is 0.55A (typical), at every switching cycle, the low-side MOSFET remains on until the inductor current drops below the fold-back valley current limit. This feature lower down the switching frequency when over current happens, prevents overheating and limits the average output current to less than 0.75 A.

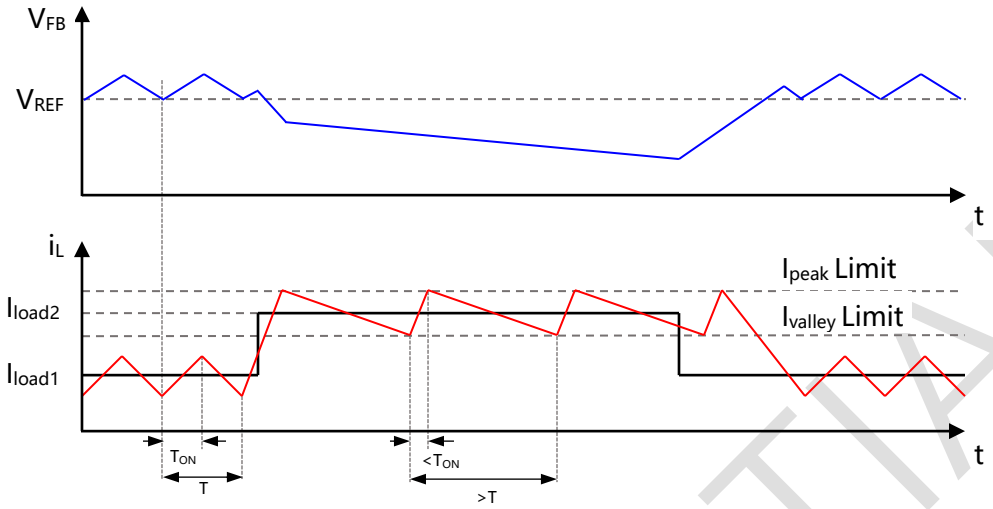


Figure 9-3. Current Limit Timing Diagram

When the output overcurrent or short circuit occurs, the converter cannot provide enough energy to satisfy loading requirement, then the output voltage drops, followed by the FB voltage. When the FB voltage drops to 25% of the reference voltage, both the I_{peak} Limit and $I_{vallley}$ Limit drop to half the original value, which is about 0.51A for high-side MOSFET current limit and 0.27A for low-side MOSFET current limit. This feature could avoid the overheating and other potential damages for the converter, also avoid the overheating of the inductor when overcurrent or short circuit occurs.

9.12 Thermal Protection

The GBI1A00 and GBI1A01 features an internal thermal shutdown circuit to protect the device from damage during excessive heat and power dissipation conditions. The thermal shutdown circuit will be asserted when the junction temperature exceeds typically 160ºC. When the junction temperature falls below 135ºC, the device restarts with internal soft start phase.

This is a non-latch protection, the GBI1A00 and GBI1A01 will re-start and out of thermal shutdown if the over temperature is gone.

10 APPLICATION INFORMATION

Typical Application 1

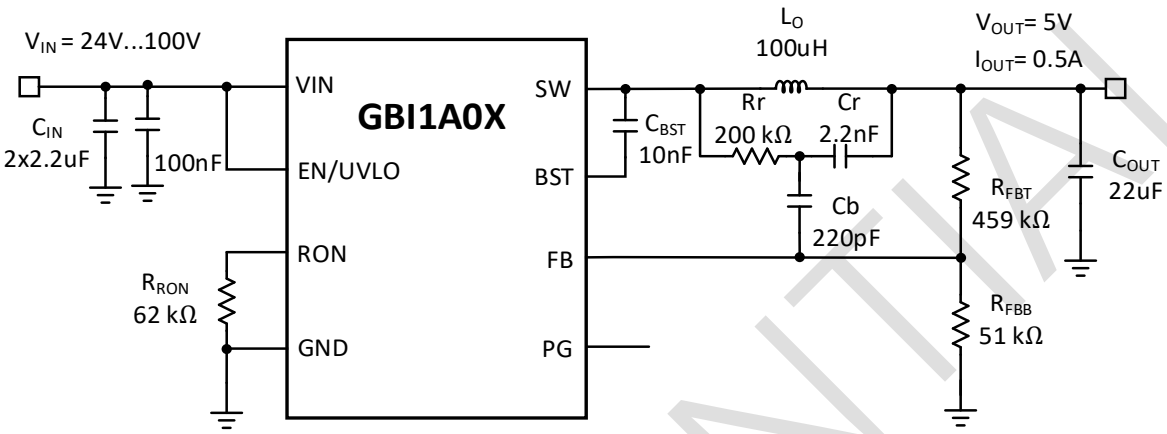


Figure 10-1. 48V Normal Input, 12V/0.5A Output

Table 10-1. Design Parameters

Design Parameters	Example Value
Input Voltage	48V(Normal), 24V -100V
Output Voltage	5V
Output Current	0.5A
Output Ripple	<25mV
Switching Frequency	200kHz

10.1 Set Output Voltage

The GBI1A00 and GBI1A01 output voltage can be easily set up using a resistor divider network R1 and R2 as shown in the typical application circuit Figure10-1. Use Equation (14) to calculate resistor divider values.

$$R1 = \frac{(V_{OUT} - 1.2) \times R2}{1.2} \tag{14}$$

In this design for example the Vout is 5V. Set the resistor R2 value to be approximately 51kΩ.

$$R1 = \frac{(V_{OUT} - 1.2) \times R2}{1.2} = \frac{(5 - 1.2) \times 51k\Omega}{1.2} = 162k\Omega$$

10.2 Set Switching Frequency (R_{RON})

The GBI1A00 and GBI1A01 switching frequency is set-up by placing on-time programming resistor from RON pin to GND. Use equation (2) in chapter 9.2. to calculate the resistor value. The 62 kΩ, 1% resistor sets the switching frequency at 200 kHz.

$$R_{RON}(k\Omega) = \frac{5 \times 2500}{200} = 62k\Omega$$

$$t_{ON}(us) = \frac{62}{2.5 \times 48} = 0.52us$$

10.3 Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. The high voltage rating X7R ceramic capacitors 2.2uF to 10μF are recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin. These capacitors must be rated with voltage larger than maximum input voltage, and are recommended with voltage rating of twice the maximum input voltage.

For this design, two 2.2uF X7R capacitors and one 0.1uF capacitor rated 100V are recommended.

The input voltage ripple can be calculated by using Equation 15 to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{0.5A}{4.4uF \times 200kHz} \times \frac{5V}{48V} \times \left(1 - \frac{5V}{48V}\right) = 53\ mV \tag{15}$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

10.4 Inductor Selection

The performance of the inductor affects the power supply' s steady state operation, transient behavior, loop stability, and buck converter efficiency. The critical parameters of inductor are the inductance, the DC resistance (DCR), the saturation current and the RMS current.

Use the following equation to calculate the minimum inductance:

$$L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (16)$$

Where

- V_{OUT} is output voltage
- K_{IND} is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.3-0.5 is recommended
- V_{INMAX} is the maximum input voltage
- f_{SW} is the converter switching frequency
- I_{OUT} is the output current

In this design example:

$$L > L_{MIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} = \frac{5V \times (48V - 5V)}{48V \times 0.5 \times 0.5 \times 200kHz} = 89uH \quad (17)$$

When selecting an inductor, choose its rated current is larger than its RMS current and saturation current is larger than short circuit current I_{LIM_HSD} during the operation. The peak switching current of inductor is calculated in equation 18:

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} = 0.5A + 0.5 \times \frac{0.5A}{2} = 0.625A \quad (18)$$

The inductance of 100uH and the saturation current of 1.8A is selected here.

10.5 Output Capacitor

The output capacitor must be chosen carefully with the reason that this capacitor value determines the regulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. Generally, choose a low-ESR output capacitor like a ceramic capacitor from X5R or X7R family to get small output voltage ripple.

From the required output voltage ripple, use Equation 19 to calculate the minimum required effective capacitance, C_{OUT}.

$$C_{OUT} > \frac{\Delta I_{LPP}}{8 \times V_{OUT\_Ripple} \times f_{SW}} = \frac{K_{IND} \times I_{OUT}}{8 \times V_{OUT\_Ripple} \times f_{SW}} \quad (19)$$

The allowed maximum ESR of the output capacitor is calculated by the equation 20.

$$R_{ESR} < \frac{V_{OUT\_Ripple}}{k_{IND} \times I_{OUT}} \quad (20)$$

Where

- V_{OUT_Ripple} is output voltage ripple caused by charging and discharging of the output capacitor.
- k_{IND} is the Ripple Ration of the inductor ripple current ($\Delta iL/I_{OUT}$), 0.3-0.5 is recommended here
- I_{OUT} is the maximum output current
- f_{SW} is the converter switching frequency.

In this design, V_{OUT_Ripple} is smaller than 25mV, f_{SW} is 200kHz, I_{OUT} is 0.5A and K_{IND} is 0.5:

$$C_{OUT} > \frac{0.5 \times 0.5A}{8 \times 25mV \times 200kHz} = 6.25uF \quad (21)$$

$$R_{ESR} < \frac{25mV}{0.5 \times 0.5A} = 100m\Omega \quad (22)$$

As the DC bias degrading and ±10% or ±20% tolerance for the ceramic capacitors, a X7R capacitors of one 22uF with 25V DC rating is selected.

10.6 Bootstrap Capacitor

For proper operation of the device, a 10nF ceramic capacitor of X5R or X7R must be placed between the SW pin to the BST pin. The DC rating of this capacitor must be 10V or higher voltage level. If the VIN voltage is larger than 80V , it is recommended to add a 18Ω boot resistor in series with the bootstrap capacitor.

10.7 Ripple Injection Circuit

For keeping lower output voltage ripple, the Type 3 ripple injection circuit is selected here.
Refer to Equation (3), Equation (4) and Equation (5), calculating the C_r, R_r and C_b as below:

$$C_r \geq \frac{10}{200kHz \times (R_1 \,||R_2\,)} = \frac{10}{300kHz \times (51k \,||162k)} = 1289pF \quad (23)$$

$$R_r C_r \leq \frac{(48V - 12V) \times 0.52us}{30mV} = 0.746 \times 10^{-3} \quad (24)$$

Keeping Rr in the range of 100kΩ to 1MΩ, choosing Cr is 2200pF and getting the Rr is 579kΩ. While for making sure a 30-mV minimum ripple voltage on FB at minimum VIN 24V, the Rr is selected with 200kΩ in the design.

$$C_b \geq \frac{t_{settling}}{3 \times R_{FBT}} = \frac{t_{settling}}{3 \times 162k\Omega} \quad (25)$$

where

- $t_{settling}$ is desired load transient response settling time

C_b calculates to 158 pF based on a 77μs settling time. A 220pF is selected in the design. To avoid capacitance fall-off with DC bias, use a C0G or NP0 dielectric capacitor for C_b.

10.8 Typical BOM Recommendation

Table 2 lists the recommended BOM for typical applications. It is recommended to work with switching frequency 200kHz if the input voltage is larger than 60V.

Considering the capacitor' s degrading under DC bias, it is recommended to leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF(≥25V) ceramic output capacitor work for most applications, if for achieving better load transient performance, two 22uF ceramic output capacitors are recommended. As described in 9.4, the ripple injection voltage is related to the R_{FBT} and R_{FBB}, so it is highly recommended to refer below table for BOM selection to avoid the unstable operation.

Table 10-2. Typical BOM For Fsw=200kHz (VIN>60V)

Vout	L	Cout	R_{RON}	R_{FBT}	R_{FBB}	Rr	Cr	Cb
5V	100uH	22uF(25V)	62k	162k	51k	200k	2.2n	220p
12V	180uH	22uF(25V)	150k	459k	51k	330k	2.2n	68p
24V	270uH	2x10uF(50V)	300k	969k	51k	500k	2.2n	47p

Table 10-2. Typical BOM For Fsw=300kHz (VIN<=60V)

Vout	L	Cout	R_{RON}	R_{FBT}	R_{FBB}	Rr	Cr	Cb
5V	68uH	22uF(25V)	41.2k	162k	51k	150k	2.2n	220p
12V	150uH	22uF(25V)	100k	459k	51k	200k	2.2n	68p
24V	220uH	2x10uF(50V)	200k	969k	51k	200k	2.2n	47p

10.9 Application Waveforms

Figure 10-2 to Figure 10-17 are tested based on Figure 10-1 with GBI1A00.

Vin=48V, Vout=5V, unless otherwise noted.

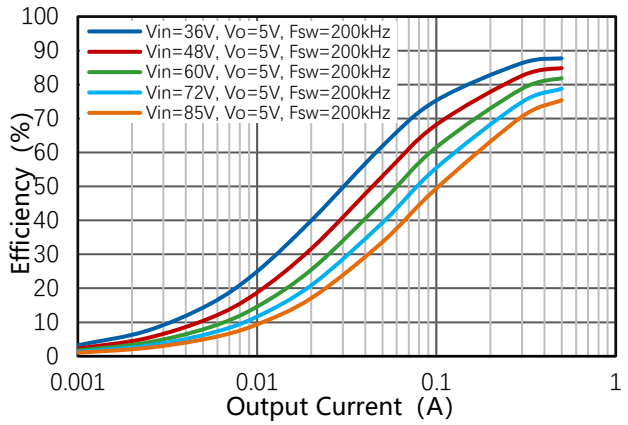


Figure 10-2. Power Efficiency

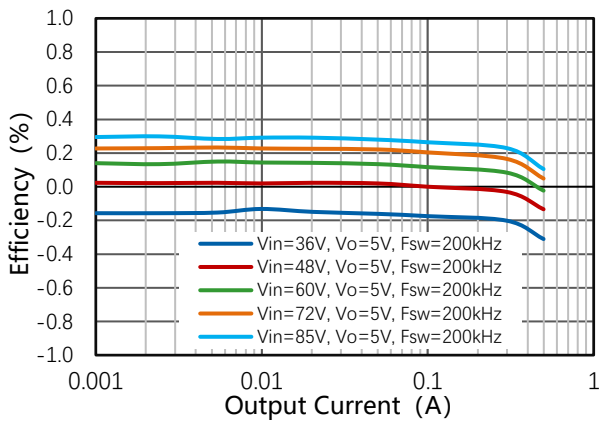


Figure 10-3. V_{OUT} Vs. Load Regulation

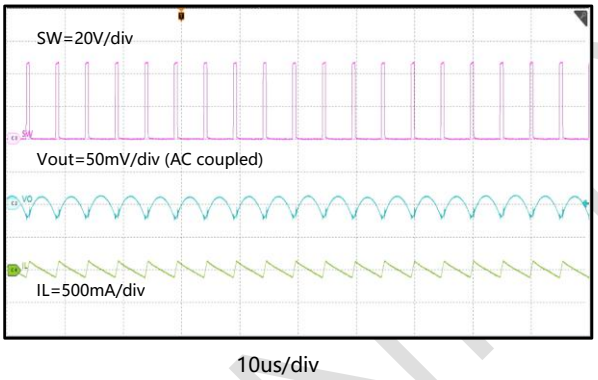


Figure 10-4. Output Voltage Ripple, I_{OUT}=0A

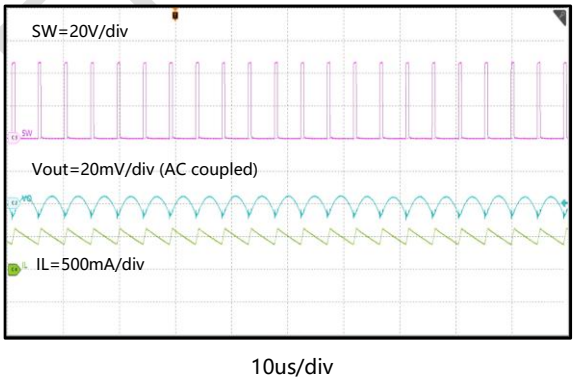


Figure 10-5. Output Voltage Ripple, I_{OUT}=0.5A

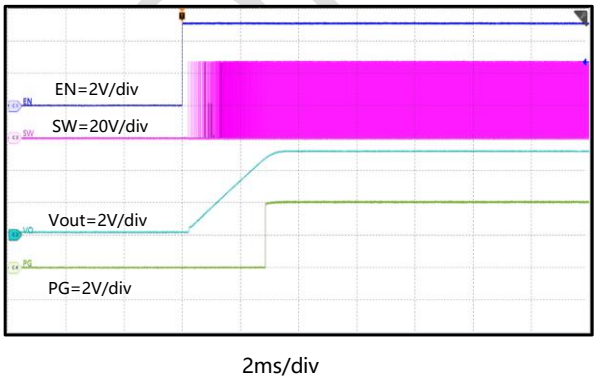


Figure 10-7. Start-Up with EN, I_{OUT}=0A

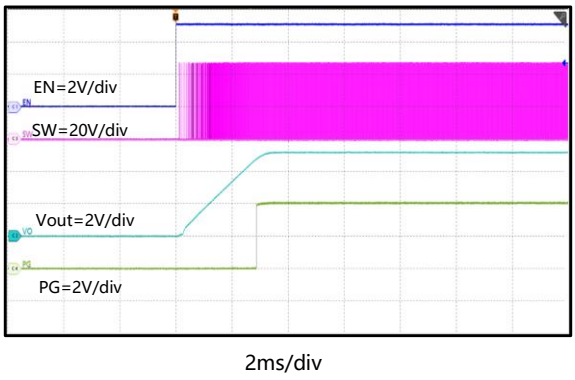
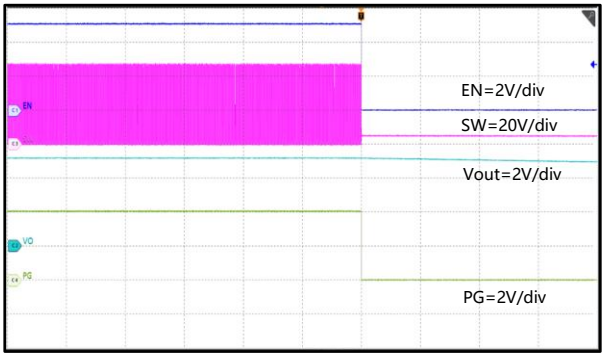
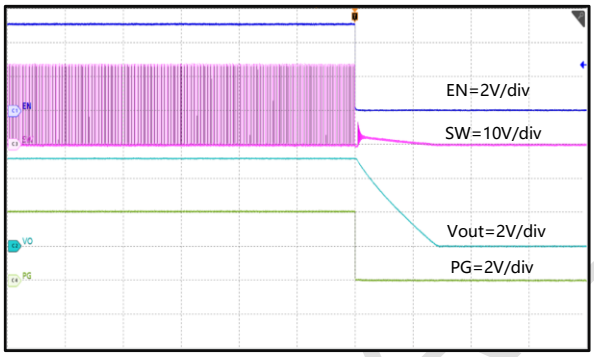


Figure 10-7. Start-Up with EN, I_{OUT}=0.5A



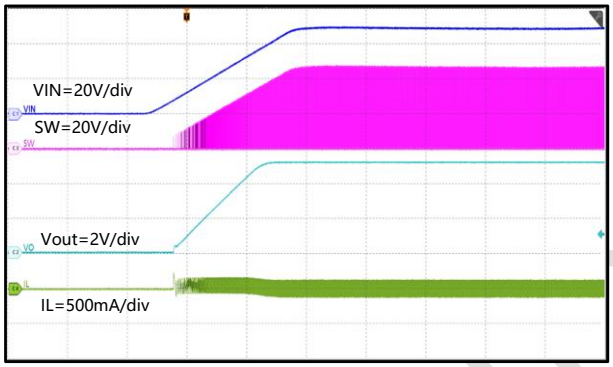
2ms/div

Figure 10-8. Shut-down with EN, I_{OUT}=0A



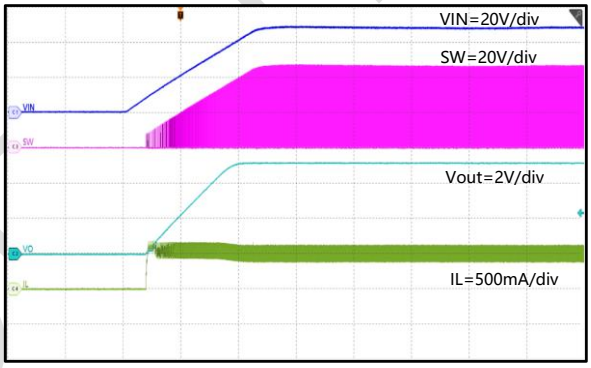
200us/div

Figure 10-9. Shut-down with EN, I_{OUT}=0.5A



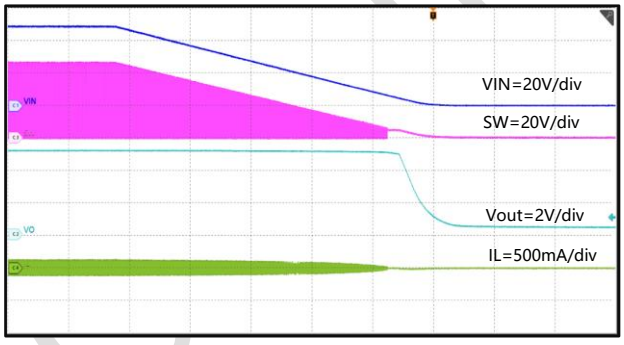
2ms/div

Figure 10-10. Start-Up with VIN rising I_{OUT}=0A



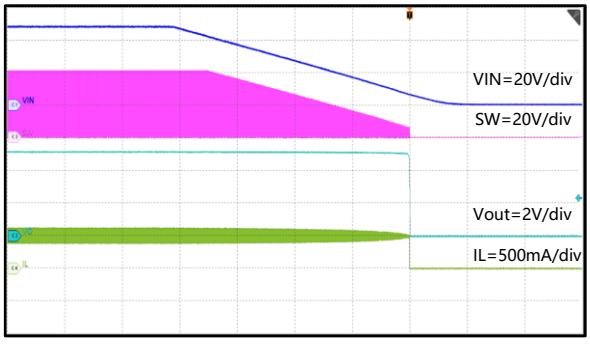
2ms/div

Figure 10-11. Start-Up with VIN Rising I_{OUT}=0.5A



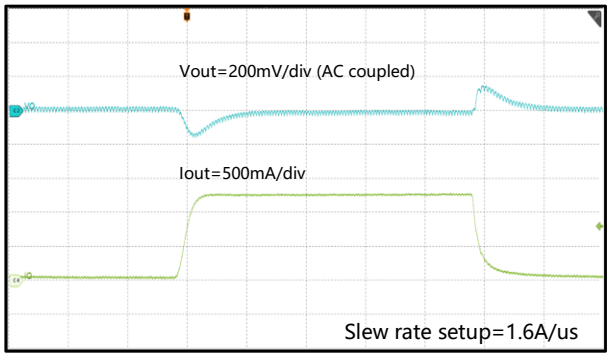
20ms/div

Figure 10-12. Shut-Down with VIN falling I_{OUT}=0A



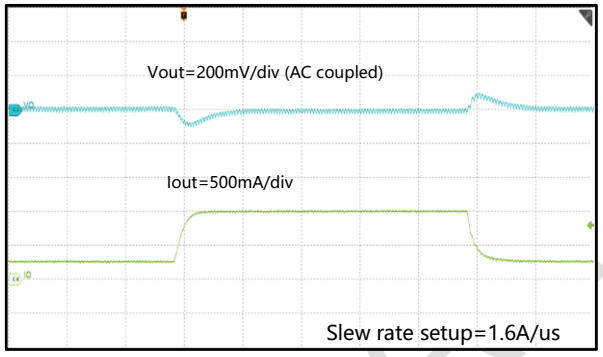
20ms/div

Figure 10-13. Shut-Down with VIN falling I_{OUT}=0.5A



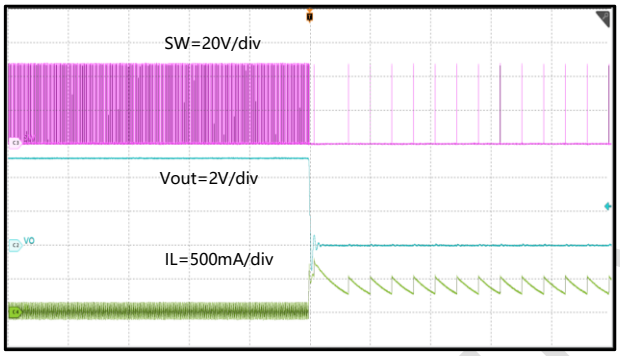
200us/div

Figure 10-14. Transient Response 0A-0.5A



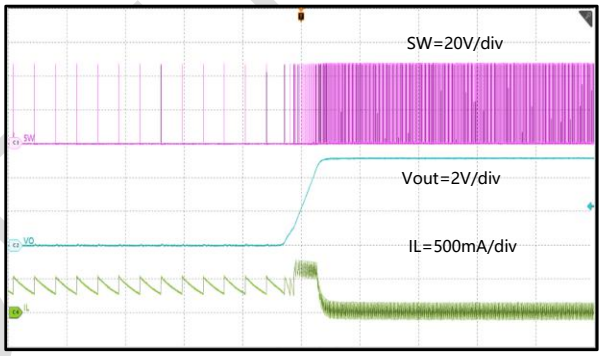
200us/div

Figure 10-15. Transient Response 0.1A-0.4A



400us/div

Figure 10-16. Normal Operation to Hard-short I_{OUT}=0A



400us/div

Figure 10-17. Hard-short Recover I_{OUT}=0A

Typical Application 2

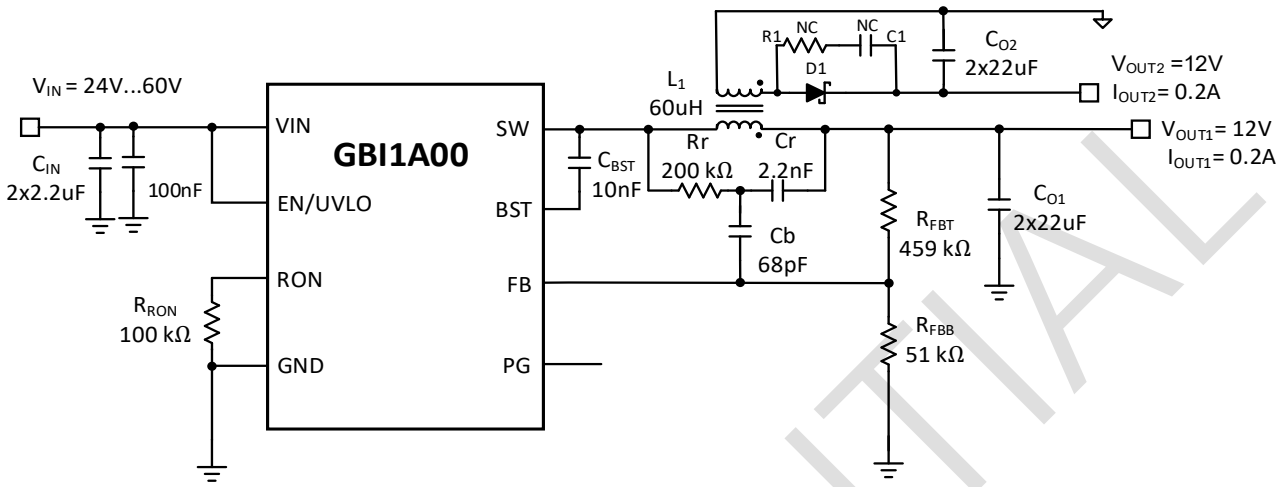


Figure 10-18. 48V Normal Input, Iso-buck 12V/0.2A Output

Table 10-3. Design Parameters

Design Parameters	Example Value
Input Voltage	48V(Normal), 24V -60V
Primary Output Voltage	12V
Primary Output Current	0.2A
Secondary Isolated Output Voltage	12V
Secondary Isolated Output Current	0.2A
Switching Frequency	300kHz

10.10 Output Setup and Transformer Turns Ratio

The primary output setup is same with normal Buck setup, refer to Equation 14 in chapter 10.1 for primary output voltage setup. The secondary isolated output depends on the turns ratio of the transformer.

$$V_{OUT2} = V_{OUT1} \times \frac{N_2}{N_1} - V_D \quad (26)$$

Where:

- $\frac{N_2}{N_1}$ is the transformer turns ratio
- V_D is the forward voltage of the rectifier diode D1

If the secondary (isolated) output voltage is significantly higher or lower than the primary output voltage, a turns ratio less than or greater than 1 is recommended. The primary output voltage is normally selected based on the input voltage range such that the duty cycle of the converter does not exceed 50% at the minimum input voltage. In this design, the turns ratio N2:N1 is selected as 1.

10.11 Rectifier Diode

When the high-side MOSFET turn on, the rectifier diode is reversed, the reverse voltage on the diode is below

$$V_R = (V_{IN} - V_{OUT1}) \times \frac{N_2}{N_1} + V_{OUT2} \quad (27)$$

If the input voltage (VIN) has transients above the normal operating maximum input voltage, then the worst-case transient input voltage must be used in calculation while selecting the secondary side rectifier diode. In this design, a 100V Schottky diode is selected.

10.12 Output Current Considerations

The secondary side only gets the energy from primary side when low-side MOSFET on, the current in primary side of the transformer need to be calculated as below,

$$I_{L1\_peak} = I_{M\_peak} = \frac{N_2}{N_1} \times I_{OUT2} + I_{OUT1} + \frac{\Delta I_M}{2} \quad (28)$$

$$\Delta I_M = \frac{(V_{IN} - V_{OUT1}) \times D}{F_{sw} \times L_1} \quad (29)$$

$$I_{L1\_peak\_N} = -\frac{\Delta I_M}{2} - \frac{N_2}{N_1} \times \frac{I_{O2}}{1-D} \quad (30)$$

Where:

- I_{M_peak} is the peak value of the magnetizing current in the transformer
- I_{L1_peak} is the peak current value in the primary side of the transformer
- ΔI_M is the peak-peak value of the magnetizing current in the transformer, which is same with primary side peak-peak current ΔI_{L1}
- $I_{L1\_peak\_N}$ is the negative peak current value of the primary side

In the actual design, below requirement should be meet,

$$I_{L1\_peak\_} < I_{LIM\_POS} = 0.75\text{A} \quad (31)$$

$$|I_{L1\_peak\_N}| < |I_{LIM\_NEG}| = 2.3\text{A} \quad (32)$$

10.13 Other Considerations

For the other external components selections, please refer to chapter 10. 2 to chapter 10.8.
In Figure10-18, R1 and C1 are parallelled with the rectifier diode D1, which is used to absorb the energy of the diode reverse recovery. If the noise in the design is not acceptable, the R1 and C1 can be considered. The recommended started value is 100Ω and 100pF, and needs to be reset based on the behavior of the rectifier diode.

10.14 Isolated Application Waveforms

Vin=48V, Vout=12V, Viso=12V, unless otherwise noted.

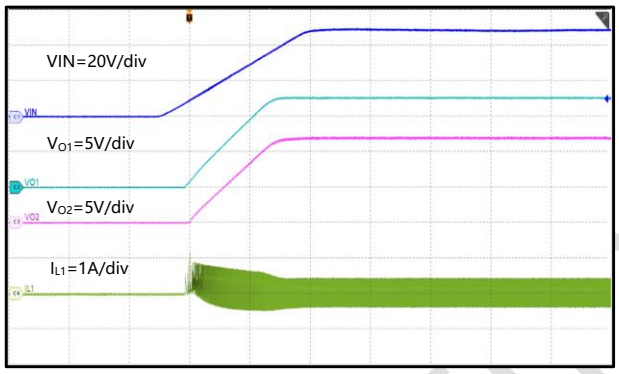


Figure 10-19. Start Up with VIN Rising
I_{O1}=0A, I_{O2}=0.2A

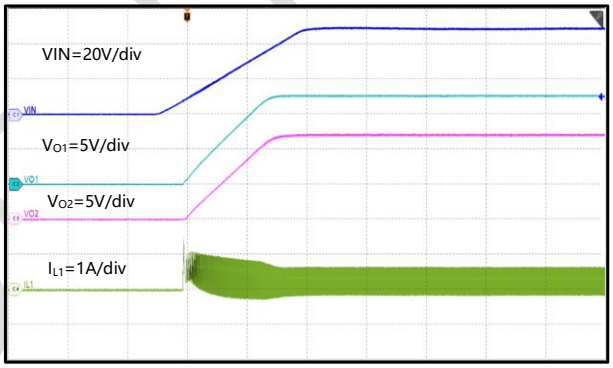


Figure 10-20. Start Up with VIN Rising
I_{O1}=0.2A, I_{O2}=0.2A

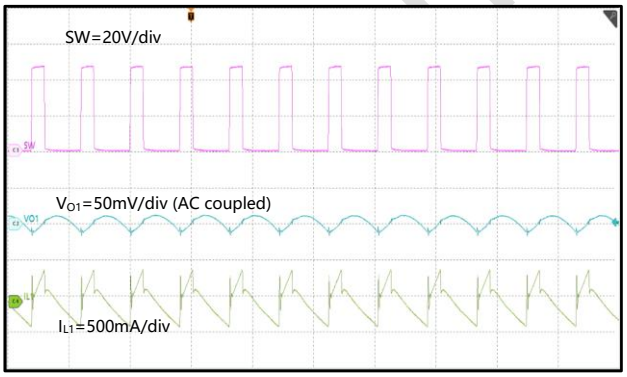


Figure 10-21. Steady State in Primary Side ,
I_{O1}=0A, I_{O2}=0.2A

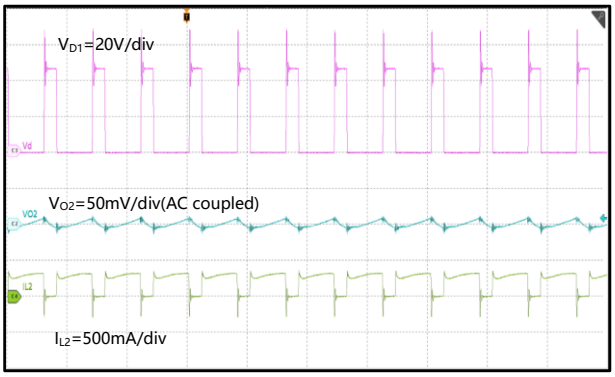


Figure 10-22. Steady State in Secondary Side ,
I_{O1}=0A, I_{O2}=0.2A

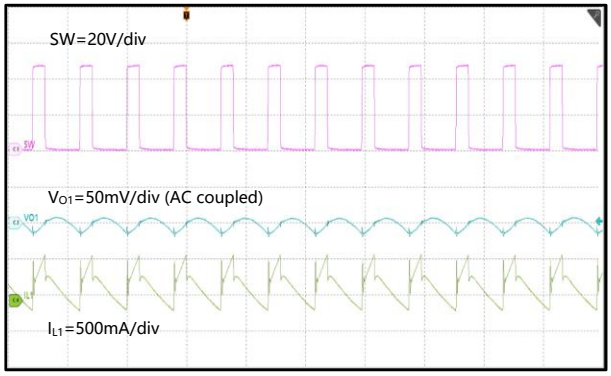


Figure 10-23. Steady State in Primary Side, I_{OUT1}=0.2A, I_{OUT2}=0.2A

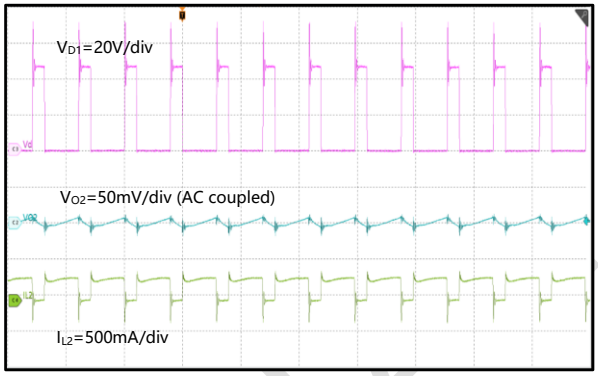


Figure 10-24. Steady State in Secondary Side, I_{OUT1}=0.2A, I_{OUT2}=0.2A

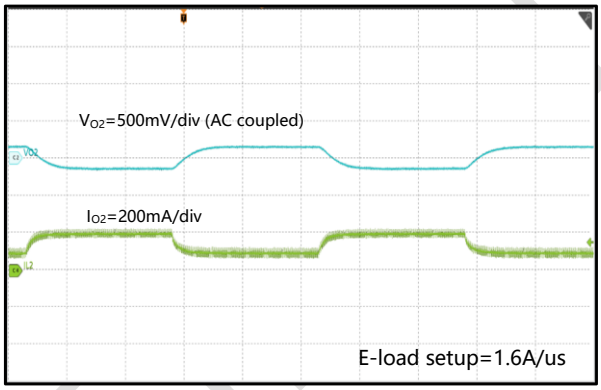
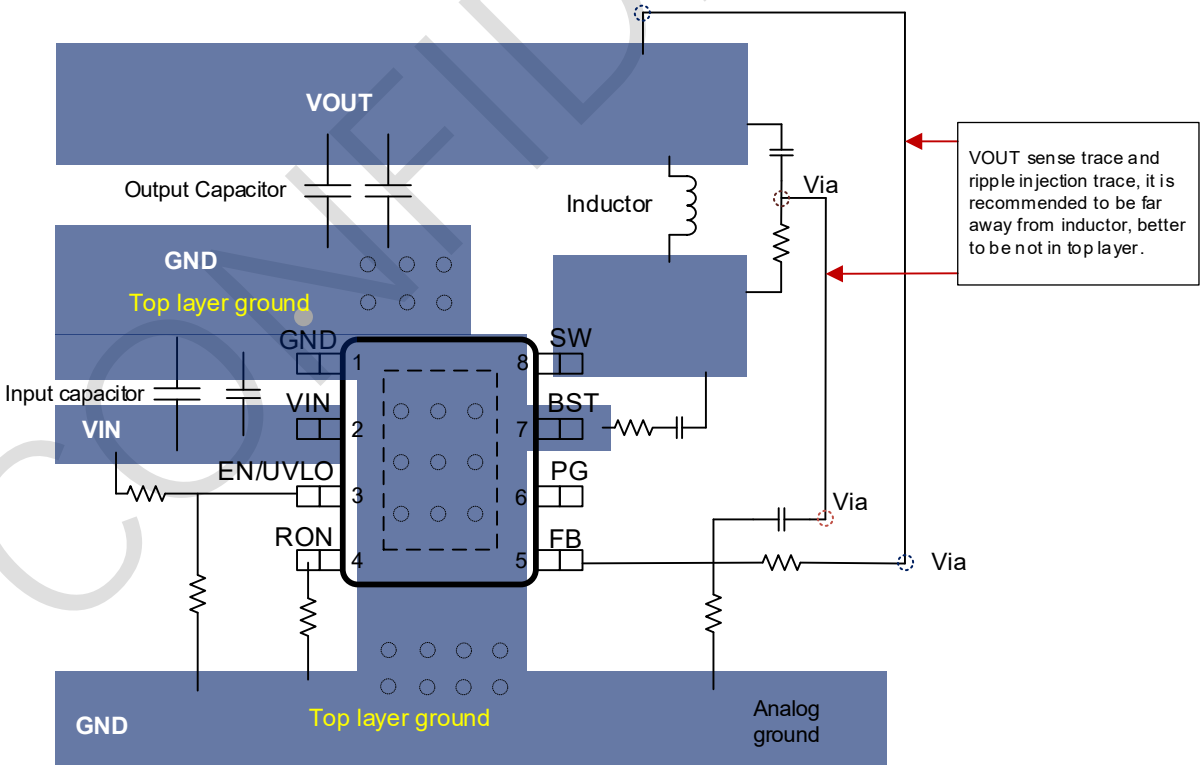


Figure 10-25, Load Transient in Secondary Side I_{OUT1}=0A , I_{OUT2}=0.1A-0.2A

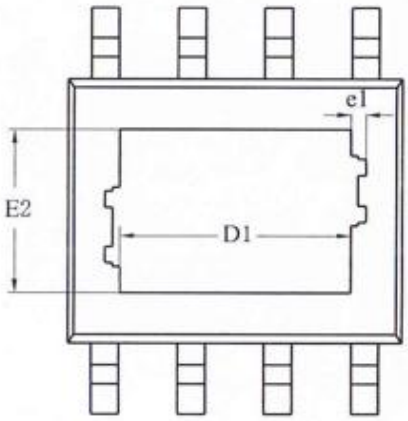
11 Layout Guideline

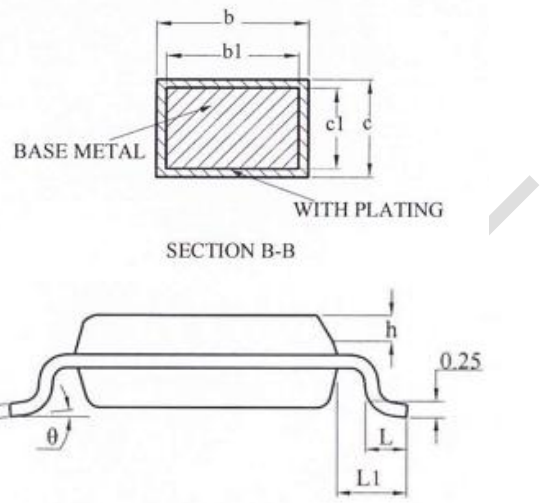
Layout is critical for proper operation. Please follow the layout guidelines.

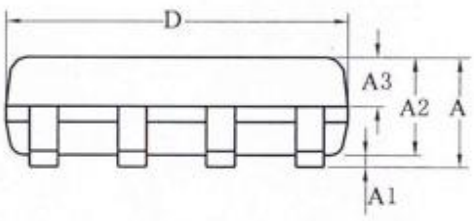
1. The power ground is very critical. The power trace should take as lowest impedance as possible and the ground area should be sufficient to optimize thermal.
2. The GND Pin should be connected directly to the thermal pad beside the IC, the 8mil Max thermal via is recommended.
3. Place the bypass input capacitor with low ESR as close as possible to the VIN pin and GND. The bypassing loop from VIN terminal to GND should be as short as possible.
4. The inductor should be located as close as possible to the SW pin to reduce magnetic and electrostatic noise.
5. The feedback resistor divider should be placed close to the FB pin. The VOUT sense trace should be far away from the inductor or in different PCB layer.
6. The ripple injection Rr, Cr is recommended to be close to the inductor, the Cb is recommended to be close to the FB pin, and the sense trace should be far away from the inductor or in different layer.
7. The ground connected to the input capacitors and output capacitors should be tied to the system ground plane in only one spot to minimize conducted noise to the system ground plane.

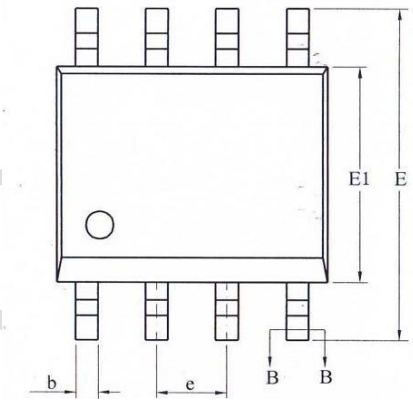


PACKAGE INFORMATION (eSOP-8L)









Symbol	Millimeter		
	Min	Nor	Max
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0	-	8°

	D1	E2	e1
95*130	3.10REF	2.21REF	0.10REF