1.8-V, Nano-Power Comparator with Voltage Reference

Features

- Ultra-Low Supply Current: 390-nA Comparator with Reference
- Internal 1.3-V Reference @ V_{DD} = 5 V
- Fast Response Time: 13-μs Propagation Delay, with 100-mV Overdrive
- Internal Hysteresis for Clean Switching
- Input Bias Current: 6 pA Typical
- Push-Pull Output with ±25-mA Drive Capability
- No Phase Reversal for Overdriven Inputs
- Low Supply Voltage: 1.8 V to 5.5 V
- Green, Space-Saving SOT23 Package

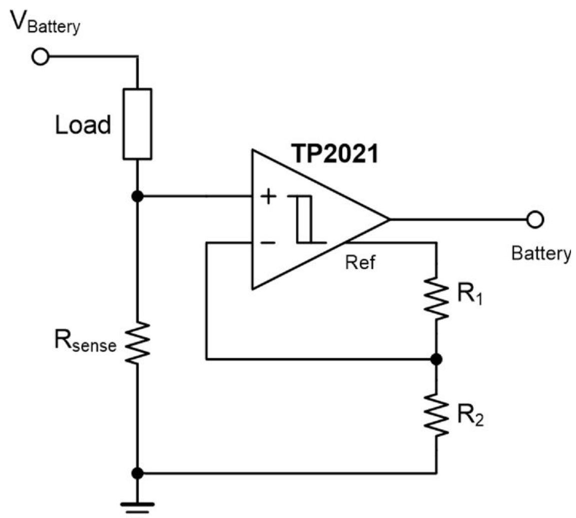
Applications

- Battery Monitoring/Management
- Alarm and Monitoring Circuits
- Threshold Detectors/Discriminators
- Sensing at Ground or Supply Line
- Ultra-Low-Power Systems

Description

The device has a push-pull output stage with loads up to 25 mA. The device features an on-chip 1.3-V reference and draws an ultra-low supply current of only 390 nA. The device incorporates 3PEAK's proprietary and patented design techniques to achieve the best world-class performance among all nano-power comparators. The internal input hysteresis eliminates the output switching due to the internal input noise voltage, reducing the current draw. These features make the device ideal for low-power applications.

Typical Application Circuit



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Revision History

Date	Revision	Notes
2022-04-29	Rev.1.6	Updated Order Information.
2024-01-25	Rev.1.7	Added the part number: TP2021A-TR. Updated the EC table: 1) Adjusted the condition of the EC table: from "V_{DD} = +1.8 V to +5.5 V, V_{IN+} = V_{DD}, V_{IN-} = 1.2 V, R_{PU} = 10 kΩ, C_L = 15 pF." to "V_{DD} = 5.5 V, C_L = 15 pF."; 2) Added the specification of V_{OS} at V_{DD} = 1.8 V; 3) Added the condition of PSRR; 4) Adjusted MIN/TYP/MAX of V_{OUT} (Reference Voltage) at V_{DD} = 5 V: MIN: from 1.225 to 1.14; TYP: from 1.248 to 1.3; MAX: from 1.285 to 1.46; 5) Adjusted MIN/TYP/MAX of V_{OUT} (Reference Voltage) at V_{DD} = 3 V: MIN: from 1.20 to 1.13; TYP: from 1.23 to 1.29; MAX: from 1.26 to 1.45. The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged. Updated the figures and application information. Removed the description about TP2025 and other part numbers that were not in production. Updated to a new format of Package Outline Dimensions. Added Tape and Reel Information.
2024-11-03	Rev.A.0	Updated to a new datasheet format. The following updates in Electrical Characteristics are about typos, the physical object remains unchanged. • V_{OS}: from V_{DD} = 5.5 V, V_{CM} = 1.2 V to V_{DD} = 1.8 V, V_{CM} = 0 V • PSRR: from V_{DD} = 1.8 V to 5.5 V, V_{CM} = 1.2 V, min 60, typ 90 to V_{DD} = 1.8 V to 5.5 V, V_{CM} = 0 V, min 50, typ 70

Pin Configuration and Functions

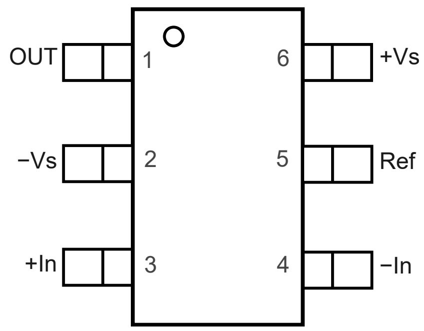


Table 1. Pin Functions: TP2021

Pin No.	Name	I/O	Description
1	Out	O	Output
2	$-V_S$	-	Negative power supply
3	+In	I	Noninverting input
4	−In	I	Inverting input
5	Ref		Reference voltage output
6	$+V_S$	-	Positive power supply

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	Supply Voltage, $(+V_S) - (-V_S)$		6.0	V
	Input Voltage	$(-V_S) - 0.3$	$(+V_S) + 0.3$	V
	Input Current: +IN, −IN (2)	−10	+10	mA
	Output Current: OUT	−25	+25	mA
	Output Short-Circuit Duration (3)		Indefinite	
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many comparators are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

All test conditions: T_A = 27°C, V_{DD} = (+V_S) − (−V_S) = 5.5 V, C_L = 15 pF, unless otherwise noted.

The ● denotes the specifications that apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage, (+V_S) − (−V_S)		●	1.8		5.5	V
V_{OS}	Input Offset Voltage (1)	V_{CM} = 1.2 V		−12.0	0.5	+12.0	mV
		V_{DD} = 1.8 V, V_{CM} = 0 V		−12.0	0.5	+12.0	mV
V_{OS}TC	Input Offset Voltage Drift (1)	V_{CM} = 1.2 V			0.3		µV/°C
V_{HYST}	Input Hysteresis Voltage (1)	V_{CM} = 1.2 V			4		mV
V_{HYST}TC	Input Hysteresis Voltage Drift (1)	V_{CM} = 1.2 V			20		µV/°C
I_B	Input Bias Current	V_{CM} = 1.2 V			6		pA
I_{OS}	Input Offset Current	V_{CM} = 1.2 V			4		pA
R_{IN}	Input Resistance				> 100		GΩ
C_{IN}	Input Capacitance	Differential Mode			2		pF
		Common Mode			4		pF
CMRR	Common-Mode Rejection Ratio	TP2021, V_{CM} = 0 V to (+V_S) − 1.2 V			82		dB
		TP2021A, V_{CM} = 0 V to (+V_S)			82		dB
V_{CM}	Common-Mode Input Voltage Range	TP2021		(−V_S)		(+V_S) − 1.2	V
		TP2021A		(−V_S)		(+V_S)	V
PSRR	Power Supply Rejection Ratio	V_{DD} = 1.8 V to 5.5 V, V_{CM} = 0 V		50	70		dB
V_{OH}	High-Level Output Voltage	I_{OUT} = −1 mA	●	(+V_S) − 0.3			V
V_{OL}	Low-Level Output Voltage	I_{OUT} = 1 mA	●			0.3	V
I_{SC}	Output Short-Circuit Current	Sink or Source Current			25		mA
I_Q	Quiescent Current per Comparator				390	550	nA
V_{OUT}	Reference Voltage	V_{DD} = 5 V		1.14	1.3	1.46	V
		V_{DD} = 3 V		1.13	1.29	1.45	V
V_{OUT} TC	Reference Voltage Drift				150		µV/°C
V_{OUT} LC		0 µA ≤ I_{source} ≤ 400 µA			1.45		µV/µA
		0 µA ≤ I_{sink} ≤ 400 µA			0.13		µV/µA
t_R	Rising Time				5		ns
t_F	Falling Time				5		ns
T_{PD+}	Propagation Delay (Low-to-High)	Overdrive = 100 mV, V_{IN-} = 1.2 V			13		µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{PD-}	Propagation Delay (High-to-Low)	Overdrive = 100 mV, V_{IN-} = 1.2 V			14		μs
T_{PDSKEW}	Propagation Delay Skew (2)	Overdrive = 100 mV, V_{IN-} = 1.2 V			3		μs

(1) The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.
(2) The propagation delay skew is defined as: $t_{PD\text{-}SKEW} = t_{PD+} - t_{PD-}$.

Typical Performance Characteristics

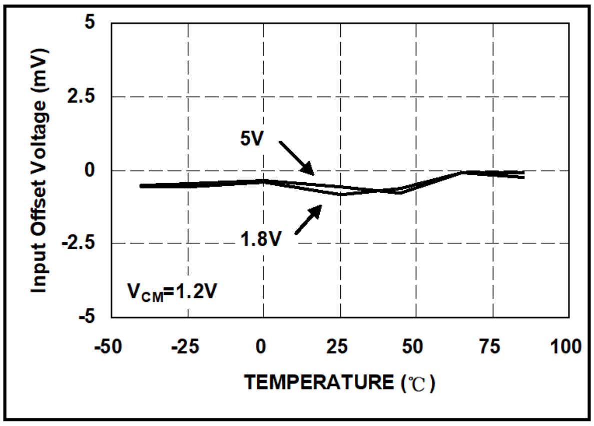


Figure 1. Input Offset Voltage vs. Temperature

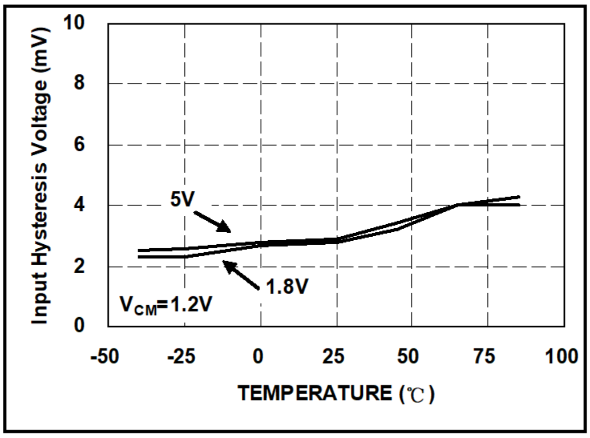


Figure 2. Input Hysteresis Voltage vs. Temperature

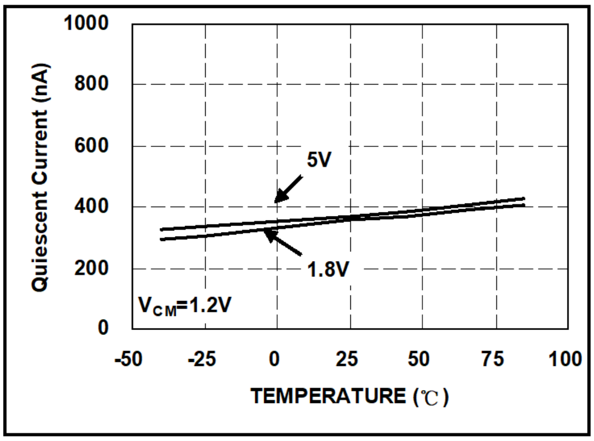


Figure 3. Quiescent Current vs. Temperature

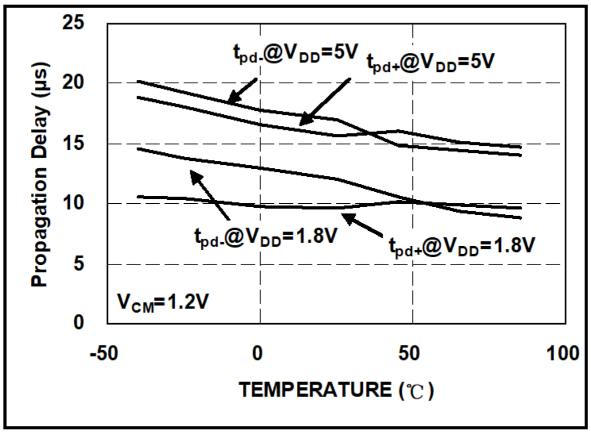


Figure 4. Propagation Delay vs. Temperature

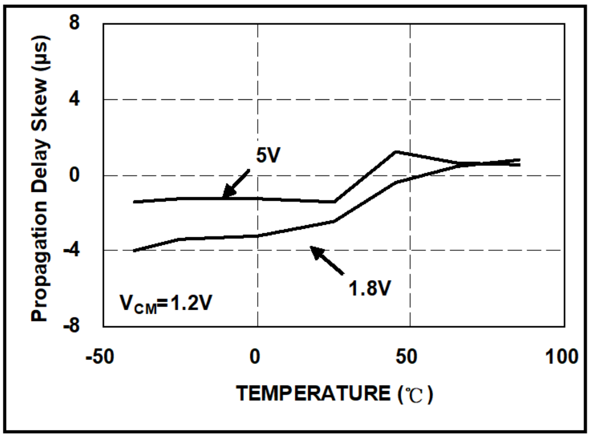


Figure 5. Propagation Delay Skew vs. Temperature

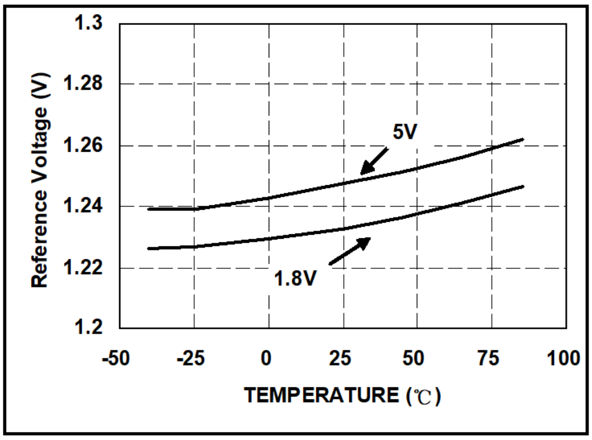


Figure 6. Reference Voltage vs. Temperature

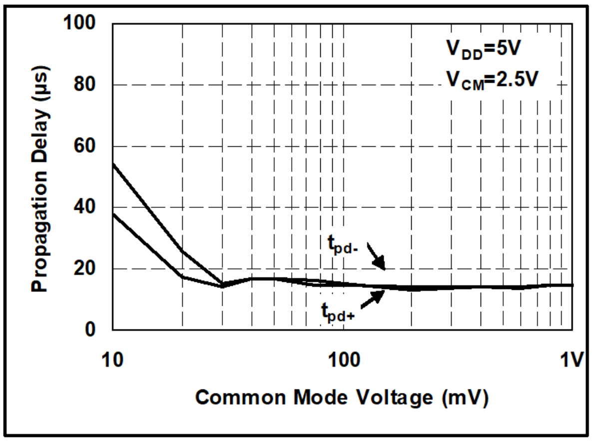


Figure 7. Propagation Delay vs. Overdrive Voltage

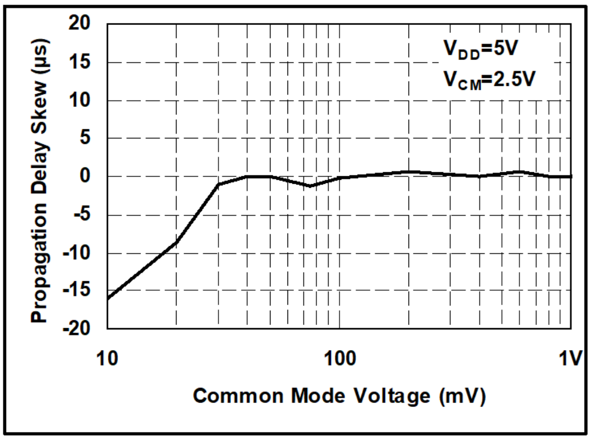


Figure 8. Propagation Delay Skew vs. Overdrive Voltage

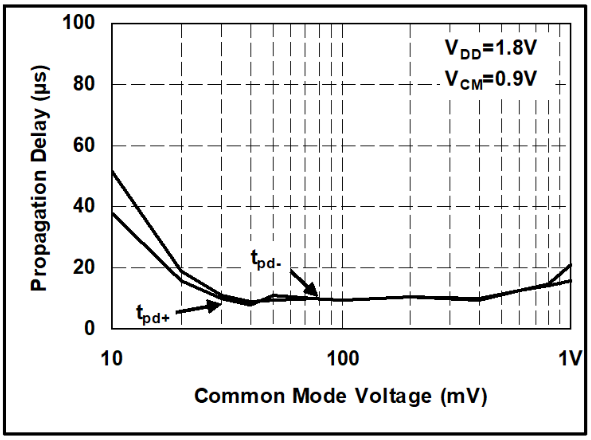


Figure 9. Propagation Delay vs. Overdrive Voltage

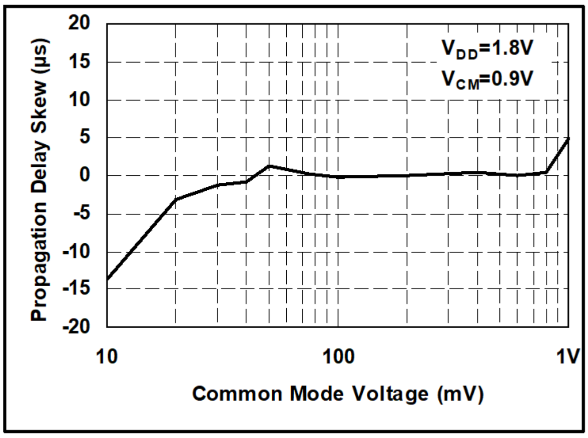


Figure 10. Propagation Delay Skew vs. Overdrive Voltage

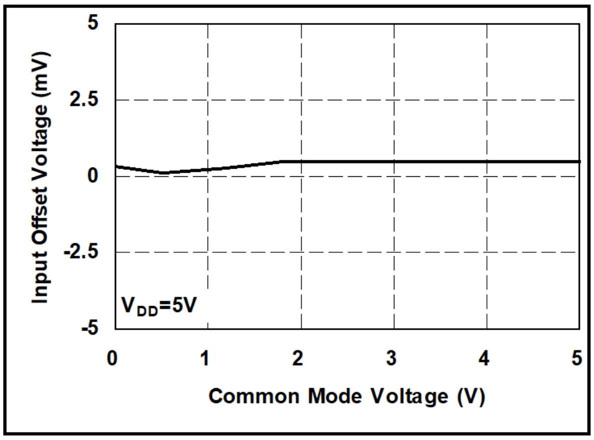


Figure 11. Input Offset Voltage vs. Common-Mode Voltage

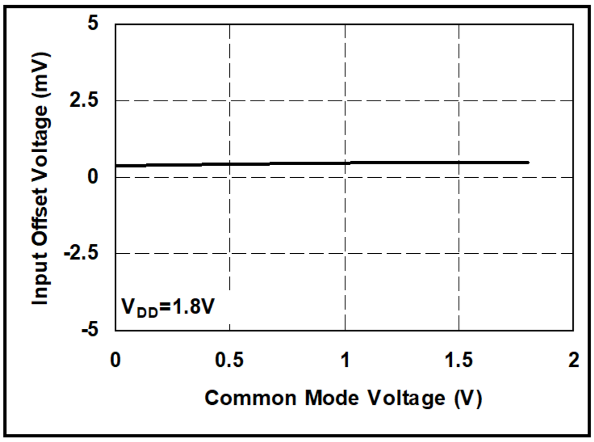


Figure 12. Input Offset Voltage vs. Common-Mode Voltage

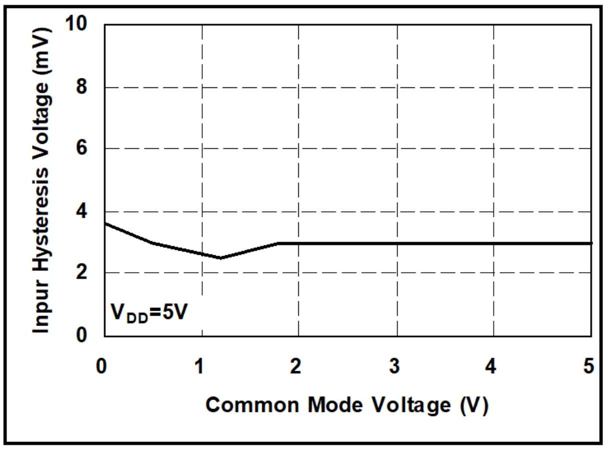


Figure 13. Input Hysteresis Voltage vs. Common-Mode Voltage

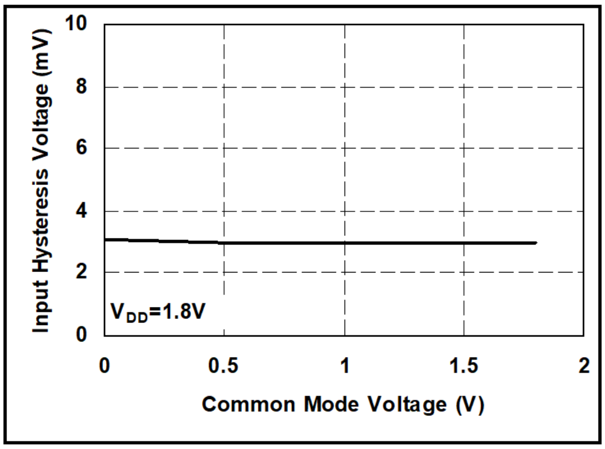


Figure 14. Input Hysteresis Voltage vs. Common-Mode Voltage

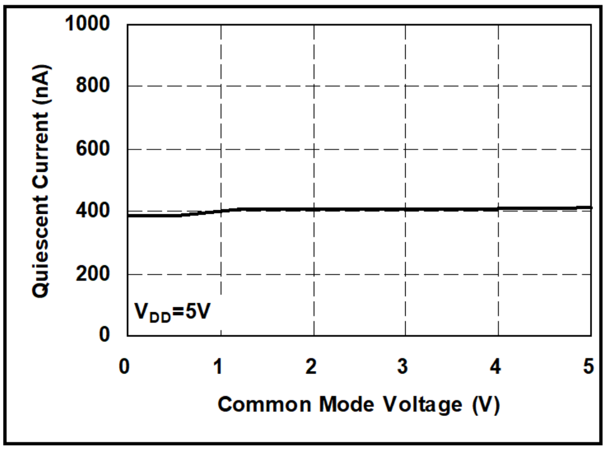


Figure 15. Quiescent Current vs. Common-Mode Voltage

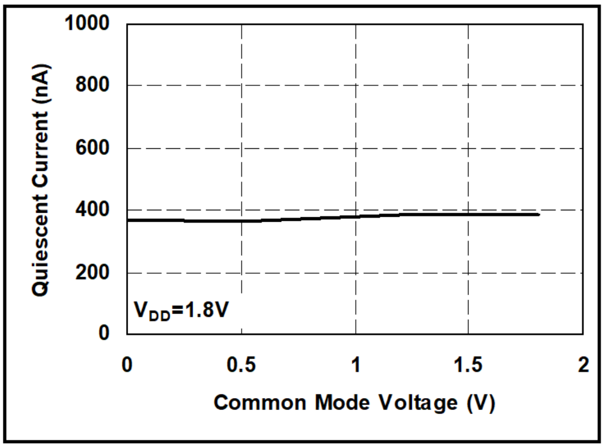


Figure 16. Quiescent Current vs. Common-Mode Voltage

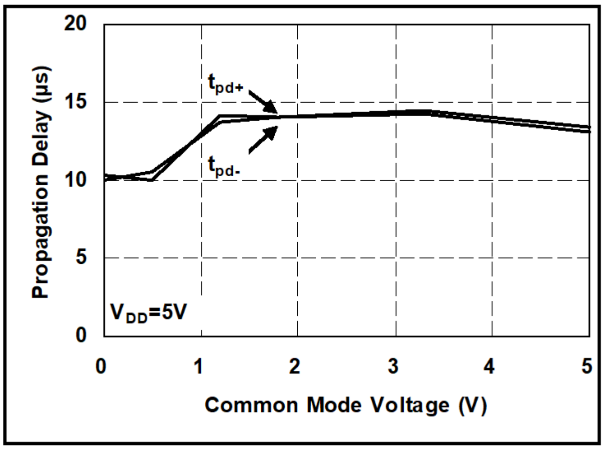


Figure 17. Propagation Delay vs. Common-Mode Voltage

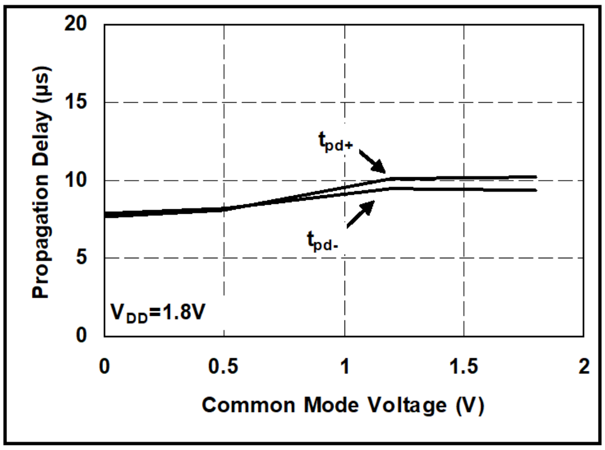


Figure 18. Propagation Delay vs. Common-Mode Voltage

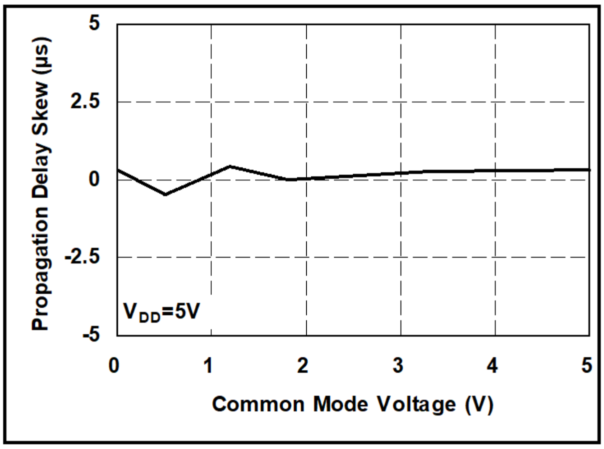


Figure 19. Propagation Delay Skew vs. Common-Mode Voltage

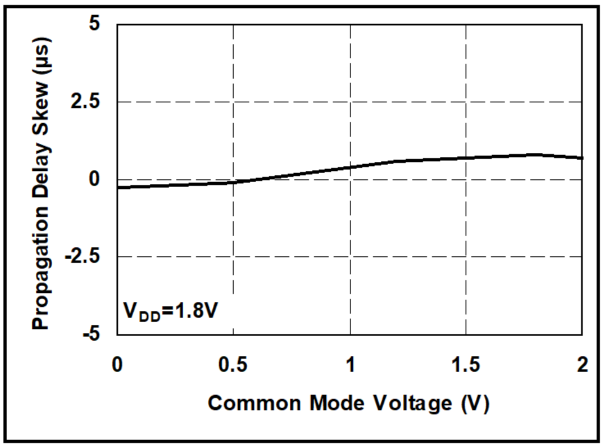


Figure 20. Propagation Delay Skew vs. Common-Mode Voltage

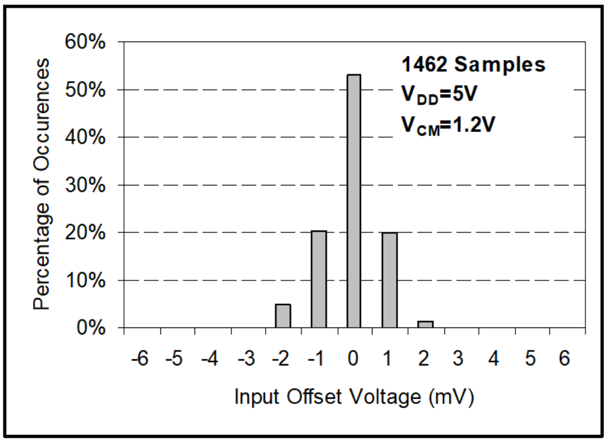


Figure 21. Input Offset Voltage Distribution

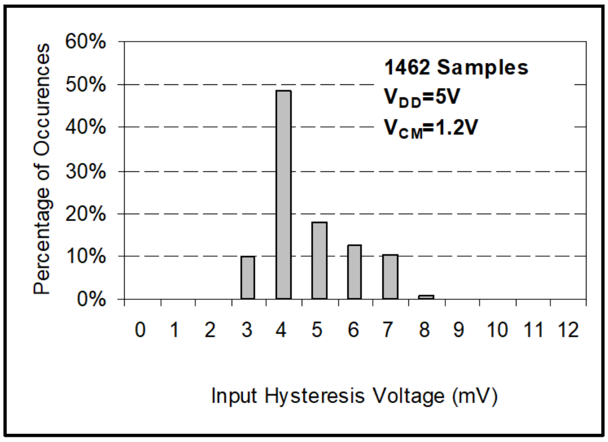


Figure 22. Input Hysteresis Voltage Distribution

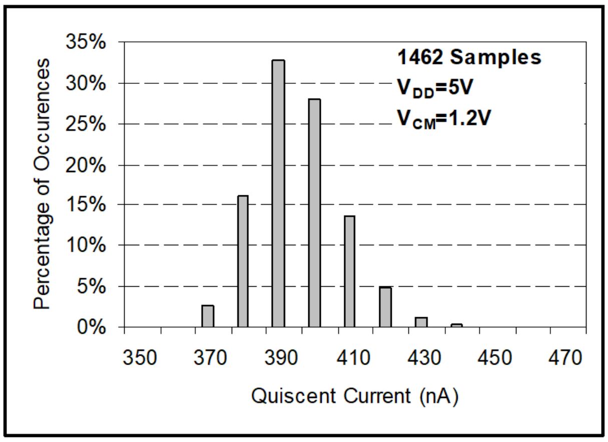


Figure 23. Quiescent Current Distribution

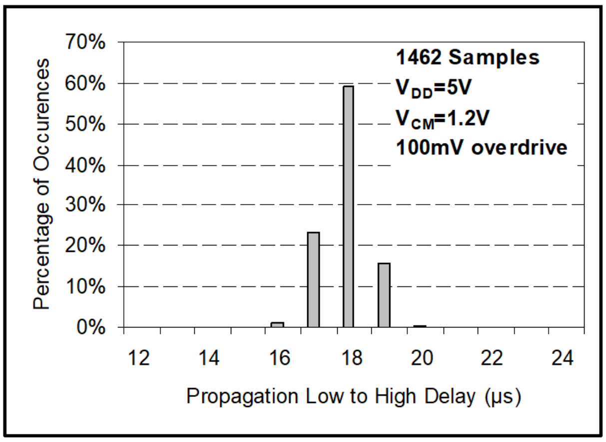


Figure 24. Low to High Propagation Delay Distribution

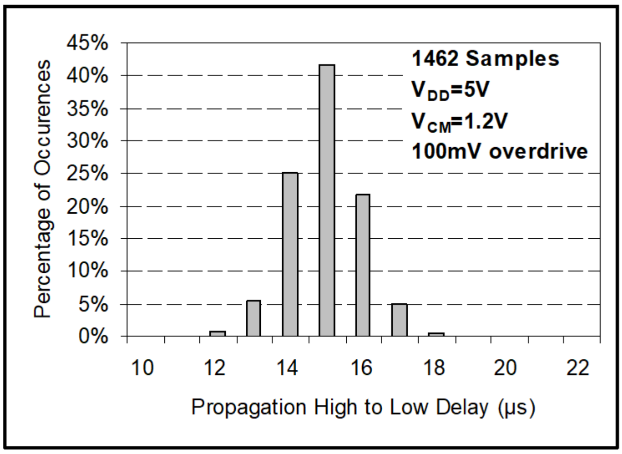


Figure 25. High-to-Low Propagation Delay Distribution

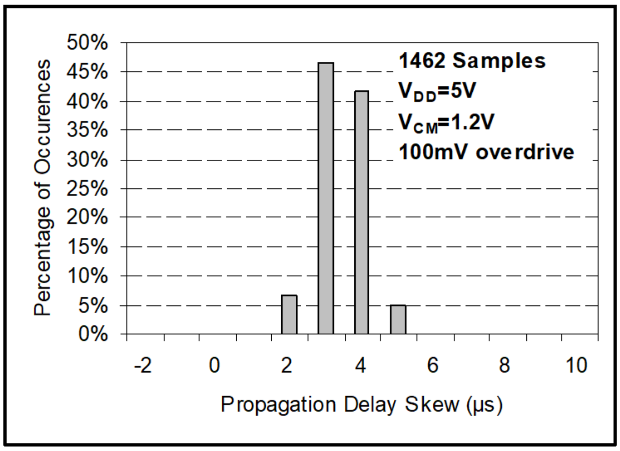


Figure 26. Propagation Delay Skew Distribution

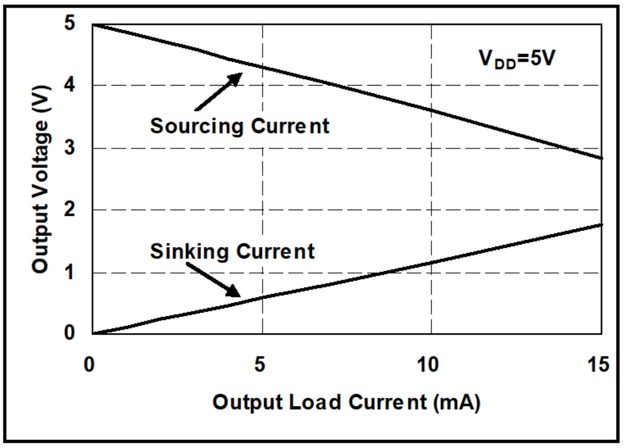


Figure 27. Output Voltage Headroom vs. Output Load Current

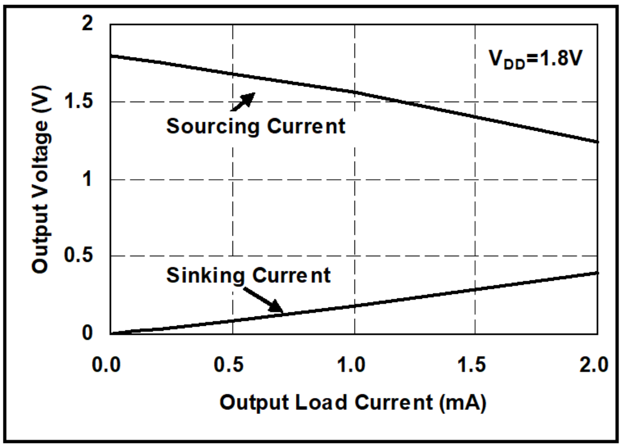


Figure 28. Output Voltage Headroom vs. Output Load Current

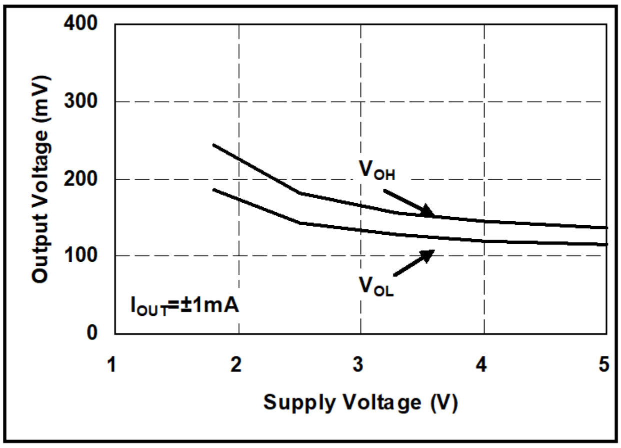


Figure 29. Output Voltage Headroom vs. Supply Voltage

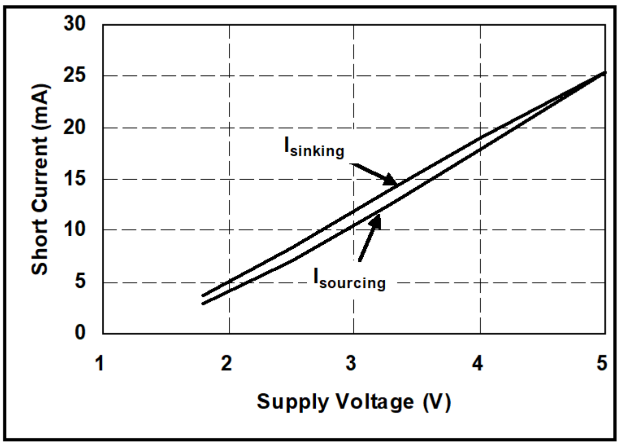


Figure 30. Output Short Current vs. Supply Voltage

Detailed Description

Overview

The TP202x is a series of single-supply comparators featuring internal hysteresis, internal reference, high speed, and ultra-low power. The input signal range extends beyond the negative and positive power supplies. The output can even extend all the way to the negative supply.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of the noise or undesired parasitic feedback. This tends to occur when the voltage on one input is equal to the voltage on the other input. To counter the parasitic effects and noise, the TP2021 series implements internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and the other for the falling input voltage. The difference between the trip points is the hysteresis. When the input voltages of the comparators are equal, the hysteresis effectively causes one input voltage of the comparator to move quickly past the other, thus taking the input out of the region where the oscillation occurs. Figure 31 illustrates the case where IN− is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the outputs would be inverted.

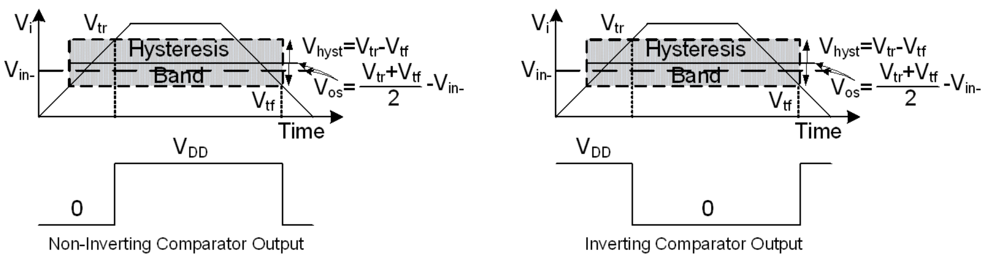


Figure 31. Comparator's Hysteresis and Offset

Low Input Bias Current

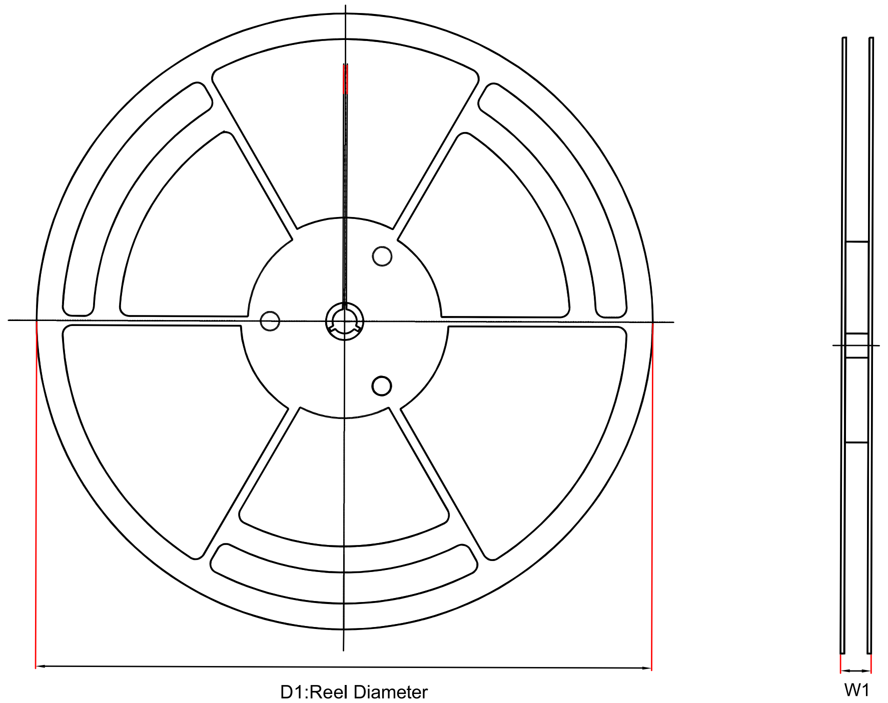
The TP2021 series is a CMOS comparator series and features a very low input bias current in the pA range. The low input bias current allows the comparators to be used in applications with high resistance sources. Care must be taken to minimize the PCB surface leakage.

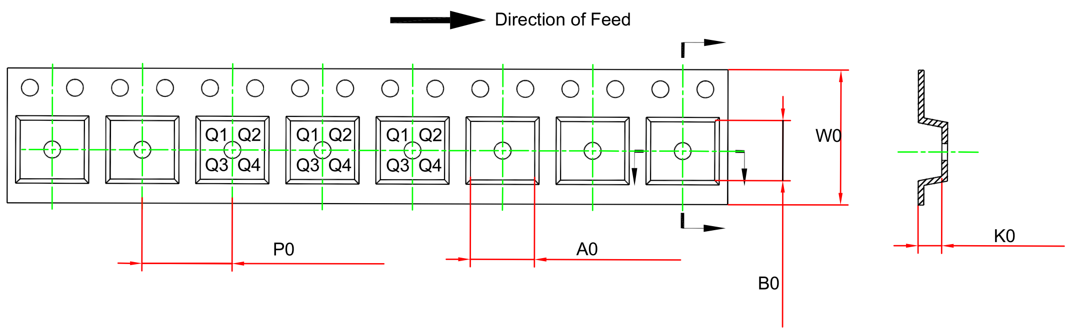
Power Supply Layout and Bypass

The power supply pin of the TP2021 series should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for good high-frequency performance. It can also use a bulk capacitor (i.e., 1 μF or larger) within 100 mm to provide large and slow currents. This bulk capacitor can be shared with other analog parts.

The good ground layout improves performance by decreasing the amount of stray capacitance and noise at the inputs and outputs of the comparator. To decrease the stray capacitance, minimize the PCB lengths and resistor leads, and place external components as close to the pins as possible.

Tape and Reel Information



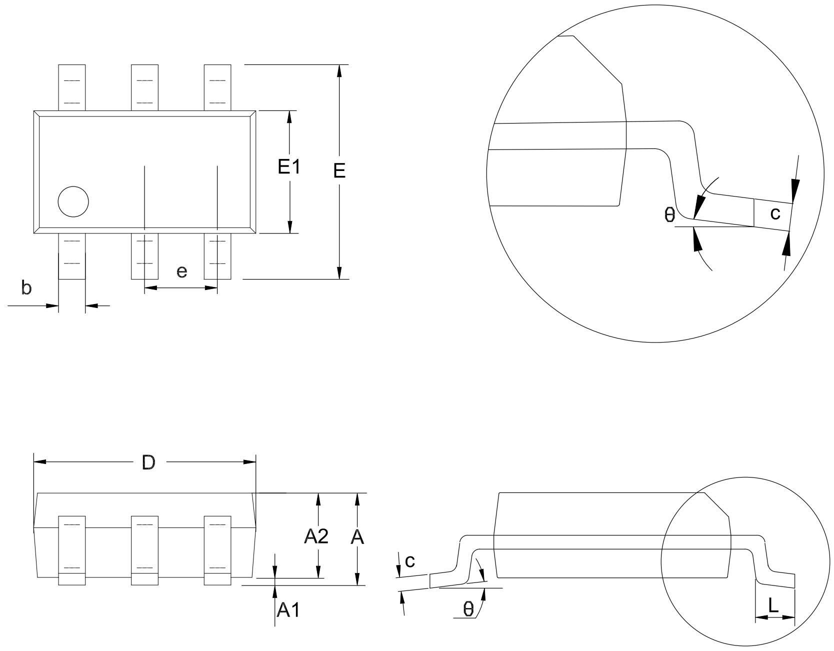


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP2021-TR	SOT23-6	180.0	12.0	3.3	3.2	1.4	4.0	8.0	Q3
TP2021A-TR	SOT23-6	180.0	12.0	3.3	3.2	1.4	4.0	8.0	Q3

Package Outline Dimensions

SOT23-6

Package Outline Dimensions S6T(SOT23-6-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TP2021-TR	0°C to 70°C	SOT23-6	C2T	MSL 3	Tape and Reel, 3000	Green
TP2021A-TR	–40°C to 125°C	SOT23-6	C2T	MSL 3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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