7-ns, 1/2/4, Ultra-High-Speed, +3-V/+5-V, Beyond-the-Rails Comparator

Features

- Ultra-Fast, 7-ns Propagation Delay
- Ideal for +3-V and +5-V Single-Supply Applications
- Offset Voltage: ±10.0 mV Maximum
- Rail-to-Rail Input and Output
- 7.5-mV Internal Hysteresis for Clean Switching
- Push-Pull, CMOS/TTL Compatible Output
- Input Common-Mode Range Extends 300 mV
- No Phase Reversal for Overdriven Inputs
- Shut-down Function (TP1961N Only)
- Supply Voltage: 2.5 V to 5.5 V
- Green, Space-Saving SOT23-5 Package Available

Applications

- High-Speed Line or Digital Line Receivers
- High-Speed Sampling Circuits
- Peak and Zero-crossing Detectors
- Threshold Detectors/Discriminators
- Sensing at Ground or Supply Line
- Logic Level Shifting or Translation
- Window Comparators
- IR Receivers
- Clock and Data Signal Restoration
- Telecom, Portable Communications

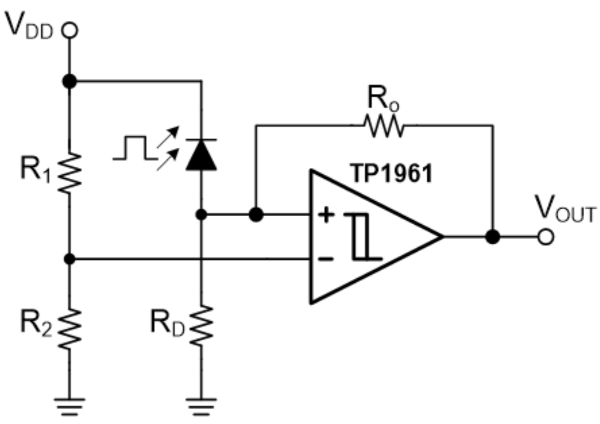
Description

The TP1961/TP1962/TP1964 is a series of low-power, ultra-high-speed comparators with internal hysteresis. The TP1961/962/964 series is optimized for single +3-V or +5-V operation. The input common-mode range extends 300 mV beyond the rail, and the outputs can sink or source 4 mA to within 80 mV of GND and V_{CC}. The propagation delay is 7 ns (50 mV overdrive), while the supply current is 1 mA per comparator.

The internal input hysteresis eliminates the output switching due to the internal input noise voltage, reducing the current draw. The push-pull output supports rail-to-rail output swing, and interfaces with the CMOS/TTL logic. The output toggle frequency can reach 50 MHz (typical) while limiting supply current surges and the dynamic power consumption during switching.

The TP1961 single comparator is available in the shut-down function, and the tiny SOT23 package for space-conservative design. The TP1961/962/964 series is specified for the temperature range from −40°C to +125°C.

Typical Application Circuit



The TP1961 Comparator in IR Receivers

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Revision History

Date	Revision	Notes
2020-03-20	Rev.B.5	Updated Thermal Information
2022-04-29	Rev.B.6	Updated Order Information
2025-11-27	Rev.B.7	The following updates are all about the new datasheet formats or typos, and the actual product remains unchanged • Updated to a new datasheet format • Updated the POD format • Added the thermal pad description in the Pin Configuration and Functions

Pin Configuration and Functions

TP1961
SOT23-5/SOT353 (SC70-5)
Top View

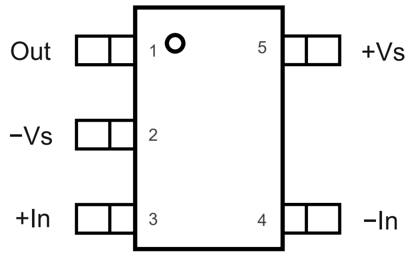
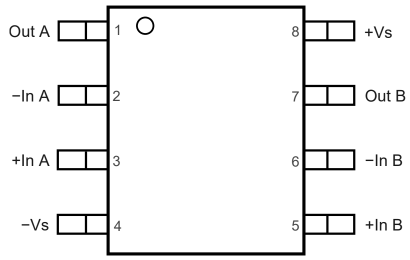


Table 1. Pin Functions: TP1961

Pin No.	Name	I/O	Description
1	Out	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
2	$-V_S$	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between V+ and V– is from 2.5 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 μF as close to the part as possible.
3	+In	I	Non-inverting input of comparator. This pin has the same voltage range as –IN.
4	−In	I	Inverting input of the comparator. The voltage of this pin ranges from (V–) – 0.3 V to (V+) + 0.3 V.
5	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 2.5 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 2.5 V and 5.5 V. A bypass capacitor of 0.1 μF as close to the part as possible should be used between the power supply pins or between supply pins and GND.

TP1962
SOP8/MSOP8
Top View



TP1962
DFN2×2-8
Top View

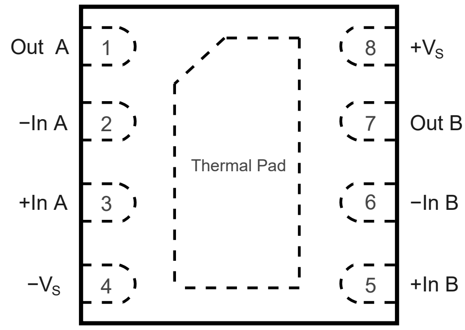


Table 2. Pin Functions: TP1962

Pin No.		Name	I/O	Description
SOP8/ MSOP8	DFN2×2-8			
1	1	Out A	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
2	2	−In A	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
3	3	+In A	I	Non-inverting input of comparator. This pin has the same voltage range as –IN.
4	4	$-V_S$	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between V+ and V– is from 2.5 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 μF as close to the part as possible.
5	5	+In B	I	Non-inverting input of comparator. This pin has the same voltage range as –IN.
6	6	−In B	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
7	7	Out B	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
8	8	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 2.5 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 2.5 V and 5.5 V. A bypass capacitor of 0.1 μF as close to the part as possible should be used between the power supply pins or between supply pins and GND.
		Thermal Pad		The thermal pad of the DFN2X2-8 is recommended to be left float or connected to $-V_S$.

TP1964
SOP14/TSSOP14
Top View

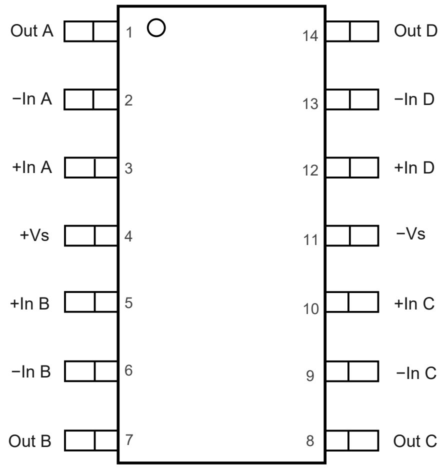


Table 3. Pin Functions: TP1964

Pin No.	Name	I/O	Description
1	Out A	Power Supply	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
2	−In A	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
3	+In A	I	Non-inverting input of comparator. This pin has the same voltage range as –IN.
4	$+V_S$	Power Supply	Positive power supply. Typically, the voltage is from 2.5 V to 5.5 V. Split supplies are possible as long as the voltage between V+ and V– is between 2.5 V and 5.5 V. A bypass capacitor of 0.1 μF as close to the part as possible should be used between the power supply pins or between supply pins and GND.
5	+In B	I	Non-inverting input of comparator. This pin has the same voltage range as –IN.
6	−In B	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
7	Out B	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
8	Out C	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.
9	−In C	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
10	+In C	I	Non-inverting input of comparator. This pin has the same voltage range as –IN.
11	$-V_S$	Power Supply	Negative power supply. It is normally tied to GND. It can also be tied to a voltage other than GND when the voltage between V+ and V– is from 2.5 V to 5.5 V. If it is not connected to GND, bypass it with a capacitor of 0.1 μF as close to the part as possible.
12	+In D	I	Non-inverting input of comparator. This pin has the same voltage range as –IN.

Pin No.	Name	I/O	Description
13	−In D	I	Inverting input of the comparator. The voltage range of this pin can go from (V–) – 0.3 V to (V+) + 0.3V.
14	Out D	O	The output of the comparator. The voltage range extends to within millivolts of each supply rail.

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	Supply Voltage, (V+) − (V−)		7.0	V
	Input Voltage	(V−) − 0.3	(V+) + 0.3	V
	Input Current: +IN, −IN (2)	−20	20	mA
	Output Current: OUT	−160	160	mA
	Output Short-Circuit Duration (3)		Infinite	
T_J	Maximum Junction Temperature		150	°C
T_A	Operating Temperature Range	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many comparators are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-5	89.1	52.0	℃/W

Electrical Characteristics

All test conditions: T_A = 27°C, V_{DD} = +2.5 V to +5.5 V, V_{IN+} = V_{DD}, V_{IN-} = 1.2 V, R_{PU} = 10 kΩ, C_L = 15 pF, unless otherwise noted.

The ● denotes the specifications which apply over the full operating temperature range.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage		●	2.5		5.5	V
V_{OS}	Input Offset Voltage (1)	V_{CM} = 1.2 V		−10	±2	+10	mV
$V_{OS}TC$	Input Offset Voltage Drift (1)	V_{CM} = 1.2 V			0.3		μV/°C
V_{HYST}	Input Hysteresis Voltage (1)	V_{CM} = 1.2 V			7.5		mV
I_B	Input Bias Current	V_{CM} = 1.2 V			6		pA
I_{OS}	Input Offset Current				4		pA
R_{IN}	Input Resistance				> 100		GΩ
C_{IN}	Input Capacitance	Differential mode			2.7		pF
		Common mode			1		pF
CMRR	Common-Mode Rejection Ratio	V_{CM} = V_{SS} to V_{DD}			110		dB
V_{CM}	Common-Mode Input Voltage Range			V_{SS} − 0.1		V_{DD} + 0.1	V
PSRR	Power Supply Rejection Ratio				110		dB
V_{OH}	High-Level Output Voltage	I_{OUT} = 4 mA, V_{ID} = 500 mV	●	V_{DD} − 0.35	V_{DD} − 0.2		V
		I_{OUT} = 0.4 mA, V_{ID} = 500 mV		V_{DD} − 0.15	V_{DD} − 0.05		V
V_{OL}	Low-Level Output Voltage	I_{OUT} = −4 mA, V_{ID} = 500 mV	●		80	250	mV
		I_{OUT} = −0.4 mA, V_{ID} = 500 mV			10	100	mV
I_{SC}	Output Short-Circuit Current	Sink or source current			100		mA
I_Q	Quiescent Current per Comparator				2.4		mA
t_R	Rising Time				1		ns
t_F	Falling Time				1		ns
T_{PD+}	Propagation Delay (Low-to-High) (2)	Overdrive = 100 mV, V_{IN-} = 1.2 V			7	19	ns
T_{PD-}	Propagation Delay (High-to-Low) (2)	Overdrive = 100 mV, V_{IN-} = 1.2 V			7	19	ns
T_{PDSKEW}	Propagation Delay Skew	Overdrive = 100 mV, V_{IN-} = 1.2 V			0.4		ns

(1) The input offset voltage is the average of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.
(2) The propagation delay skew is defined as: $t_{PD-SKEW} = t_{PD+} - t_{PD-}$.

Typical Performance Characteristics

All test conditions: T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2, C_L = 10 pF, unless otherwise noted.

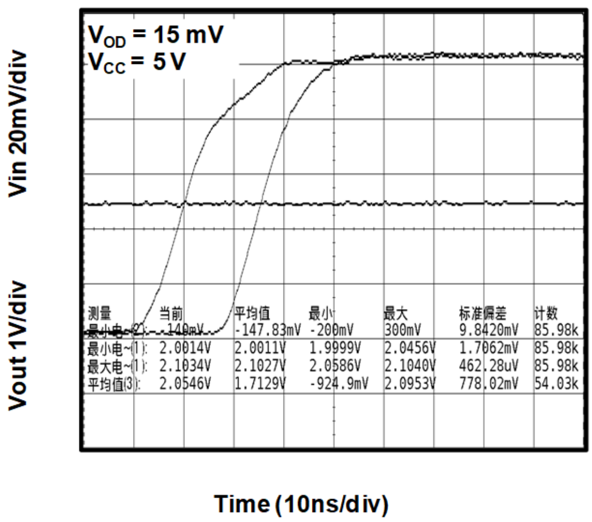


Figure 1. Propagation Delay (t_{PD+})

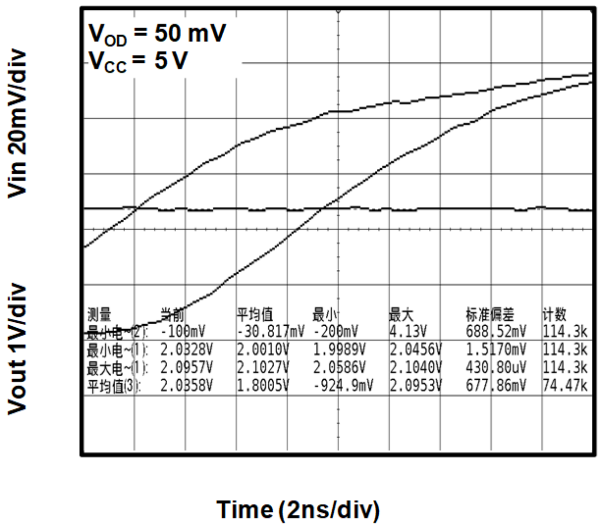


Figure 2. Propagation Delay (t_{PD+})

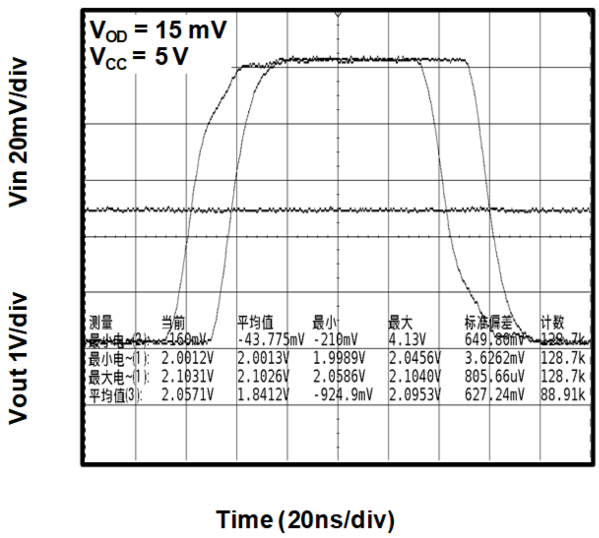


Figure 3. Propagation Delay (t_{PD})

Detailed Description

Overview

The TP1961/TP1962/TP1964 is a series of single-supply comparators featuring internal hysteresis, ultra-high-speed operation, and low power consumption. The outputs are guaranteed to pull within 0.52 V of either rail without the external pull-up or pull-down circuitry. Beyond-the-rails input voltage range and the low-voltage, single-supply operation make the series ideal for portable equipment. These comparators all interface directly to the CMOS logic.

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Inputs

The TP196x series uses CMOS transistors at the input which prevents the phase inversion when the input pins exceed the supply voltages. Figure 4 shows an input voltage exceeding both supplies with no resulting phase inversion.

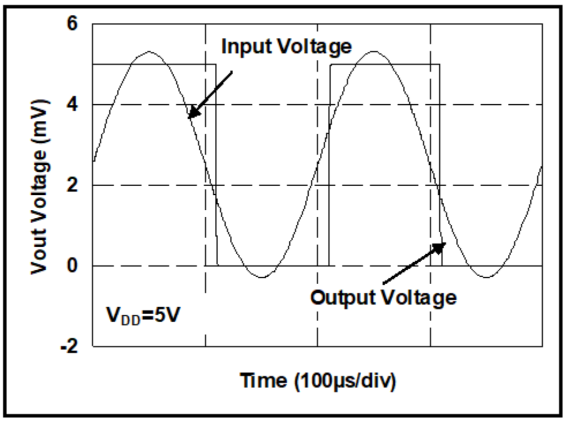


Figure 4. Comparator Response to Input Voltage

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1-kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed supply voltages, as shown in Figure 5. Large differential voltages exceeding the supply voltage should be avoided to prevent damage to the input stage.

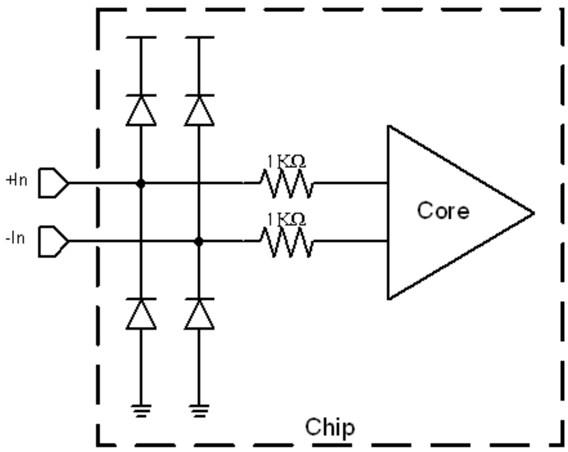


Figure 5. Equivalent Input Structure

Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of the noise or undesired parasitic feedback. This tends to occur when the voltage on one input is equal to the voltage on the other input. To counter the parasitic effects and noise, the TP196x series implements the internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and the other for the falling input voltage. The difference between the trip points is the hysteresis. When the input voltages of the comparators are equal, the hysteresis effectively causes one input voltage of the comparator to move quickly past the other, and thus taking the input out of the region where the oscillation occurs. Figure 6 illustrates the case where IN− is fixed and IN+ is varied. If the inputs are reversed, the figure looks the same, except the outputs are inverted.

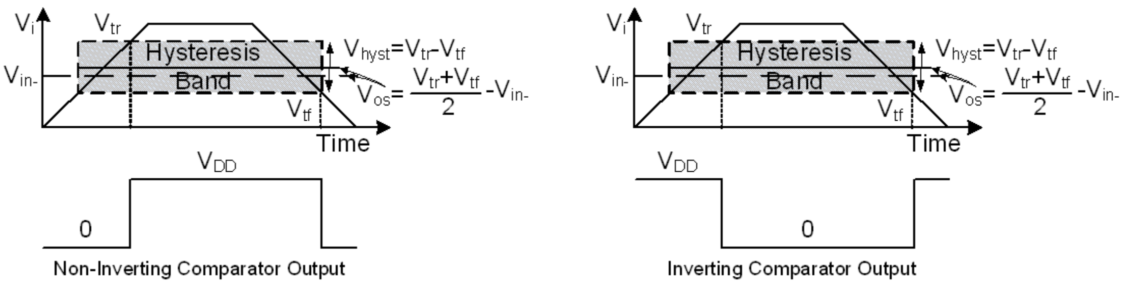


Figure 6. Comparator's Hysteresis and Offset

External Hysteresis

Greater flexibility in selecting hysteresis is achieved by using external resistors. The hysteresis reduces the output chattering when one input is slowly moving past the other. It is beneficial for systems where it is best not to cycle between high and low states too frequently (e.g., air conditioner thermostatic control). The output chattering also increases the dynamic supply current.

Non-Inverting Comparator with Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 7 and a voltage reference (V_r) at the inverting input.

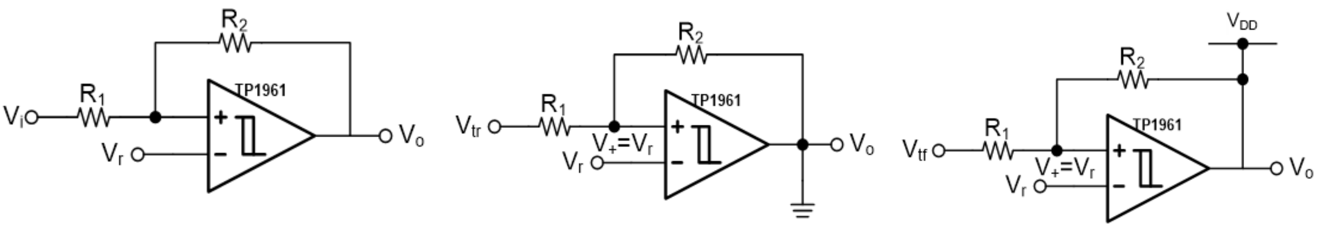


Figure 7. Non-Inverting Configuration with Hysteresis

When V_i is low, the output is also low. For the output to switch from low to high, V_i must rise up to V_{tr}. When V_i is high, the output is also high. In order for the comparator to switch back to a low state, V_i must equal V_{tf} before the non-inverting input V_+ is again equal to V_r.

$$V_r = \frac{R_2}{R_1 + R_2} V_{tr} \tag{1}$$

$$V_r = (V_{DD} - V_{tf}) \frac{R_1}{R_1 + R_2} + V_{tf} \tag{2}$$

$$V_{tr} = \frac{R_1 + R_2}{R_2} V_r \quad (3)$$

$$V_{tf} = \frac{R_1 + R_2}{R_2} V_r - \frac{R_1}{R_2} V_{DD} \quad (4)$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1}{R_2} V_{DD} \quad (5)$$

Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the supply voltage (V_{DD}) of the comparator, as shown in Figure 8.

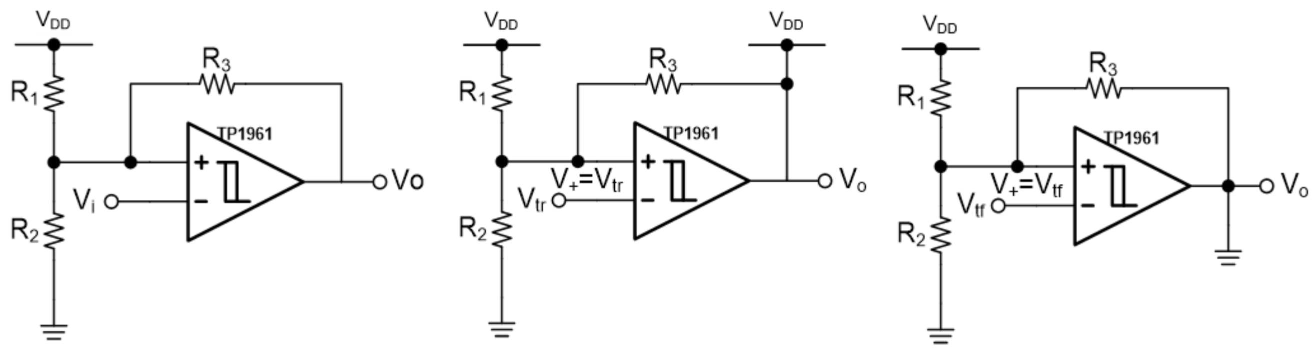


Figure 8. Inverting Configuration with Hysteresis

When V_i is greater than V_+, the output voltage is low. In this case, the three network resistors can be presented as paralleled resistor R_2 || R_3 in series with R_1. When V_i at the inverting input is less than V_+, the output voltage is high. The three network resistors can be represented as R_1 || R_3 in series with R_2.

$$V_{tr} = \frac{R_2}{R_1 \,||\, R_3 + R_2} V_{DD} \quad (6)$$

$$V_{tf} = \frac{R_2 \,||\, R_3}{R_2 \,||\, R_3 + R_1} V_{DD} \quad (7)$$

$$V_{hyst} = V_{tr} - V_{tf} = \frac{R_1 \,||\, R_2}{R_1 \,||\, R_2 + R_3} V_{DD} \quad (8)$$

Low Input Bias Current

The TP196x series is a CMOS comparator series and features very low input bias current in the pA range. The low input bias current allows the comparators to be used in applications with high resistance sources. Care must be taken to minimize the PCB surface leakage. See PCB Surface Leakage for more details.

PCB Surface Leakage

In applications where the low input bias current is critical, the Printed Circuit Board (PCB) surface leakage effects need to be considered. The surface leakage is caused by humidity, dust, or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 10^{12} Ω. A 5-V difference would cause a 5-pA current to flow, which is greater than the input bias current of the TP196x series at +27°C (±6 pA, typical). It is recommended to use the multi-layer PCB layout and route the −IN and +IN signal of the device under the PCB surface.

An effective way to reduce surface leakage is to use a guard ring around the sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 9 for inverting gain applications.

1. For non-inverting configuration:
   a. Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common-mode input voltage.
2. For inverting configuration:
   a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., V_{DD} / 2 or ground).
   b. Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

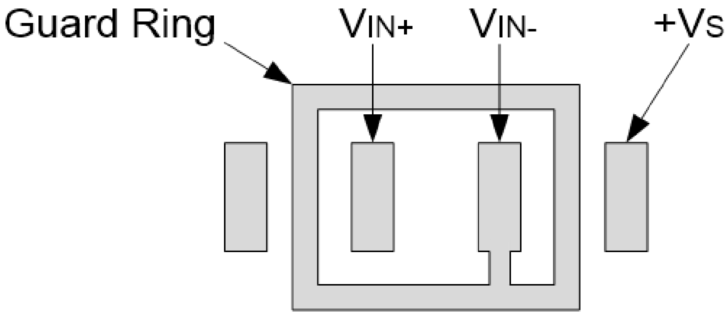


Figure 9. Example Guard Ring Layout of Inverting Comparator

Ground Sensing and Rail-to-Rail Output

The TP196x series implements a rail-to-rail topology that is capable of swinging to within 10 mV of either rail. Since the inputs can go 300 mV beyond either rail, the comparator can easily perform ‘True Ground Sensing'.

The maximum output current is a function of the total supply voltage. As the supply voltage of the comparator increases, the output current capability also increases. Attention must be paid to keeping the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5 V beyond either supply, otherwise the current flows through these diodes.

ESD

The TP196x series has reverse-biased ESD protection diodes on all inputs and outputs. The input and output pins cannot be biased more than 300 mV beyond either supply rail.

Power Supply Layout and Bypass

The power supply pin of the TP196x series should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for good high-frequency performance. It can also use a bulk capacitor (i.e., 1 μF or larger) within 100 mm to provide large and slow currents. This bulk capacitor can be shared with other analog parts.

The good ground layout improves performance by decreasing the amount of the stray capacitance and noise at the inputs and outputs of the comparator. To decrease the stray capacitance, minimize the PCB lengths and resistor leads, and place external components as close to the pins as possible.

Proper Board Layout

The TP196x series is a series of fast-switching, high-speed comparators and requires high-speed layout considerations. For best results, the following layout guidelines should be followed:

1. Use a printed circuit board (PCB) with a good and unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1-μF ceramic, surface-mount capacitor) as close as possible to the supply.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep the inputs away from the output.

4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to the propagation delay when the impedance is low. The topside ground plane should be placed between the output and inputs.
6. The ground trace of the ground pin should run under the device up to the bypass capacitor, and thus shielding the inputs from the outputs.

Typical Applications

IR Receiver

The TP1961 is an ideal candidate to be used as an infrared receiver shown in Figure 10. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across R_D. When this voltage level crosses the voltage applied by the voltage divider to the inverting input, the output transitions. Optional R_o provides additional hysteresis for the noise immunity.

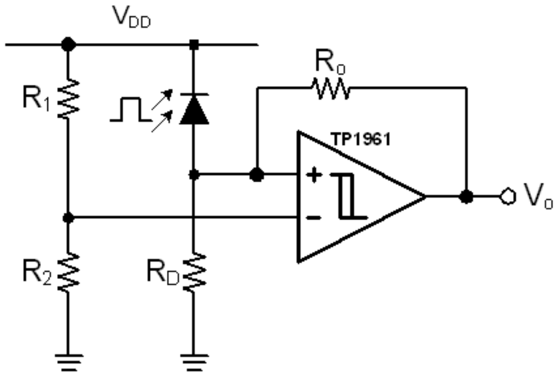


Figure 10. IR Receiver

Relaxation Oscillator

A relaxation oscillator using the TP1961 is shown in Figure 11. Resistors R_1 and R_2 set the bias point at the inverting input of the comparator. The period of the oscillator is set by the time constant of R_4 and C_1. The maximum frequency is limited by the large signal propagation delay of the comparator. The low propagation delay of the TP1961 guarantees the high frequency oscillation.

If the inverted input (V_{C1}) is lower than the noninverting input (V_A), the output is high which charges C_1 through R_4 until V_{C1} is equal to V_A. The value of V_A at this point is

$$V_{A1} = \frac{V_{DD} \cdot R_2}{R_1 \,||\, R_3 + R_2} \tag{9}$$

At this point, the comparator switches and pulls down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{DD} \cdot R_2 \,||\, R_3}{R_1 + R_2 \,||\, R_3} \tag{10}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{DD} / 3$, and $V_{A2} = V_{DD} / 3$.

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2\ V_{DD} / 3$ to $V_{DD} / 3$. Therefore, the frequency is:

$$\text{Freq} = \frac{1}{2 \cdot \ln 2 \cdot R_4 \cdot C_1} \quad (11)$$

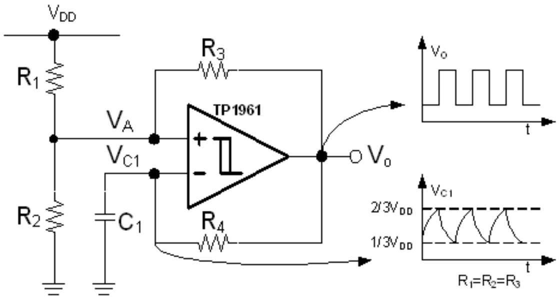


Figure 11. Relaxation Oscillator

Windowed Comparator

xref not found shows one approach to designing a windowed comparator using a single TP1962 chip. Choose different thresholds by changing the values of R_1, R_2, and R_3. Out A provides an active-low undervoltage indication, and Out B gives an active-low overvoltage indication. ANDing the two outputs provides an active-high, power-good signal. When the input voltage V_i reaches the overvoltage threshold V_{OH}, Out B gets low. Once V_i falls to the undervoltage threshold V_{UH}, Out A gets low. When $V_{UH} < V_i < V_{OH}$, the AND Gate gets high.

$$V_{OH} = V_r \cdot (R_1 + R_2 + R_3) / R_1 \quad (12)$$

$$V_{UH} = V_r \cdot (R_1 + R_2 + R_3) / (R_1 + R_2) \quad (13)$$

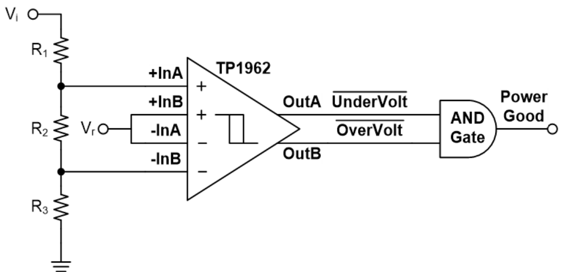
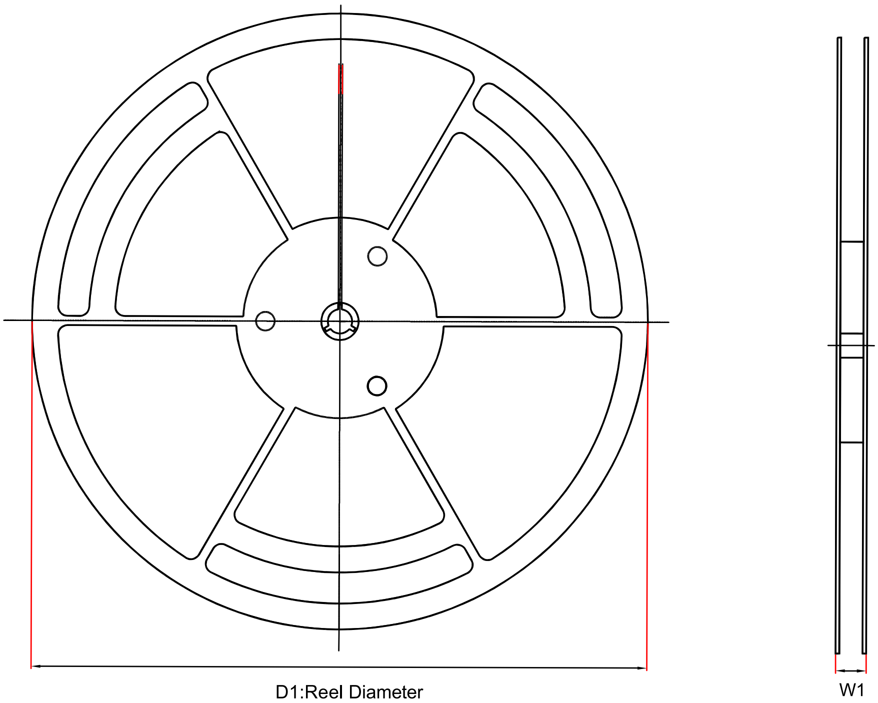
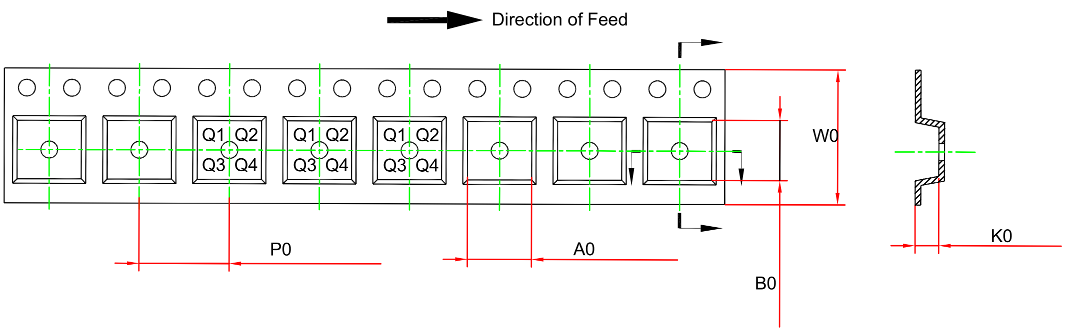


Figure 12. Windowed Comparator

Tape and Reel Information





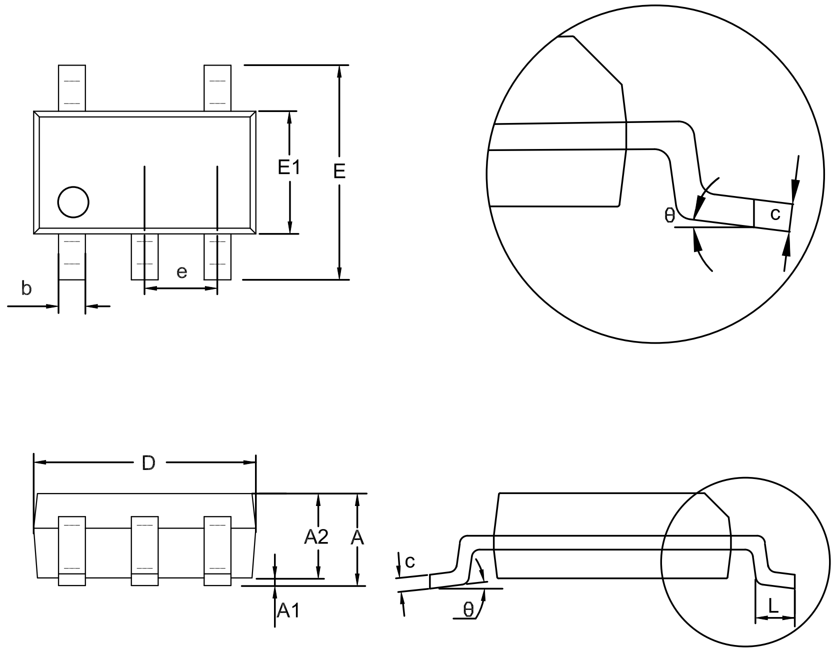
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm) (1)	B0 (mm) (1)	K0 (mm) (1)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TP1961-TR	SOT23-5	180.0	12.0	3.3	3.25	1.4	4.0	8.0	Q3
TP1961-CR	SOT353(SC70-5)	178.0	12.1	2.4	2.5	1.2	4.0	8.0	Q3
TP1962-FR	DFN2x2-8	180.0	12.5	2.3	2.3	1.1	4.0	8.0	Q1
TP1962-SR	SOP8	330	17.6	6.5	5.4	2.0	8.0	12.0	Q1
TP1962-VR	MSOP8	330	17.6	5.3	3.4	1.3	8.0	12.0	Q1

(1) The value is for reference only. Contact the 3PEAK factory for more information.

Package Outline Dimensions

SOT23-5

Package Outline Dimensions S5T(SOT23-5-A)



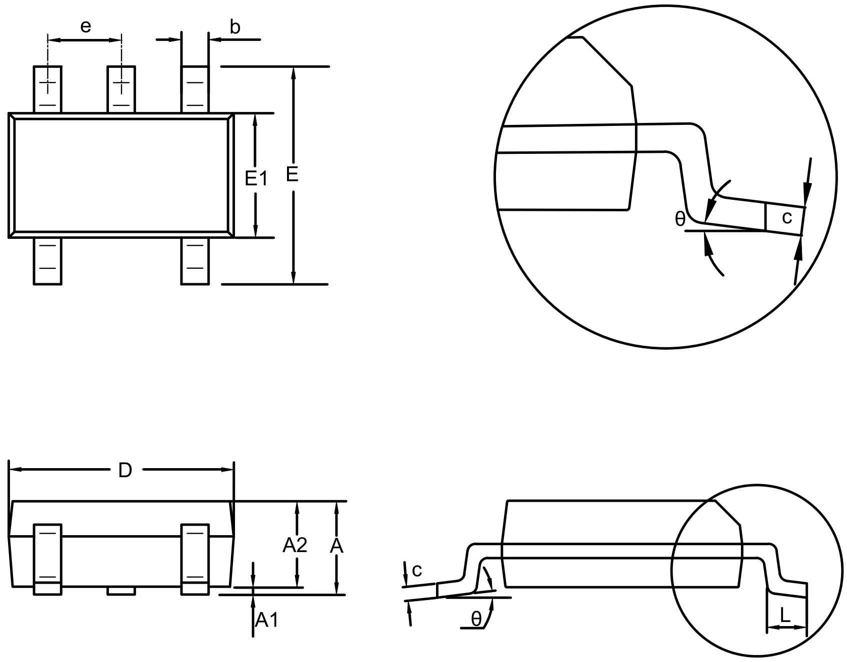
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.280	0.500	0.011	0.020
c	0.100	0.230	0.004	0.009
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.720	0.059	0.068
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOT353 (SC70-5)

Package Outline Dimensions SC5(SOT353-5-A)



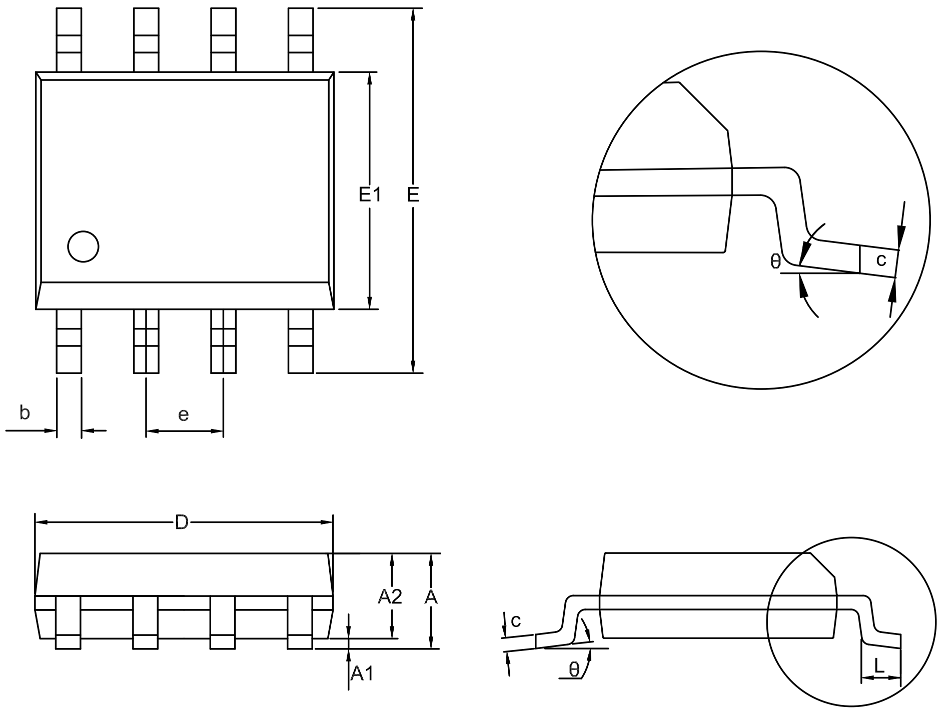
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.850	1.100	0.033	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.230	0.004	0.009
D	2.000	2.200	0.079	0.087
E	2.150	2.450	0.085	0.096
E1	1.150	1.350	0.045	0.053
e	0.650 BSC		0.026 BSC	
L	0.260	0.460	0.010	0.018
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP8

Package Outline Dimensions SO1(SOP-8-A)



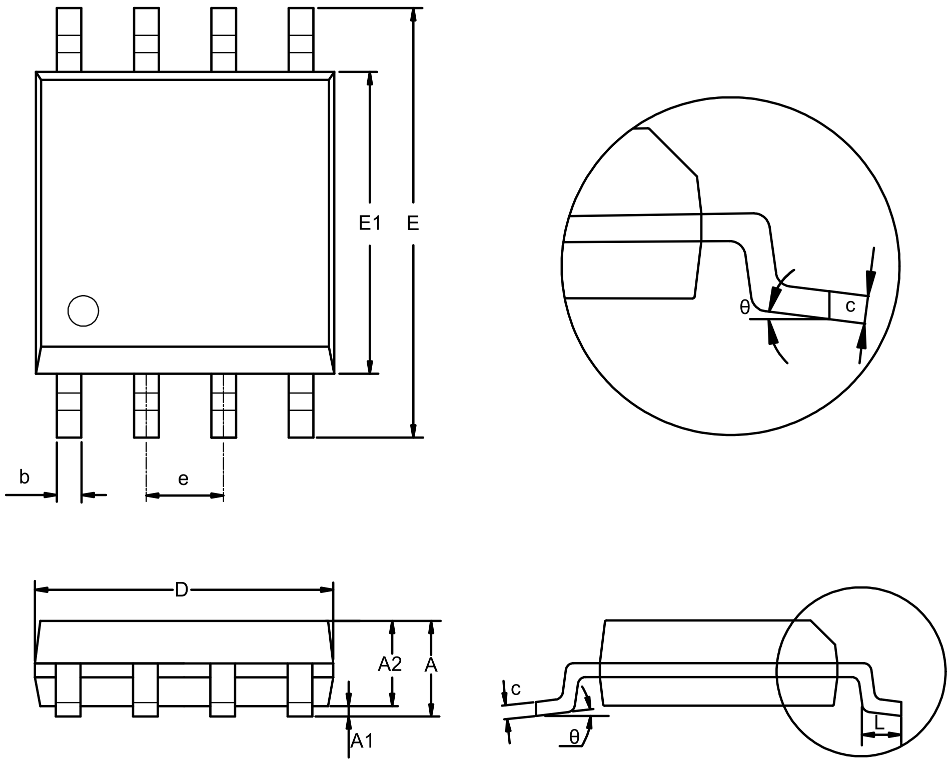
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

MSOP8

Package Outline Dimensions VS1(MSOP-8-A)



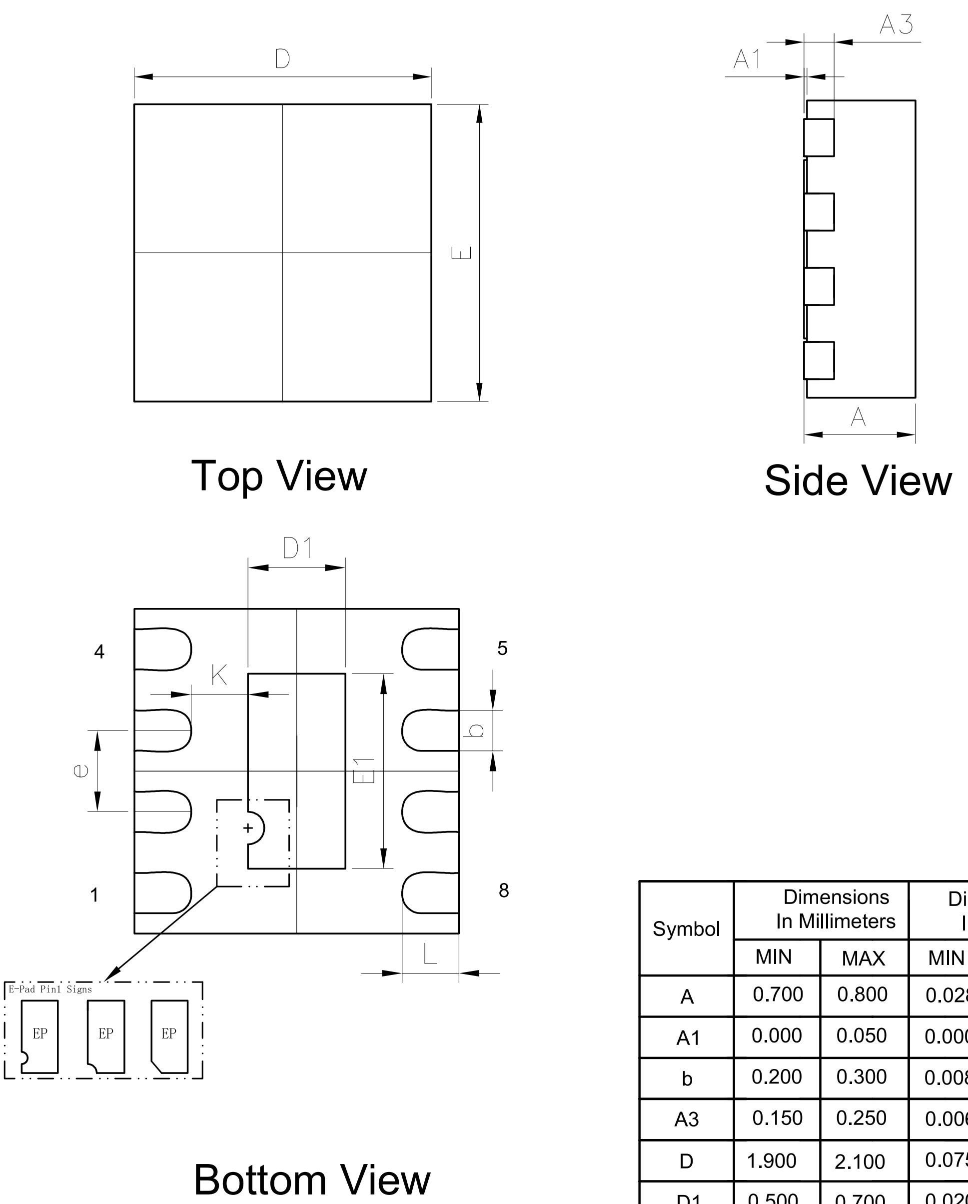
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN2X2-8

Package Outline Dimensions DF4(DFN2X2-8-A)



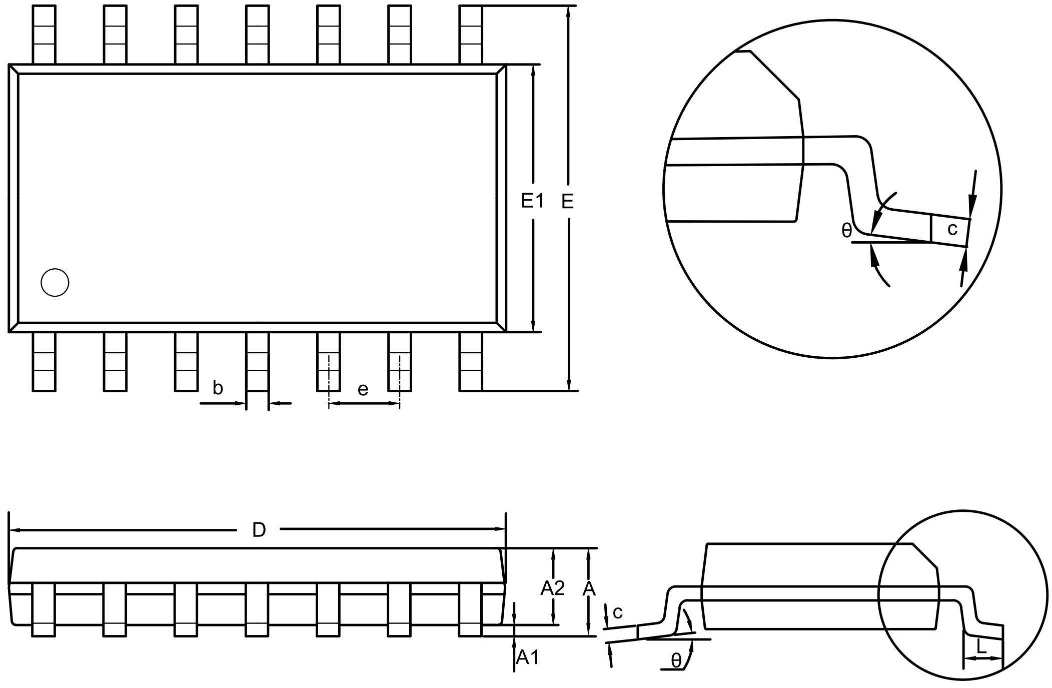
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
A3	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D1	0.500	0.700	0.020	0.028
E	1.900	2.100	0.075	0.083
E1	1.100	1.300	0.043	0.051
e	0.500 BSC		0.020BSC	
L	0.274	0.426	0.011	0.017

SOP14

Package Outline Dimensions SO2(SOP-14-A)



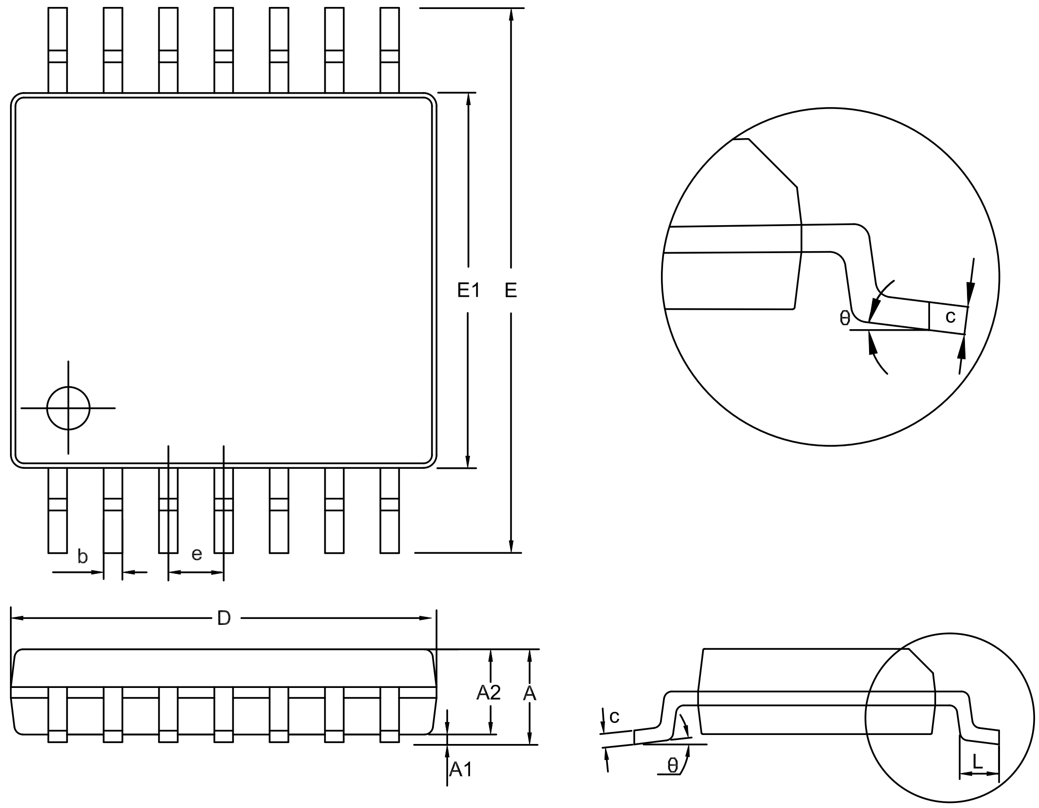
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP14

Package Outline Dimensions TS2(TSSOP-14-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TP1961-TR	−40 to 125°C	SOT23-5	961	MSL3	Tape and Reel, 3000	Green
TP1962-FR	−40 to 125°C	DFN2X2-8	962	MSL3	Tape and Reel,3000	Green
TP1962-SR	−40 to 125°C	SOP8	TP1962	MSL3	Tape and Reel,4000	Green
TP1961-CR	−40 to 125°C	SOT353(SC70-5)	961	MSL3	Tape and Reel,3000	Green
TP1962-VR (1)	−40 to 125°C	MSOP8	TP1962	MSL3	Tape and Reel,3000	Green

(1) For future products, contact the 3PEAK factory for more information and samples.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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