Quad-Channel High Voltage Output DAC

Features

- Quad-Channel High Voltage Digital-to-Analog Converter (DAC) with a 12-bit Resolution
- Pin-Selectable Output Range of 30 V or 60 V
- Integrated Precision Reference for Enhanced Accuracy
- Low Power Serial Interface with Readback Capability for Output Verification
- Integrated Temperature Sensor with an Alarm Function to Detect Temperature Anomalies
- Power-on Reset Feature for Reliable Startup
- Simultaneous Updating of All Channels via the LDAC Pin for Synchronized Outputs
- Wide Operating Temperature Range: −40°C to +125°C

Applications

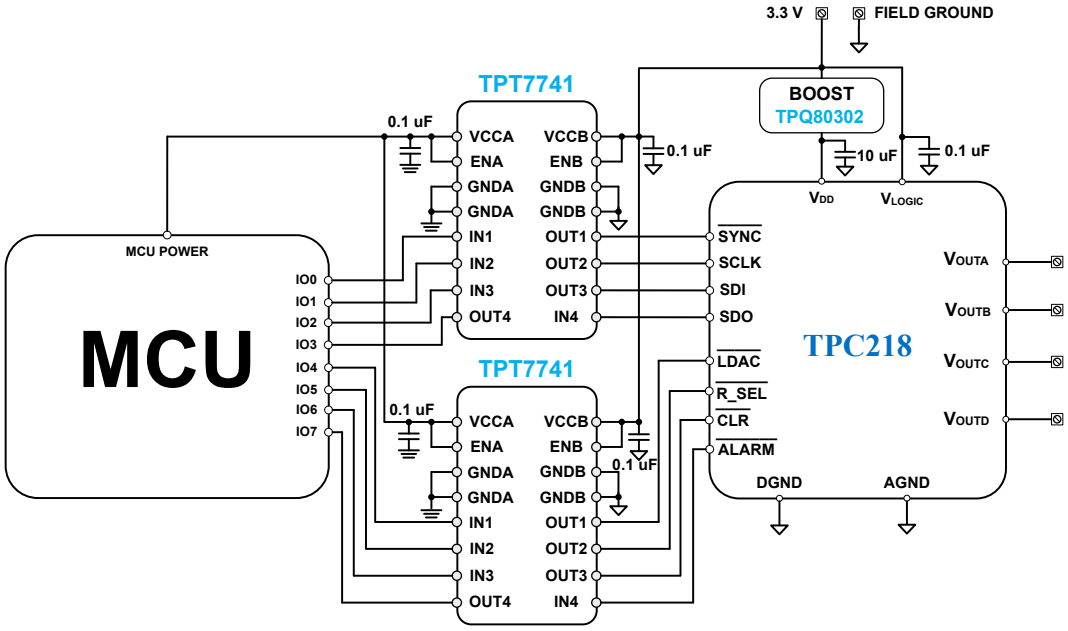
- High Voltage Bias for Optical Communications
- Programmable Voltage Sources

Description

The TPC2182 is a quad-channel 12-bit digital-to-analog converter (DAC) that features integrated high-voltage output amplifiers and a precision reference on the chip. The output voltage of the DAC can be tailored using the range select pin (R_SEL). When R_SEL is set to a high state, the output spans from 0 V to 30 V. Conversely, setting R_SEL to a low state extends the range from 0 V to 60 V.

The device has a high-speed serial interface compatible with various industry standards, including SPI®, QSPI™, MICROWIRE™, and DSP interfaces.

Typical Application Circuit



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Product Family Table

Order Number	Resolution	Output Range(V)	Package
TPC2182-TS3R	12	30/60	TSSOP16

Revision History

Date	Revision	Notes
2024-09-12	A.0	First version.

Pin Configuration and Functions

TSSOP16 Package
Top View

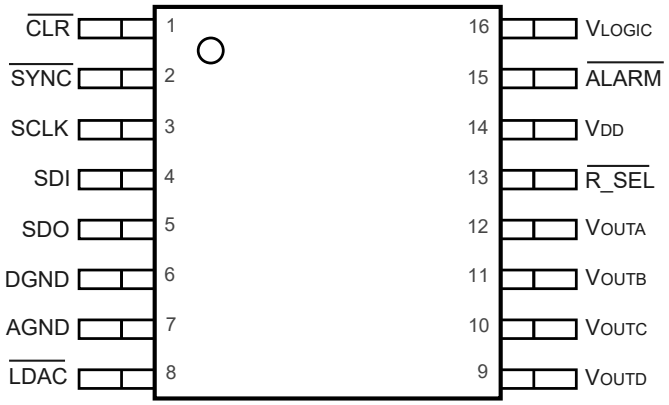


Table 1. Pin Function Descriptions

Pin No	Mnemonic	Description
1	$\overline{CLR}$	Asynchronous Clear Input, is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the input register and the DAC register are set to 0x000 and the outputs to zero scale.
2	$\overline{SYNC}$	Falling Edge Synchronization Signal, the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the rising edges of the following clocks.
3	SCLK	Serial Clock Input. Data is clocked into the input shift register on the rising edge of the serial clock input.
4	SDI	Serial Data Input. Data is clocked into the register on the rising edge of the serial clock input.
5	SDO	Serial Data Output. CMOS output. This pin serves as the readback function for all DAC and control registers. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
6	DGND	Digital Ground Pin.
7	AGND	Analog Ground Pin.
8	$\overline{LDAC}$	Load DAC Input. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to update simultaneously. Alternatively, this pin can be tied permanently low.
9	V_{OUTD}	Buffered Analog Output Voltage from DAC D.
10	V_{OUTC}	Buffered Analog Output Voltage from DAC C.
11	V_{OUTB}	Buffered Analog Output Voltage from DAC B.

Pin No	Mnemonic	Description
12	V_{OUTA}	Buffered Analog Output Voltage from DAC A.
13	$\overline{R\_SEL}$	Range Select Pin. Low: selects DAC output range of 0 V to 60 V. High: selects DAC output range of 0 V to 30 V.
14	V_{DD}	Positive Analog Power Supply.
15	$\overline{ALARM}$	Active Low CMOS Output Pin.
16	V_{LOGIC}	Logic Power Supply

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	VDD to GND	–0.3	70	V
	V_{LOGIC} to DGND	–0.3	6	V
	Analog Output to GND	–0.3	VDD + 0.3	V
	Digital Input to GND	−0.3	V_{LOGIC} + 0.3	V
	SDO Output to GND	−0.3	V_{LOGIC} + 0.3	V
	AGND to DGND	−0.3	0.3	V
T_A	Operating Temperature	−40	125	°C
T_{STG}	Storage Temperature	−65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V_{DD}	Analog Supply Voltage	10		65	V
V_{LOGIC}	Logic Supply Voltage	2.3		5.5	V
T_A	Operating Ambient Temperature	−40		125	°C

Thermal Information

Thermal Metric		TSSOP16	Unit
Θ_{JA}	Junction-to-Ambient Thermal Resistance	112.6	°C/W

Electrical Characteristics

All minimum/maximum specifications: V_{DD} = 10 to 65 V, V_{IO} = 2.3 to 5.5 V , Internal V_{REFIN} = 4 V, R_{LOAD} = 60 kΩ to GND, C_{LOAD} = 200 pF to GND, digital inputs at V_{IO} or GND, T_J = –40℃ to +105℃ and all typical specifications at T_J = 25℃.

Parameter		Test Conditions	Min	Typ	Max	Unit
Static Performance Note: Static performance specified with DAC outputs unloaded for all gain options, unless otherwise noted. End point fit between codes. 16-bit: Code 512 to 65280						
Resolution				12		Bits
DNL	Differential Nonlinearity	Specified 12-bit monotonic			±1	LSB
INL	Integral Nonlinearity	60-V Mode			±1	LSB
		30-V Mode			±1	LSB
	Voutx TC			50		ppm/°C
OE	Offset Error	DAC code = 32 for 60 V mode; DAC code = 64 for 30 V mode	−40		40	mV
	Offset Error Temperature Drift			60		µV/°C
GE	Gain Error		−0.35		0.35	%FSR
	Gain Error Temperature Drift			10		ppm of FSR/°C
ZSE	Zero-scale Error				20	mV
	Zero-scale Error Temperature Drift			60		µV/°C
FSE	Full-scale Error	60-V mode	−200		200	mV
		30-V mode	−100		100	mV
	Full-scale Error Temperature Drift	−40°C to +25°C; 60-V mode		1000		µV/°C
		+25°C to +105°C; 60-V mode		350		
Output Characteristics						
Voltage Range		60-V Mode	0		60	V
		30-V Mode	0		30	V
Output Voltage Headroom		I_{LOAD} < 1 mA	AGND +0.5		VDD - 0.5	V
Short Circuit Current		DAC code = middle scale. Output shorted to GND		2.6		mA
CL	Capacitive Load Stability	R_{LOAD}= 60 k to ∞	0		1	nF
RL	Resistive Load			60		kΩ
	Load Current	On any single channel		±1		ma
Load Regulation		DAC code = midscale, −1 mA <= IOUT<= 1 mA		85		µV/mA
DC Output Impedance		DAC code = midscale		3		Ω
DC CrossTalk		Due to Single Channel Full-Scale Output Change		3		mV

Parameter		Test Conditions	Min	Typ	Max	Unit
		Due to Powering Down (Per Channel)		4		mV
DC Output Leakage				10µ		µA
Dynamic Performance						
Tst	Output Voltage Settling Time	¼ to ¾ scale settling to ±1 LSB, 60-V Mode		50		µs
		¼ to ¾ scale settling to ±1 LSB, 30-V Mode		30		µs
	Slew Rate	10% to 90% scale		0.65		V/µs
Vn	Output Noise	0.1 Hz to 10 Hz, midscale code		240		µVpp
		0.1 Hz to 10K Hz, midscale code		4		mVpp
PSRRac	AC PSRR	Midscale code, frequency = 60 Hz, amplitude = 200 mVPP superimposed on V_{DD}		85		dB
PSRRdc	DC PSRR	Full-scale code, 60-V Mode		70		dB
		Full-scale code, 30-V Mode		80		dB
	Digital to Analog Glitch Impulse Energy	1 LSB change around major carrier, 60-V Mode		300		nV-s
	Glitch Impulse Peak Amplitude	60-V Mode		170		mV
	Digital Feedthrough			40		nV-s
	Digital Crostalk			5		nV-s
	Analog Crosstalk			600		nV-s
	DAC to DAC Crosstalk			600		nV-s
	Power-up Time	VDD = 62 60-V MODE		20		µs
	Power-down Glitch Amplitude	VDD = 62 ENABLE		25		mV
	Overshot/Downshot	1/4 to 3/4 scale and 3/4 to 1/4 scale 60-V mode		10		mV
	Channel-to-channel DC Crosstalk	Measured DAC output at midscale, adjacent channel at full-scale		5		µV
		Measured DAC output at midscale, all other DAC outputs at full-scale		10		µV
Internal Reference Characteristics						
V_{REFOUT}	Internal Reference Voltage	T_A = 25°C		4		V
TC	Internal Reference Temperature Coefficient	T_J = −40°C to 125°C		10		ppm/°C
Digital Input Characteristics						
V_{IH}	High-level Input Voltage	V_{LOGIC} = 4.5 ~ 5.5 V	2			V

Parameter		Test Conditions	Min	Typ	Max	Unit
		V_{LOGIC} = 2.3 ~ 4.5 V	1.8			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{hys}	Input Vhys	V_{LOGIC} = 3.6		65		mV
	Input Current				±1	μA
	Input Pin Capacitance			5		pF
Digital Output Characteristics						
V_{OH}	High-level Output Voltage	I_{LOAD} = 0.2 mA	V_{IO} – 0.4			V
V_{OL}	Low-level Output Voltage	I_{LOAD} = 0.2 mA			DGND + 0.4	V
	Output Pin Capacitance			5		pF
Power Consumption Characteristics						
I_{VDD}	VDD Supply Current	Active mode. Internal reference enabled. DAC code = mid scale. Outputs unloaded. SPI static		2	3	mA
	Power Down Mode	Software Power-down		50		μA
I_{VIO}	VIO Supply Current	V_{IH} = V_{LOGIC}; V_{IL} = DGND		1	10	μA

Timing Requirements

All minimum/maximum specifications: V_{DD} = 10 to 65 V, V_{IO} = 2.3 to 5.5 V , Internal VREFIN = 4 V, R_{LOAD} = 60 kΩ to GND, C_{LOAD} = 200 pF to GND, digital inputs at V_{IO} or GND, T_J = –40℃ to +105℃ and all typical specifications at T_J = 25℃.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1[2]	SCLK Cycle Time	60			ns
t_2	SCLK High Time	10			ns
t_3	SCLK Low Time	10			ns
t_4	SYNC Falling Edge to SCLK Rising Edge Setup Time	25			ns
t_5	Data Setup Time	15			ns
t_6	Data Hold Time	5			ns
t_7	SCLK Falling Edge to SYNC Rising Edge	0			ns
t_8	Minimum SYNC High Time	20			ns
t_9	LDAC Pulse Width Low	20			ns
t_{10}	SCLK Falling Edge to LDAC Rising Edge	50			ns
t_{11}	CLR Pulse Width Low	15			ns
t_{12}	CLR Pulse Activation Time		100		ns
t_{13}	ALARM Clear Time		20		μs
t_{14}	SCLK Cycle Time in Read Mode	110			ns
t_{15}[3]	SCLK Rising Edge to SDO Valid			55	ns
t_{16}[3]	SCLK to SDO Data Hold Time	25			ns
t_{17}[4]	Power-on Reset Time (this is not shown in the timing diagrams)			50	μs
t_{18}[5]	Power-on Time (this is not shown in the timing diagrams)			50	μs
t_{19}	ALARM Clear to Output Amplifier Turn on (this is not shown in the timing diagrams)		5		μs

(1) Guaranteed by characterization; not production tested.
(2) All input signals are specified with tR = tF = 5 ns (10% to 90% of DVCC) and timed from a voltage level of 1.2 V.
(3) See Figure 2, Figure 3, and Figure 4.
(4) CL SDO = capacitive load on SDO output.

Timing Diagrams

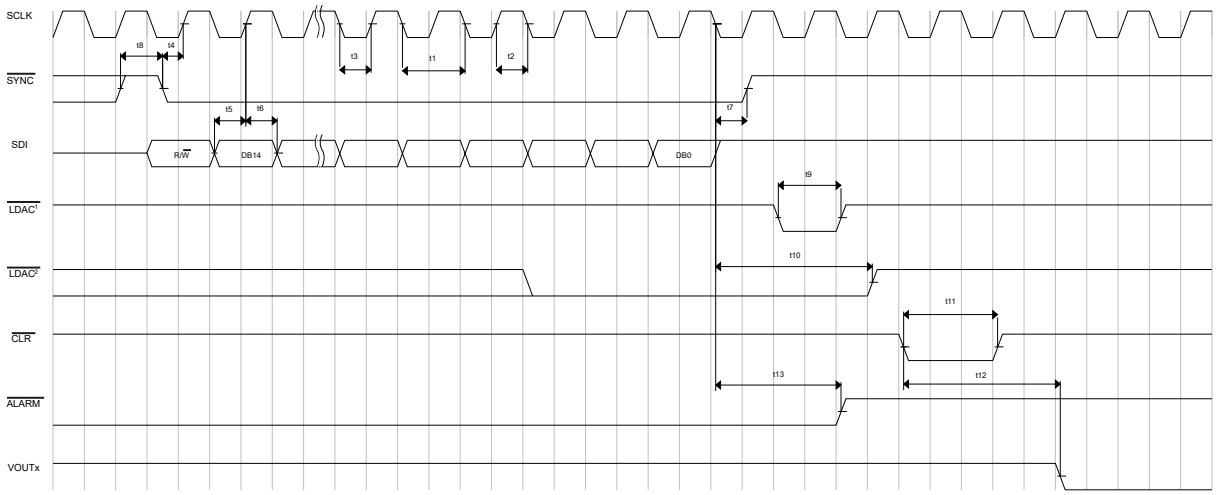


Figure 1. Write Timing Diagram

(1) ASYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE MODE.
(2) SYNCHRONOUS $\overline{\text{LDAC}}$ UPDATE MODE.
(3) IN THE EVENT OF OVERTEMPERATURE CONDITIONS.
(4) VOUTx REFERS TO ANY OF VOUTA, VOUTB, VOUTC OR VOUTD.

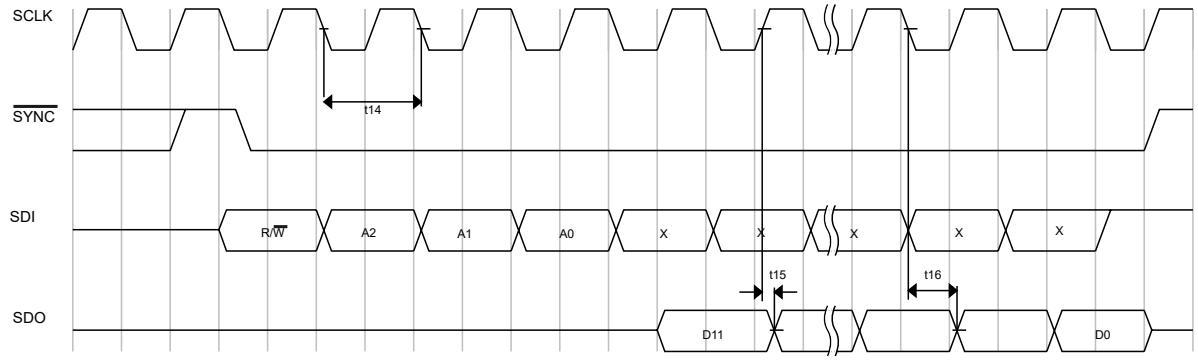


Figure 2. Read Timing Diagram

Typical Performance Characteristics

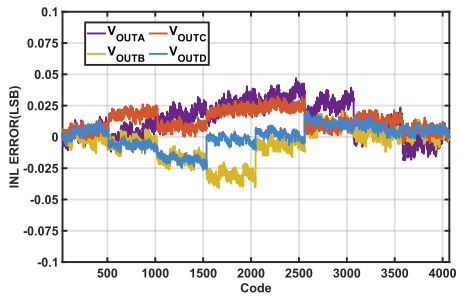


Figure 3. Typical INL

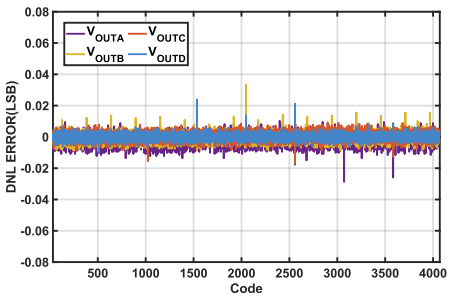


Figure 4. Typical DNL

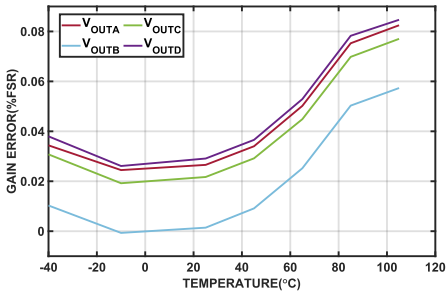


Figure 5. Gain Error vs. Temperature

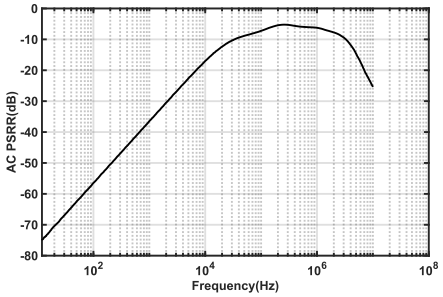


Figure 6. AC PSRR

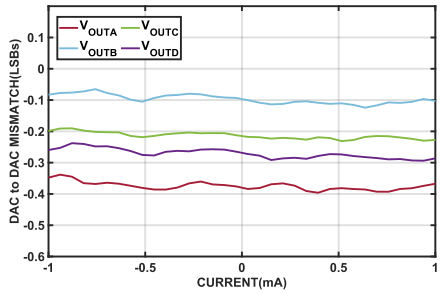


Figure 7. DAC to DAC mismatch

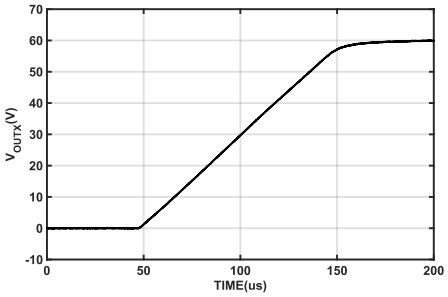


Figure 8. Full-Scale Voltage Positive Step

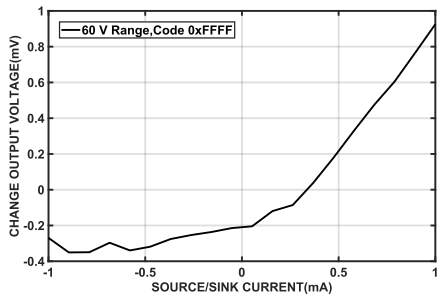


Figure 9. DAC Output Capability

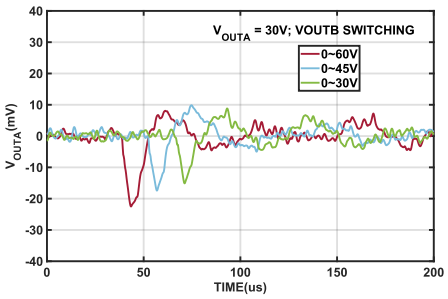


Figure 10. DAC to DAC Crosstalk

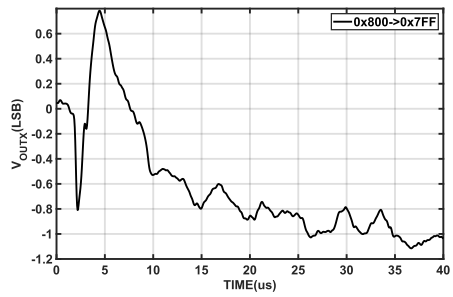


Figure 11. Digital to Analog Positive Glitch Impulse

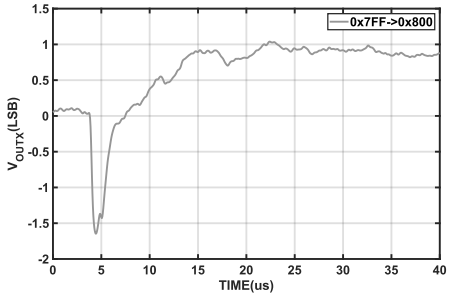


Figure 12. Digital to Analog Negative Glitch Impulse

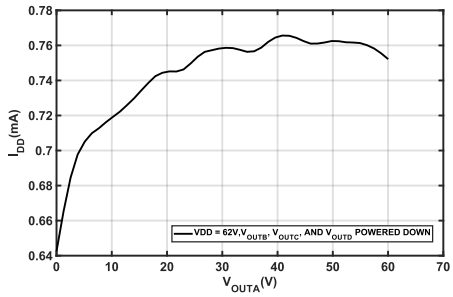


Figure 13. I_{DD} vs. V_{OUTA}

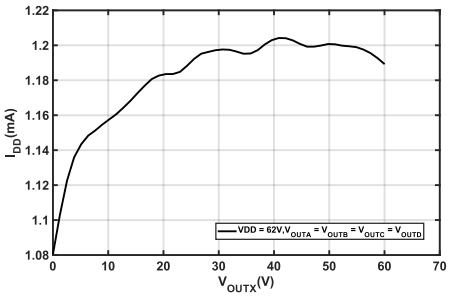


Figure 14. I_{DD} vs. $V_{OUTA}$to V_{OUTD}

Detailed Description

Overview

The device integrates four digital-to-analog converters (DACs), four output amplifiers, and a high-precision reference voltage source within a compact package. Each DAC channel is composed of a 12-bit resistive string DAC with a high-voltage output buffer amplifier. This component functions with a single power supply voltage. The voltage range of the DAC output is determined by the state of the range selection pin, $\overline{R\_SEL}$. When $\overline{R\_SEL}$ is set high, the output spans from 0 V to 30 V; when set low, it extends from 0 V to 60 V. Data is input to the device in a 16-bit word format, through a serial communication interface.

Functional Block Diagram

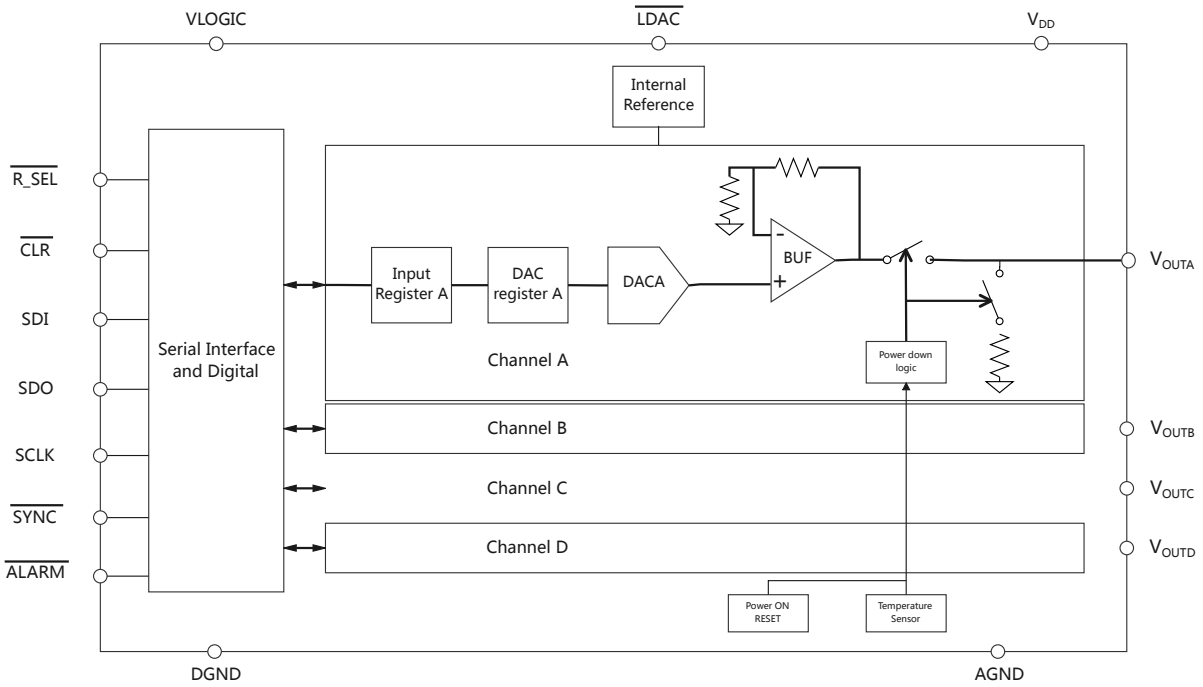


Figure 15. Functional Block Diagram

Feature Description

Power Up State

the device's power-on reset circuitry initializes the control register's bits to 0x40 on power up. This default setting is specifically designed to minimize power usage. Users are able to set the DAC registers to desired values. Additionally, the power-on reset mechanism guarantees that all input and DAC registers start in a predefined state, 0x000, and maintain this state until a proper write operation to the device is executed. The activation of the analog section can be achieved by setting any combination of Bits C2 through C5 in the control register to the value of 1.

Power Down Mode

Each DAC channel can be powered up or down through manipulation of the control register (refer to Table 10),. When a DAC channel is in a power-down state, its corresponding analog circuitry is deactivated, thereby cutting down on power usage. Meanwhile, the digital section of the device continues to operate. The output of the DAC could be three-stated or connected to AGND by an internal resistor.

The activation of the power-down mode is contingent upon the status of Bit C6 within the control register. This mode is designed to preserve the DAC register's contents, ensuring that the channel resumes its prior voltage level once the power-down bit is activated. The device provides users with the capability to update the DAC registers even while in power-down mode. Moreover, the control register is accessible for reading at any moment, allowing users to verify the status of its bits.

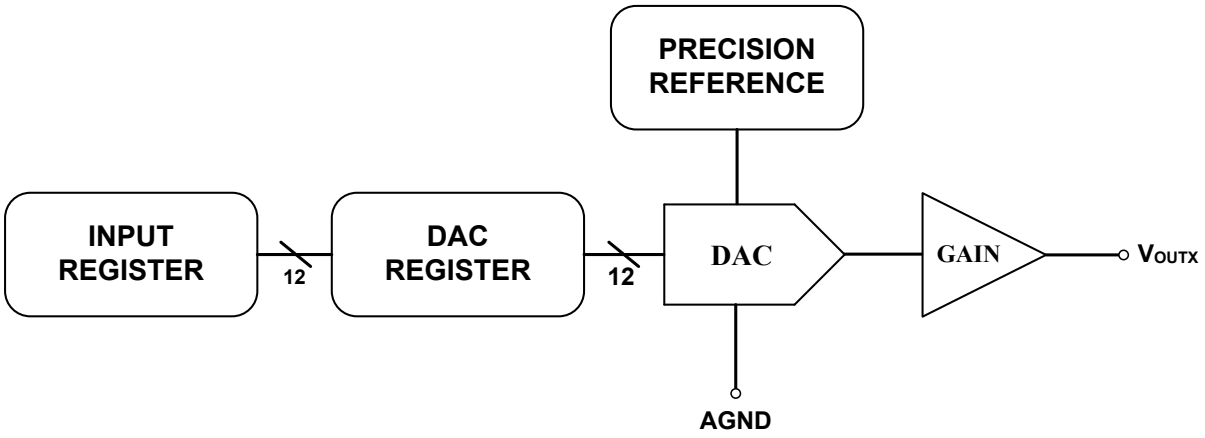


Figure 16. DAC Channel Architecture (Single Channel Shown)

DAC Channel

The device's data format is straight binary and the output voltage follows the formula:

$$V_{OUT} = \frac{D}{4096} \times \text{Range} \quad (1)$$

Where:

D is the code loaded to the DAC.

Range = 30, if $\overline{\text{R\_SEL}}$ is high, and 60 if $\overline{\text{R\_SEL}}$ is low.

SELECTING THE OUTPUT RANGE

The selection of the DACs' output voltage range is controlled by the $\overline{\text{R\_SEL}}$ pin. By setting the $\overline{\text{R\_SEL}}$ pin to Logic 1, the output voltage range is confined between 0 V and 30 V. Conversely, when the $\overline{\text{R\_SEL}}$ pin is set to Logic 0, the range expands to span from 0 V to 60 V. The $\overline{\text{R\_SEL}}$ pin can be altered at any time, provided that the serial interface is idle, meaning it is not engaged in a read or write operation. Upon changing the state of the $\overline{\text{R\_SEL}}$ pin, the output voltage at the pin remains constant until the DAC register is updated with a new value and the $\overline{\text{LDAC}}$ signal is set low or pulsed low. For instance, if a user writes the value 0x800 to the DAC register while in the 30 V mode (with $\overline{\text{R\_SEL}}$ set to 1), the resulting output voltage would be 15 V, given that $\overline{\text{LDAC}}$ is either low or has been pulsed to a low state. When the user transitions to the 60 V mode (with $\overline{\text{R\_SEL}}$ set to 0), the output voltage maintains at 15 V until a new value is written to the DAC register. The $\overline{\text{LDAC}}$ signal must be low or pulsed to a low state to effect a change in the output voltage.

$\overline{\text{CLR}}$ Function

The device has a hardware $\overline{\text{CLR}}$ pin that is an asynchronous clear input. The $\overline{\text{CLR}}$ input is falling edge-sensitive. Bringing the $\overline{\text{CLR}}$ line low clears the contents of the input register and the DAC registers to 0x000.

$\overline{\text{LDAC}}$ Function

The DAC outputs in the device can be refreshed through the use of the hardware $\overline{\text{LDAC}}$ pin. Under normal conditions, the $\overline{\text{LDAC}}$ pin remains in a high state. When a falling edge is detected on the $\overline{\text{LDAC}}$ pin, the data from the input registers is transferred to the DAC registers, resulting in an immediate and simultaneous update of all DAC outputs (this is known as the asynchronous update mode). Conversely, if the $\overline{\text{LDAC}}$ pin is held in a low state, or if it transitions to a low state on the falling edge of the 16th SCLK (Serial Clock) pulse, the designated DAC register and its corresponding output are updated automatically (this is referred to as the synchronous update mode).

Temperature Sensor

The device features a built-in temperature sensor that triggers a thermal shutdown procedure when the temperature on the chip exceeds the threshold of 110°C. Once in thermal shutdown mode, the analog components of the device are automatically powered off, and the DAC outputs are isolated. However, the digital section of the device continues to function effectively, as in the action of setting the power-down bit in the control register. In temperature shut down mode, Bit 0 of the control register is set to 1, and the $\overline{\text{ALARM}}$ pin goes low, even if the die temperature falls, until Bit 0 in the control register is cleared to 0.

Power Supply Sequencing

The device allows for the power supply connections to be made in any sequence without causing any disruption to the device's operation. Nevertheless, it is essential to connect the AGND and DGND pins to the appropriate ground plane before connecting the power supplies. During the power-up process, it is imperative to avoid leaving any of the digital input pins, including SCLK, SDI, $\overline{\text{SYNC}}$, $\overline{\text{R\_SEL}}$, and $\overline{\text{CLR}}$, in a floating state. To prevent this, the digital input pins can be appropriately linked with pull-up resistors to the VLOGIC level or pull-down resistors to the DGND level, depending on the specific requirements.

Serial Interface and Register

The device is equipped with a serial interface that includes the $\overline{\text{SYNC}}$, SCLK, SDI, and SDO pins, designed to be compatible with the SPI. Through this interface, it is possible to write data to the input and control registers of the device. However, the DAC registers are not accessible for direct writing or reading. The input shift register within the device is 16 bits in length. This 16-bit word format is structured to include one read/write (R/W) control bit at the beginning, succeeded by three address bits, and concluding with 12 bits dedicated to the DAC data. The loading of data into the shift register occurs with the most significant bit (MSB) first.

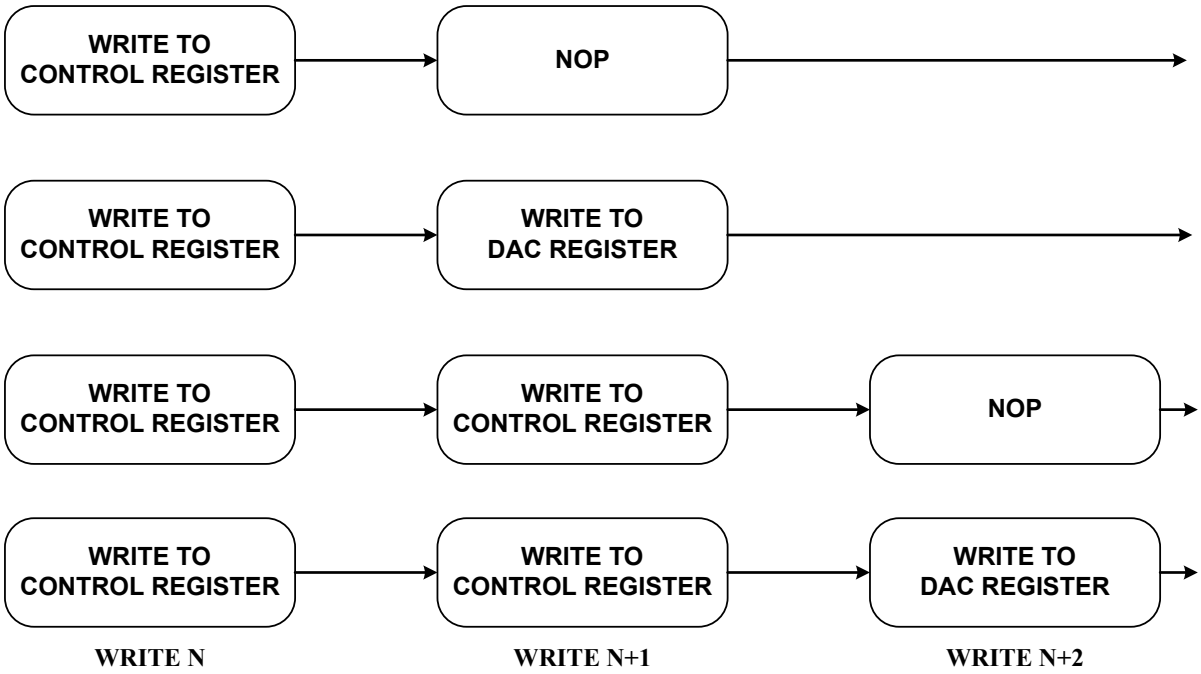


Figure 17. Control Register Write Sequences

Write Mode

To write data to a register in the device, set the R/$\overline{W}$ bit to 0, and use the three address bits (A2 to A0) to select the target register. Data is loaded during the 12 SCLK pulses following the address bits. The write process starts with a low $\overline{SYNC}$ signal and concludes on the 16th SCLK falling edge, executing the programmed function. The device conserves power by requiring SCLK only during writes. After writing, the $\overline{SYNC}$ line should be high for at least 20 ns to prepare for the next write. Keeping interface pins near supply rails minimizes power consumption.

Read Mode

The device facilitates data readback from all accessible registers except the DAC registers through its serial interface. To initiate a readback, the R/W bit must be set to 1, and the address bits will select the register. The data from the chosen register is then sent out via the SDO pin during the subsequent twelve clock cycles. The SDO pin, normally in a high-impedance state, becomes active on the fifth SCLK pulse's rising edge and stays active until the data transfer is complete or the $\overline{SYNC}$ line goes high. The SPI interface's maximum read operation speed should meet the timing requirement of t14.

Writing to the Control Register

The control register is written when Bits [DB14:DB12] are 1. The control register sets the power-up state of the DAC outputs. A write to the control register must be followed by another write operation. The second write operation can be a write to a DAC input register or a NOP write.

Register Table

Table 2. Input Register Bit Map

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/$\overline{W}$	A2	A1	A0	Data											

Table 3. Input Register Bit Functions

Bit R/$\overline{W}$	Description Indicates a read from or a write to the addressed register.			
A2, A1, A0	These bits determine if the input registers or the control register are to be accessed.			
	A2	A1	A0	Function/Address
	0	0	0	No operation
	0	0	1	DAC A input register
	0	1	0	DAC B input register
	0	1	1	DAC C input register
	1	0	0	DAC D input register
	1	0	1	Write data contents to all four DAC input registers
	1	1	0	Reserved
	1	1	1	Control register
D11:D0	Data bits			

Table 4. Control Register Functions

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0[1]
	1	1	1	0	0	0	0	0	C6	C5	C4	C3	C2	C1	C0

(1) Read-only bit. This bit should be 0 when writing to the control register.

Bit No.	Bit Name	Description
DB0	C0	C0 = 0: the device is not in thermal shutdown mode.
		C0 = 1: the device is in thermal shutdown mode.
DB1	C1	C1 = 0: reserved. This bit should be 0 when writing to the control register.
DB2	C2[1]	C2 = 0: DAC Channel A power-down (default).
		C2 = 1: DAC Channel A power-up.
DB3	C3[1]	C3 = 0: DAC Channel B power-down (default).
		C3 = 1: DAC Channel B power-up.
DB4	C4[1]	C4 = 0: DAC Channel C power-down (default).
		C4 = 1: DAC Channel C power-up.
DB5	C5[1]	C5 = 0: DAC Channel D power-down (default).
		C5 = 1: DAC Channel D power-up.
DB6	C6	C6 = 0: outputs connected to AGND through a 20 kΩ resistor (default).
		C6 = 1: outputs are three-stated.

(2) If Bit C2 to Bit C5 are set to 0, the part is placed in power-down mode.

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPC2182 is quad-channel, 12-bit, serial input, digital-to-analog converter with on-chip high voltage output amplifiers and an integrated precision reference. Customer can use TPC2182 and other power and interface products of 3PEAK to build an overall solution.

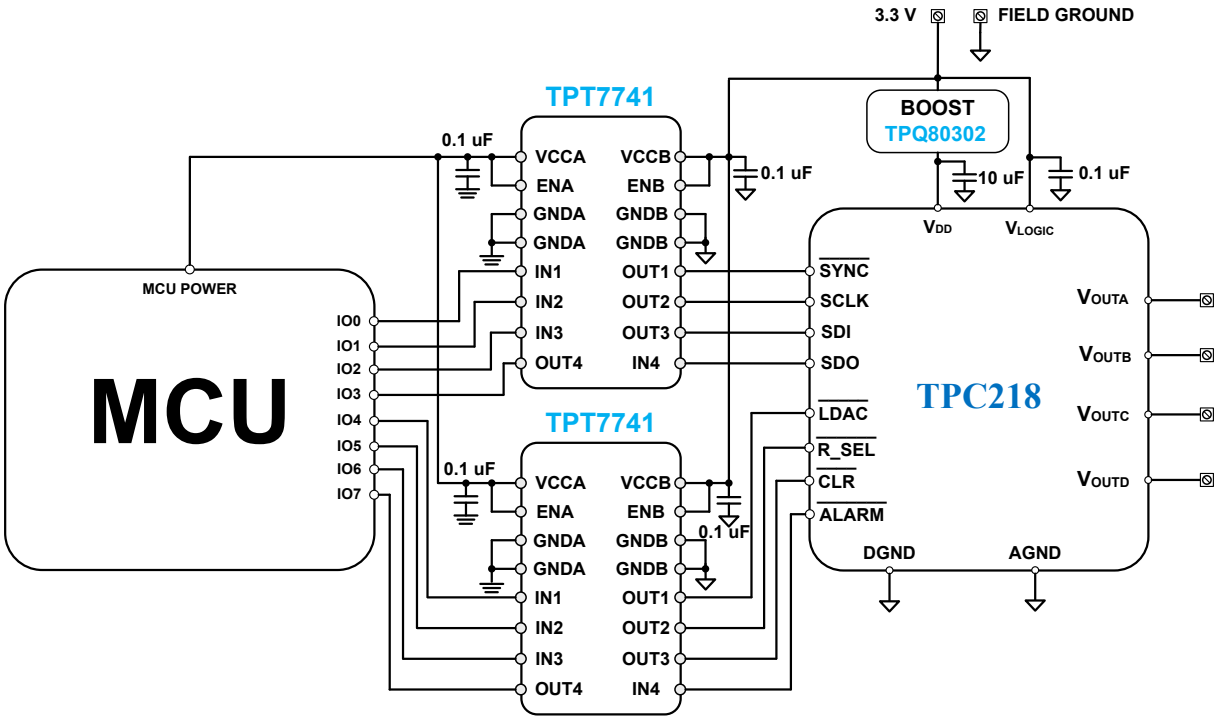
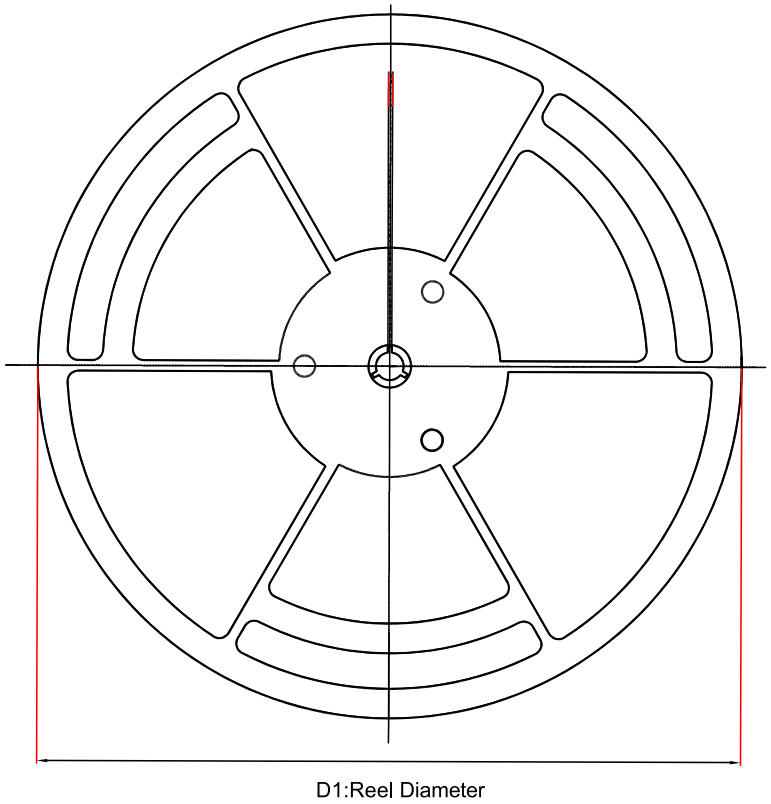
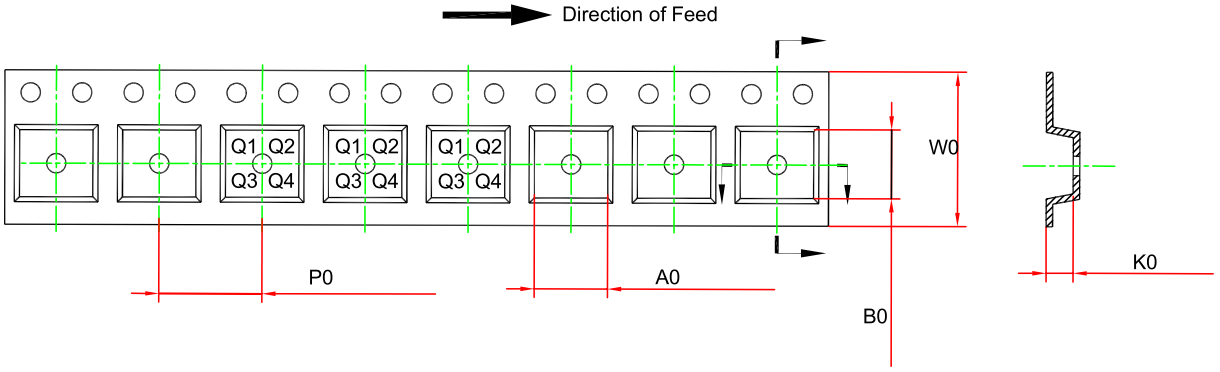


Figure 18. Typical Application Diagram

Tape and Reel Information



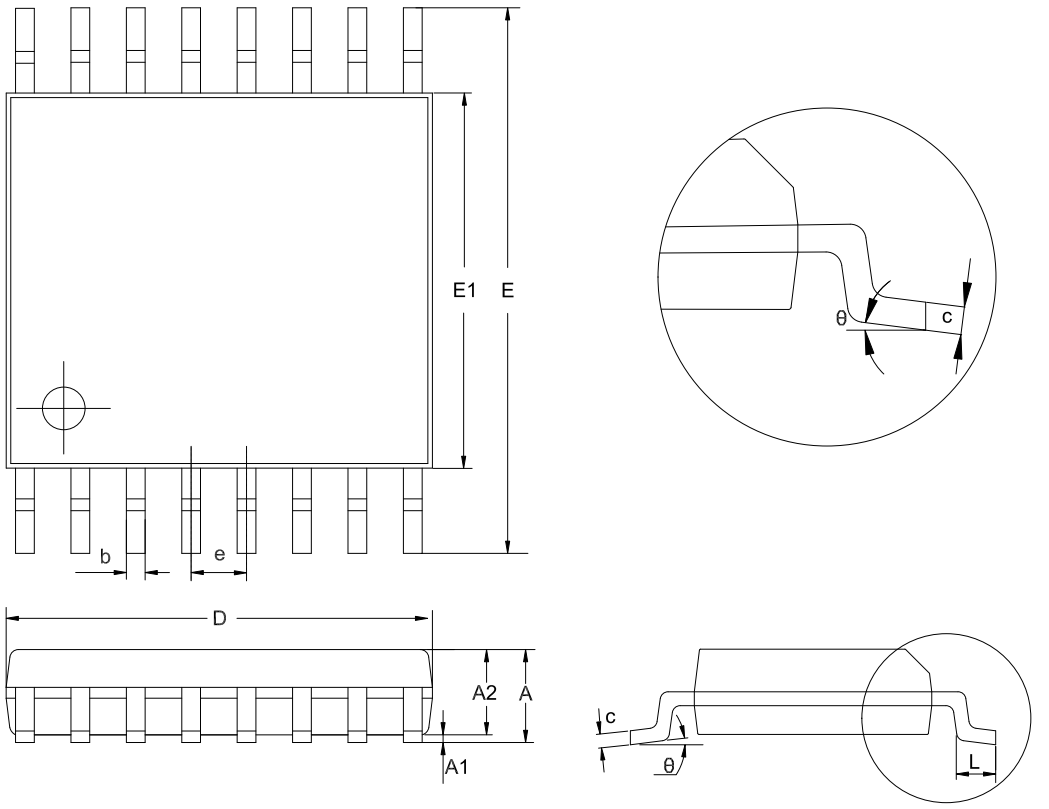


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC2182-TS3R	TSSOP16	330	17.6	6.8	5.5	1.5	8	12	Q1

Package Outline Dimensions

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC2182-TS3R	−40 to 125°C	TSSOP16	2182	3	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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