

N-Ch200V Fast Switching MOSFETs

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Product Summary

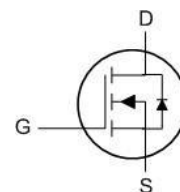
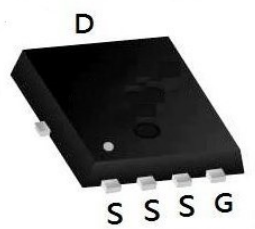


BVDSS	RDSON	ID
200V	82mΩ	30A

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

PDFN5060-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	200	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	30	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	17	A
I_{DM}	Pulsed Drain Current ²	63	A
EAS	Single Pulse Avalanche Energy ³	130	mJ
I_{AS}	Avalanche Current	36	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	51	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	56	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3.2	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	200	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	---	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=1A$	---	82	99	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	2.5	3.4	4.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=200V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=200V$, $V_{GS}=0V$, $T_J=100^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V$, $I_D=10A$	---	11	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	2.0	---	Ω
Q_g	Total Gate Charge	$V_{DS}=100V$, $V_{GS}=10V$, $I_D=10A$	---	6.5	---	nC
Q_{gs}	Gate-Source Charge		---	2.3	---	
Q_{gd}	Gate-Drain Charge		---	2.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V$, $V_{DD}=100V$, $R_G=2.7\Omega$, $I_D=10A$	---	3.9	---	ns
T_r	Rise Time		---	3.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	6.4	---	
T_f	Fall Time		---	4.5	---	
C_{iss}	Input Capacitance	$V_{DS}=100V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	380	---	pF
C_{oss}	Output Capacitance		---	64	---	
C_{rss}	Reverse Transfer Capacitance		---	9.4	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	30	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=60A$, $T_J=25^\circ\text{C}$	---	---	1.3	V
t_{rr}	Reverse Recovery Time	$I_F=10A$, $di/dt=100A/\mu s$	---	92	---	nS
Q_{rr}	Reverse Recovery Charge	μs , $T_J=25^\circ\text{C}$	---	287	---	nC

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$
2. The EAS data shows Max. rating . The test condition is $V_{DD}=100V$, $V_{GS}=10V$, $L=1\text{mH}$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Performance Characteristics

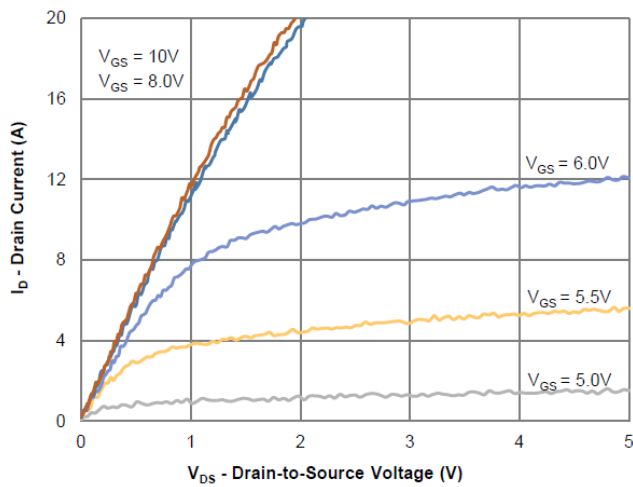


Figure 1: Output Characteristics

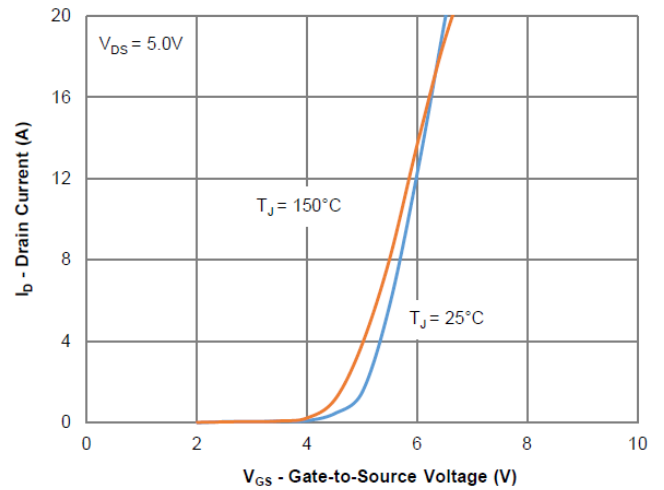


Figure 2: Transfer Characteristics

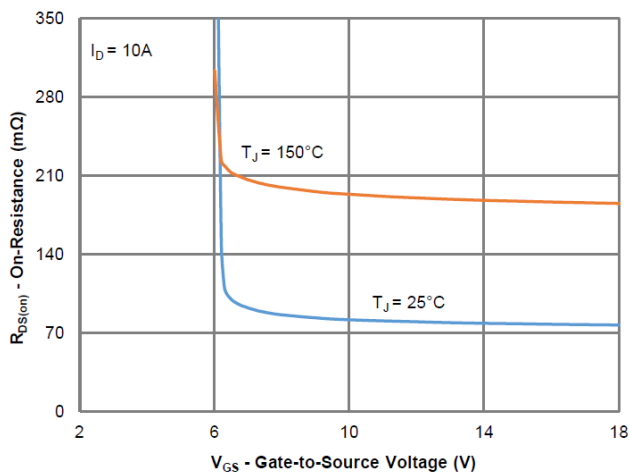


Figure 3: On-Resistance vs. Gate-Source Voltage

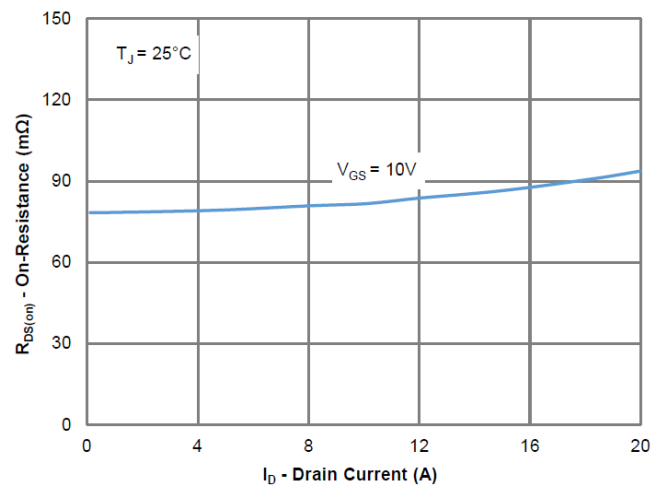


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

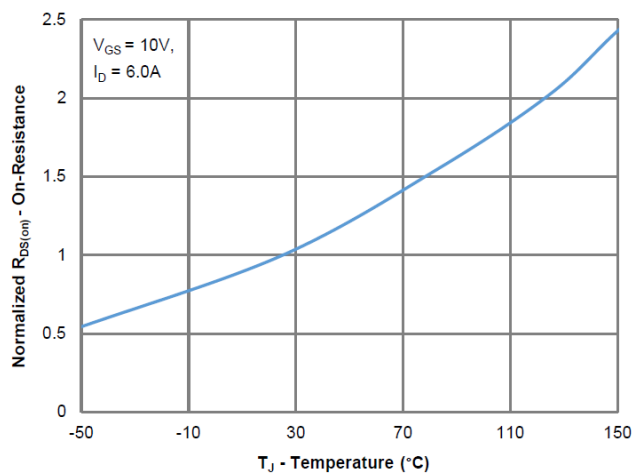


Figure 5: On-Resistance vs. Junction Temperature

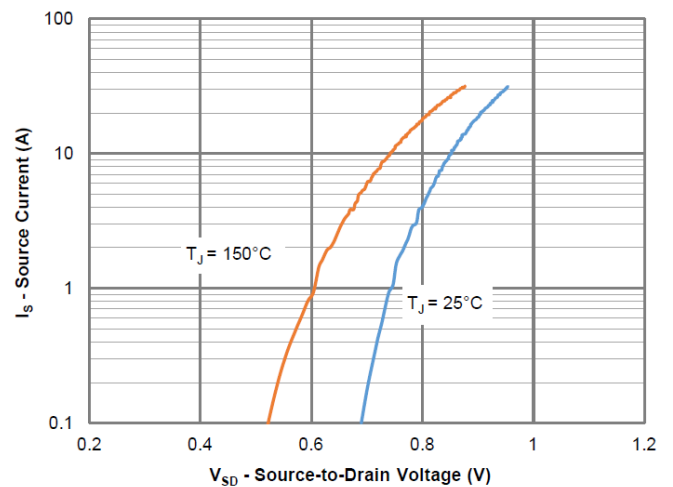


Figure 6: Source-Drain Diode Forward Voltage

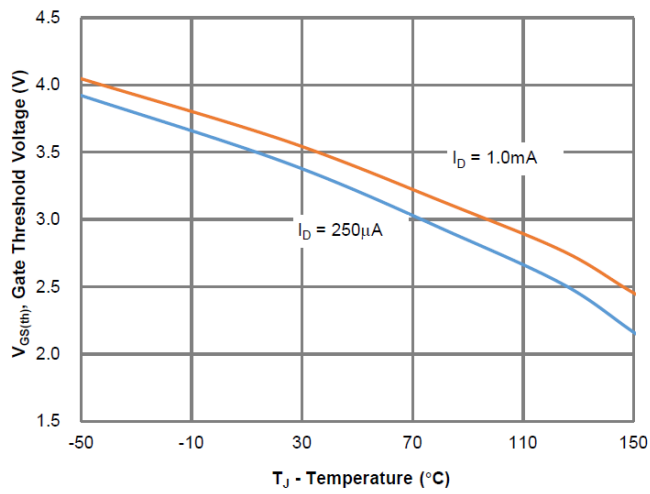


Figure 7: Gate Threshold Variation vs. Junction Temperature

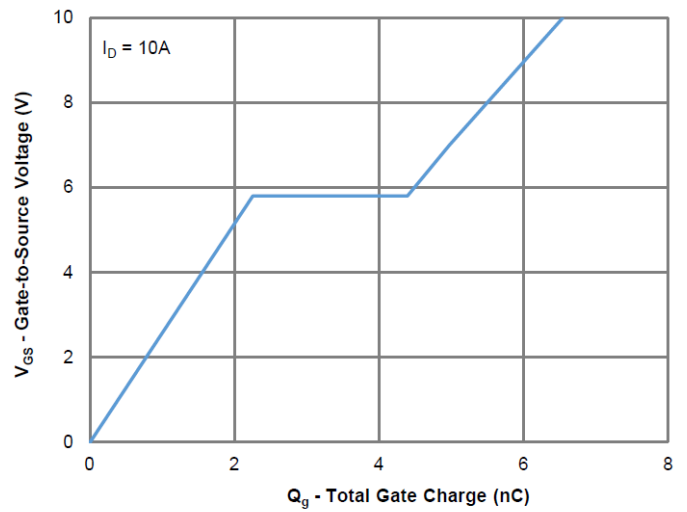


Figure 8: Gate Charge Characteristics

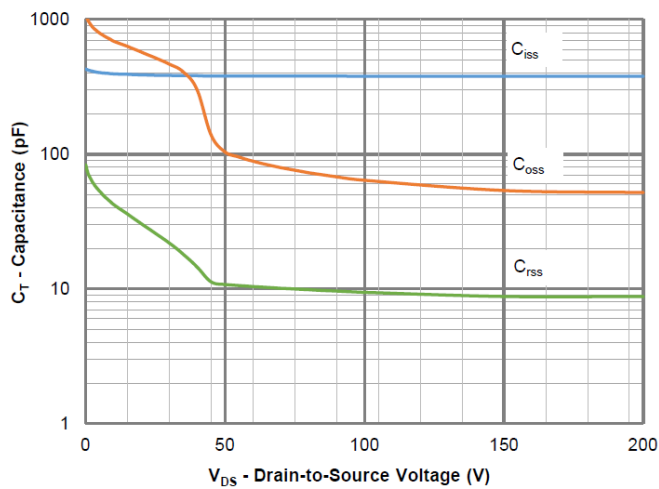


Figure 9: Capacitance Characteristics

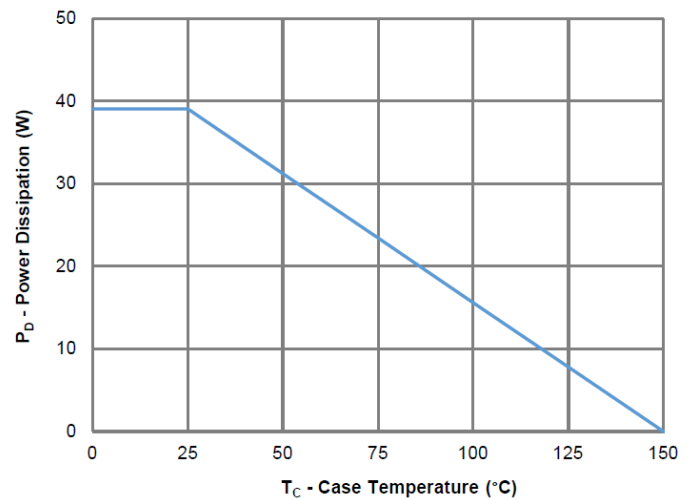


Figure 10: Power Derating

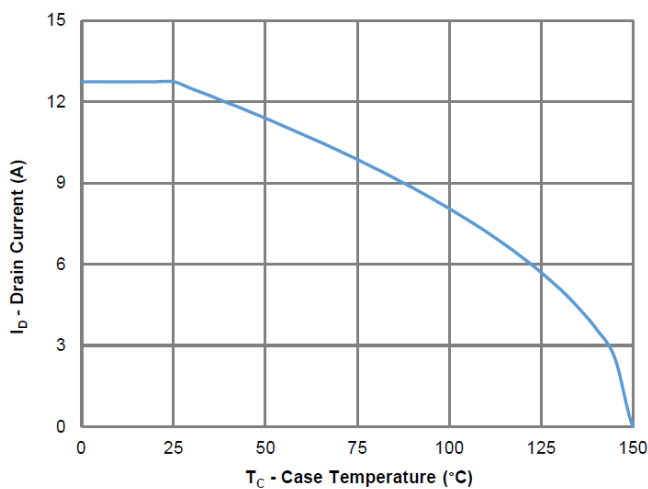


Figure 11: Current Derating

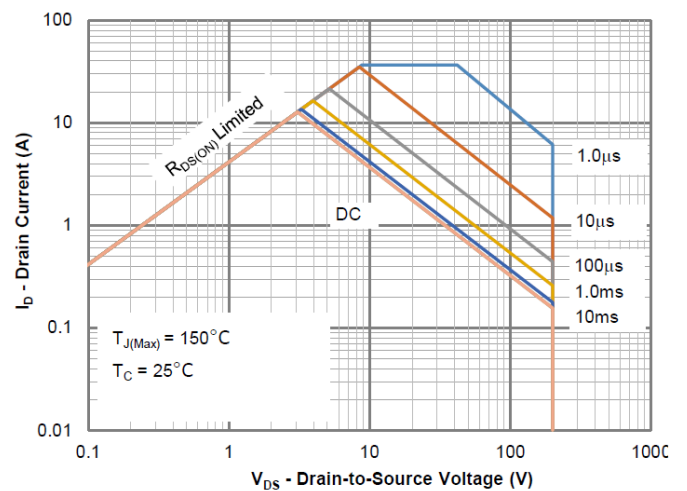


Figure 12: Safe Operating Area

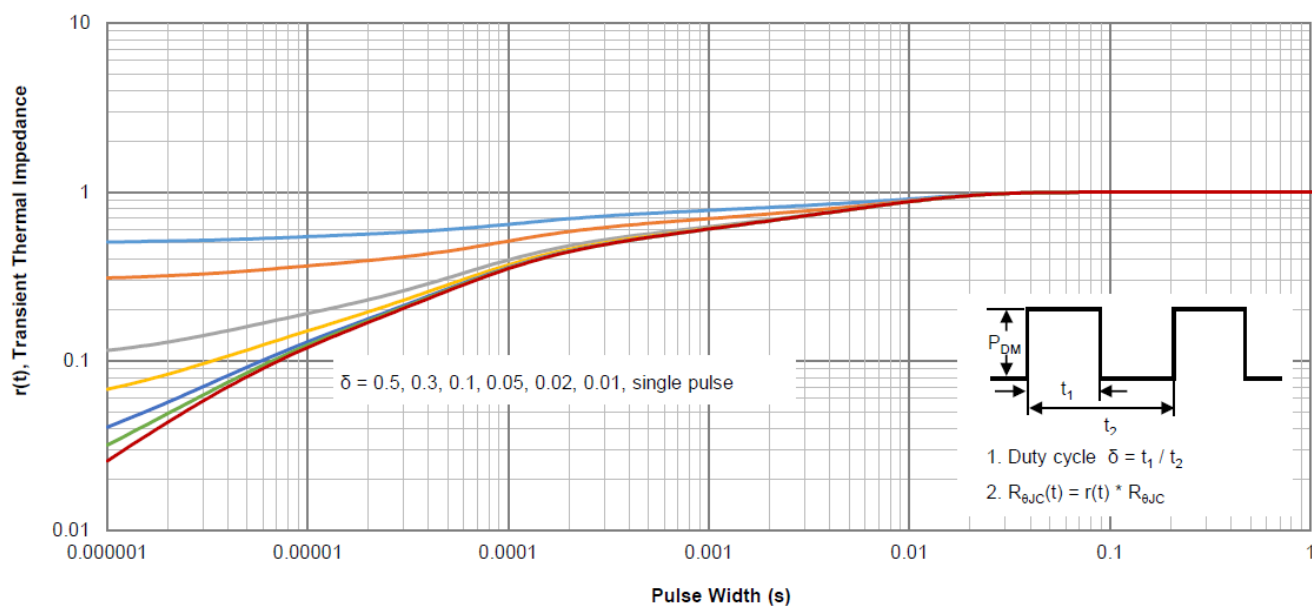
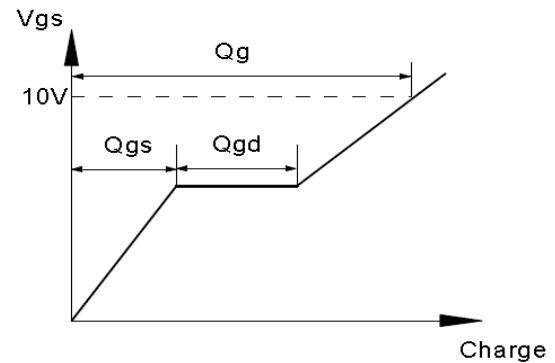
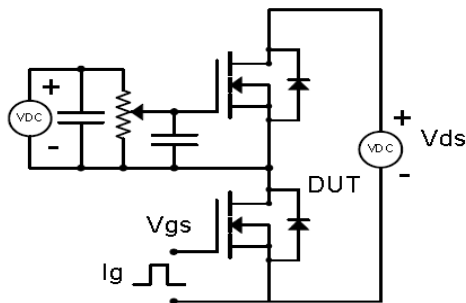


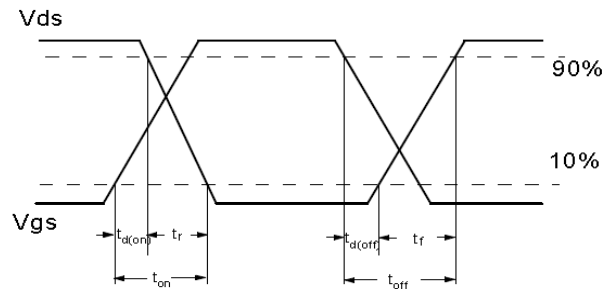
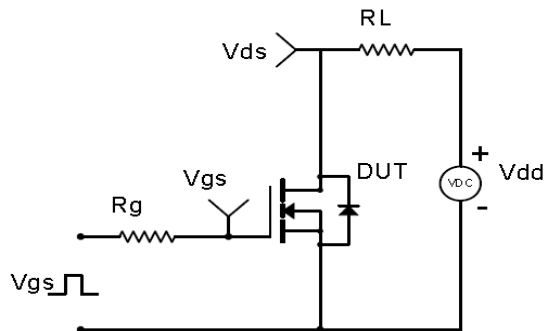
Figure 13: Normalized Maximum Transient Thermal Impedance

Test Circuit & Waveform

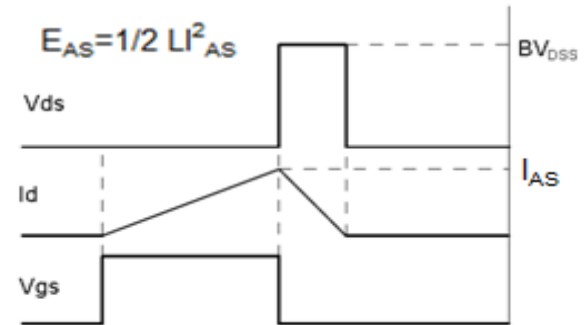
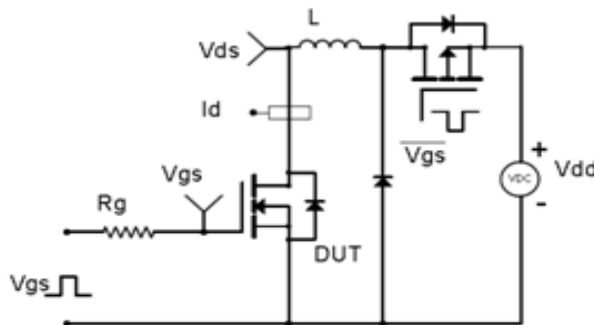
Gate Charge Test Circuit & Waveform



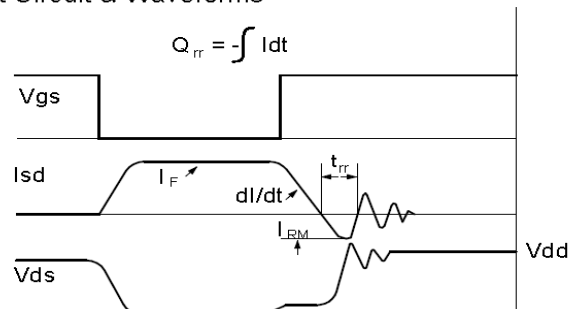
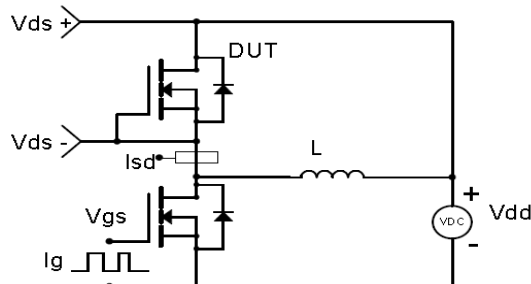
Resistive Switching Test Circuit & Waveforms



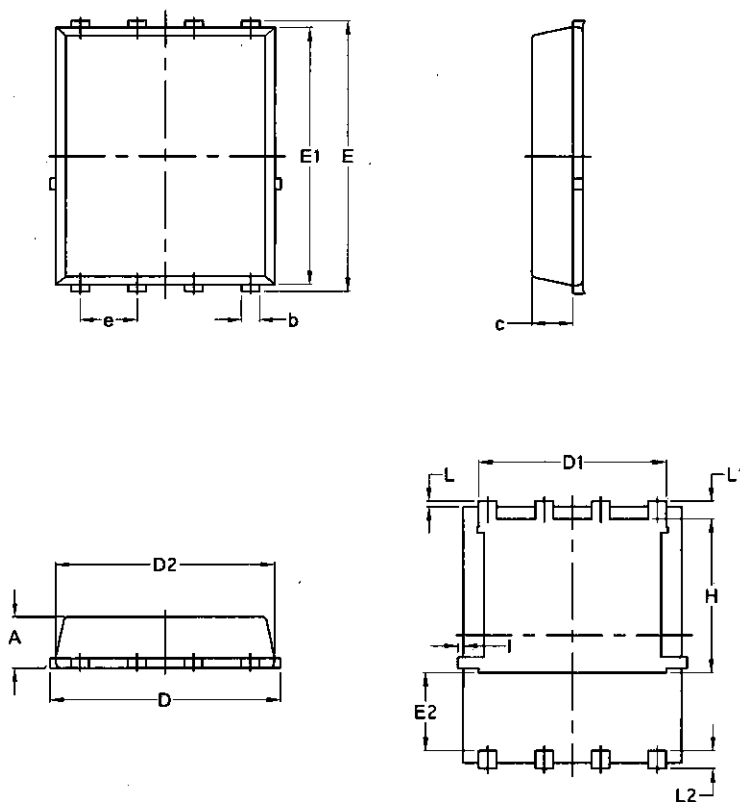
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-PDFN5060-8L-Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070