FE1.1

USB 2.0 High Speed 4-Port Hub Controller

Data Sheet

Introduction

Terminus FE1.1 is a highly integrated, high-quality, high-performance, low power consumption, yet low-cost USB 2.0 High Speed 4-Port Hub solution.

FE1.1 adopts Multiple Transaction Translator (MTT) architecture to explore the maximum possible throughput. Six non-periodic transaction buffers, instead of two, are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no microcontroller is used in this chip.

To guarantee high quality, the whole chip is covered by the *Test Scan Chain* – even on the high-speed (480MHz) modules, so that all the logic components can be fully tested before shipping. A Special Built-in Self-Test Mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components on the packaging and testing stages as well.

Low power consumption is achieved by using 0.18μm technology and comprehensive power/clock control mechanism. Most parts of the chip will not be clocked unless needed.

Features

- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
  - Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes;
  - 4 Downstream Facing Ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resisters;
- Integrated 5V to 3.3V and Core power regulator.
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resister, and crystal load capacitance;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- *Multiple Transaction Translators* (MTT) –
  - One TT for each downstream port;
  - Alternate Interface 0 for Single-TT, and Alternate Interface 1 for Multiple-TT;
  - Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 non-periodic transactions;

- Automatic self-power status monitoring;
  - Automatic re-enumeration when Self-Powered switching to Bus-Powered;
- Board configured options (**48**-pin **P**ackage) –
  - *Ganged* or *Individual Power Control Mode* select;
  - *Global* or *Individual Over-Current Protection Mode* select;
  - *Removable or Non-Removable Downstream Devices* configuration;
- Comprehensive Port Indicators support (**48**-pin **P**ackage):
  - Standard downstream port status indicators (Green and Amber LED control for each downstream port);
  - Hub active LED support;

Order Information

P/N-Order Code	Description	Package Type	Packing	Minimum Order Quantity
FE1.1-AQFP48A	USB 2.0 4-Port MTT Hub Controller	48-pin LQFP (7mm x 7mm)	Tray	15000
FE1.1-AQFP48AT(Note)		48-pin LQFP (7mm x 7mm)	Tray	2500
FE1.1-AQFN48A		48-pin QFN (6mm x 6mm)	Tape & Reel	12500
FE1.1-AQFP48B		48-pin LQFP (7mm x 7mm)	Tray	15000
FE1.1-AQFN24A		24-pin QFN (4mm x 4mm)	Tape & Reel	15000
FE1.1-AQFN24AT(Note)		24-pin QFN (4mm x 4mm)	Tape & Reel	3000

Note: Product of order code AQFP48AT and AQFN24AT are final tested in Room Temperature, 85°C, and -40°C, respectively.

Block Diagram

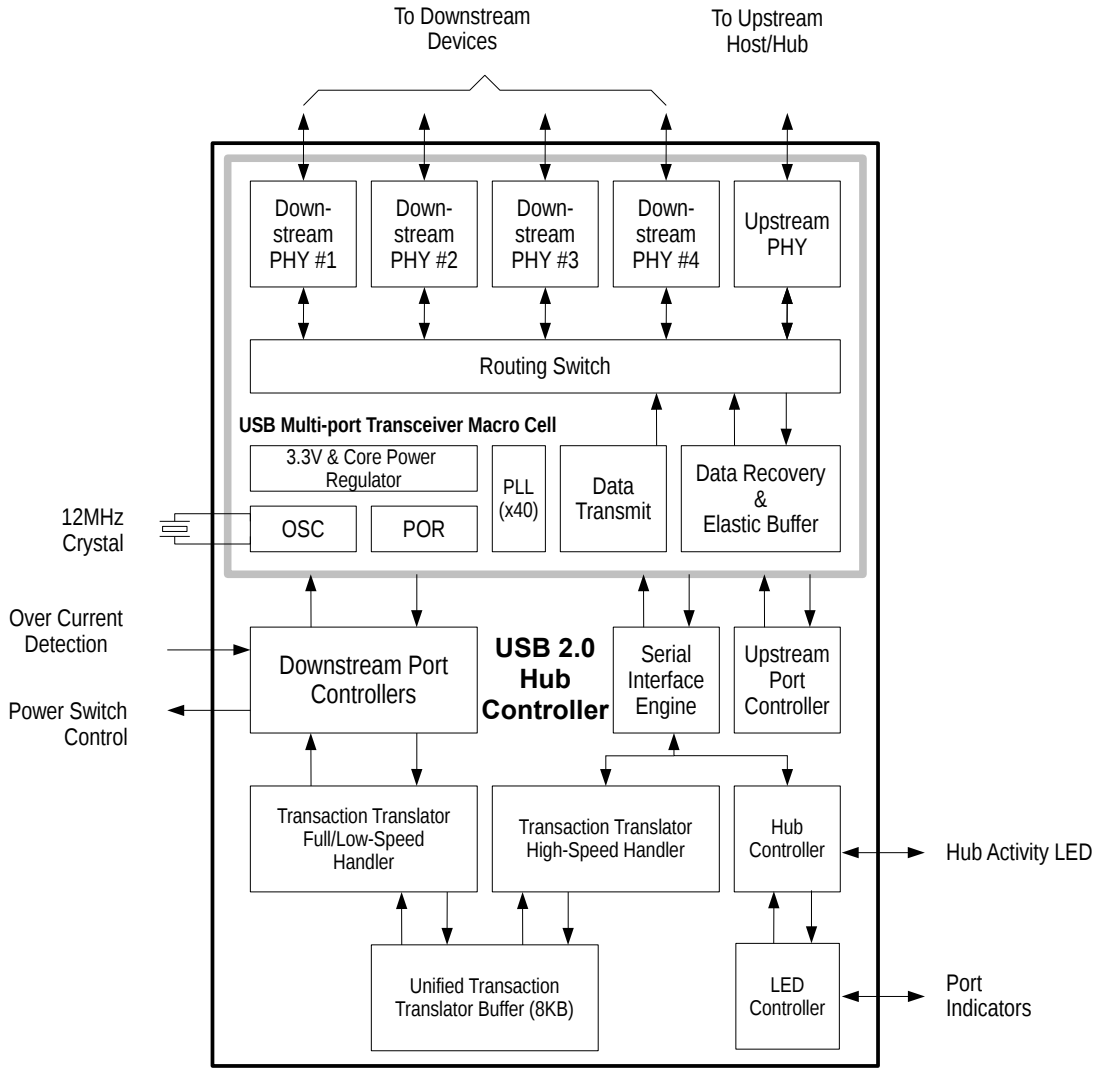


Fig. 1: Block Diagram

Package I – 48-pin LQFP
(Body Size: 7mm x 7mm)

Pin Assignment

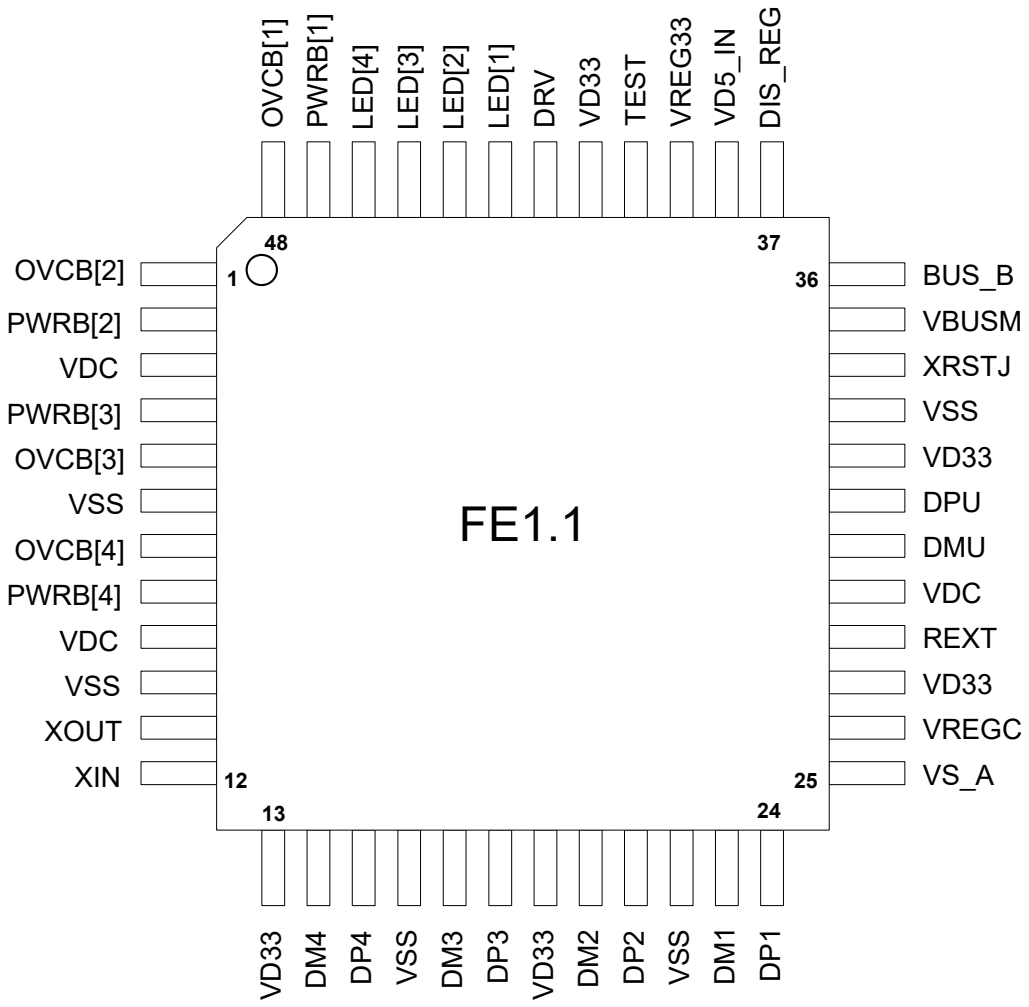


Fig. 2: 48-Pin LQFP Pin Assignment

PACKAGE II– 48-PIN QFN

(Body Size: 6mm x 6mm, 0.4pitch)
(Exposed Pad: 4.5mm x 4.5mm)

PIN ASSIGNMENT

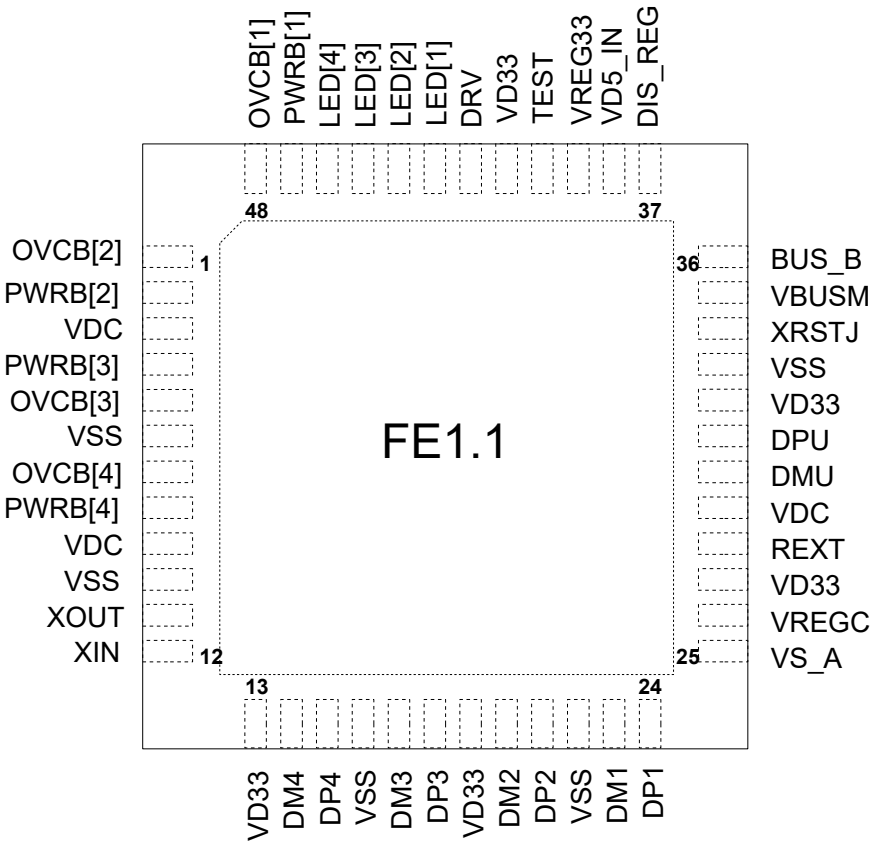


Fig. 3: 48-Pin QFN Pin Assignment

Package III– 24-pin QFN

(Body Size: 4mm x 4mm, 0.5pitch)
(Exposed Pad: 2.5mm x 2.5mm)

Pin Assignment

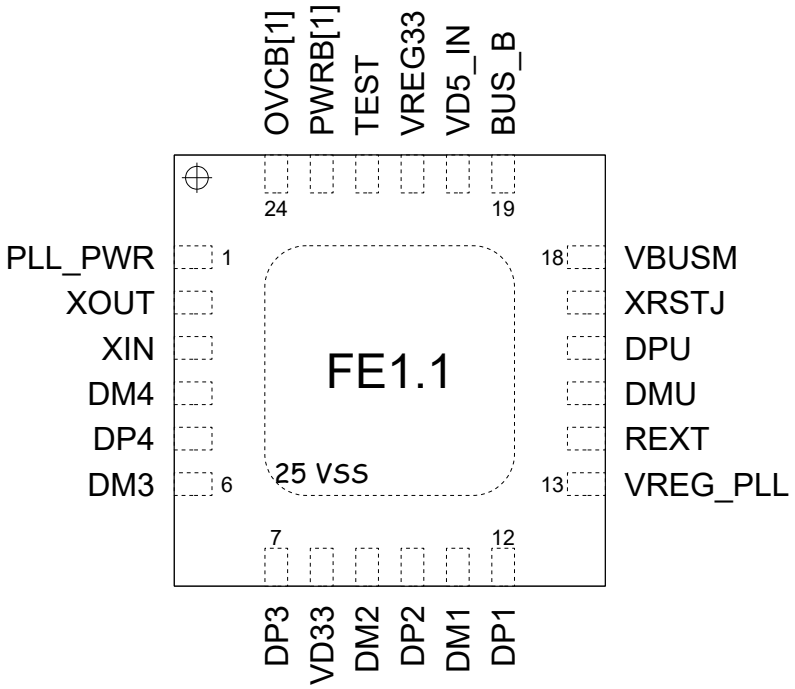


Fig. 4: 24-Pin QFN Pin Assignment

Pin Description Table

Pin Name	Pin No.		Type	Function	Note
	48-pin	**24**-pin			
OVCB[1]	48	24	I	Over Current Indicators – active low, for each corresponding downstream facing port. 1) When *Global Over-Current Protection Mode* is selected with PWRB[4] tied to ground, only OVCB[1] is functional, and all the other pins (OVCB[4:2]) should be tied to ground. OVCB[1] pin must be pulled high if it is not used. 2) When using *Individual Port Over-Current Protection Mode*, all OVCB[4:1] are functional. All OVCB[4:1] pins must be pulled high if it is not used. Reminder: **24**-pin **P**ackage only supports *Global Over-Current Protection Mode*.	1
OVCB[2]	1	–			
OVCB[3]	5				
OVCB[4]	7				
PWRB[1]	47	–	O	Downstream Device Power Enable – active low, for each corresponding downstream device. When *Ganged Power Switching Mode* is selected, with PWRB[4] tied to ground, only PWRB[1] is used. Reminder: **24**-pin **P**ackage only supports *Global Over-Current Protection Mode*, and PWRB[1] is open-drain output signal.	1
	–	23	OD		
PWRB[2]	2	–	O		
PWRB[3]	4				
PWRB[4]	8	–	I/O	When this pin is tied to ground, the *Global Over-Current Protection* and *Ganged Power Control Modes* are selected. In these modes, only OVCB[1] and PWRB[1] are effective. Otherwise, it is Downstream Device Power Enable, active low, for the 4th Downstream Facing Port.	1
PLL_PWR	–	1	P	Power for PLL.	3
VDC	3, 9, 29	–	P	Core Power.	3
XOUT	11	2	OSC	12 MHz Crystal Oscillator output	4
XIN	12	3	OSC	12 MHz Crystal Oscillator input.	4
VD33	13, 19, 27, 32, 41	8	P	3.3V Power.	3
DM4	14	4	UT	The D- pin for the 4th Downstream Facing Port.	
DP4	15	5	UT	The D+ pin for the 4th Downstream Facing Port.	
VSS	6, 10, 16, 22, 33	25	P	Ground.	
DM3	17	6	UT	The D- pin for the 3rd Downstream Facing Port.	
DP3	18	7	UT	The D+ pin for the 3rd Downstream Facing Port.	
DM2	20	9	UT	The D- pin for the 2nd Downstream Facing Port.	

DP2	21	10	UT	The D+ pin for the 2nd Downstream Facing Port.	
DM1	23	11	UT	The D- pin for the 1st Downstream Facing Port.	
DP1	24	12	UT	The D+ pin for the 1st Downstream Facing Port.	
VS_A	25	—	P	Analog Ground.	
VREG_PLL	—	13	P	PLL power regulator – always be connected to PLL_PWR, 1µF decoupling ceramic capacitor required.	3
VREGC	26	—	P	Core Power regulator output – a 10µF output ceramic capacitor is required. For internal use only.	3
REXT	28	14		A 2.7KΩ (± 1%) resister should be connected to VS_A to provide internal bias reference.	
DMU	30	15	UT	The D- pin of the Upstream Facing Port.	
DPU	31	16	UT	The D+ pin of the Upstream Facing Port.	
XRSTJ	34	17	I	External Reset – active low, it is an optional source of chip reset signal besides the built-in Power-On-Reset. The minimum low pulse width is 10µs.	
VBUSM	35	18	I	The V_{BUS} Monitor of Upstream Facing Port.	
BUS_B	36	19	I	Bus power indicator – active low when no local power presented.	
DIS_REG	37	—	I	Disable Built-in 5V→3.3V Regulator – tie to 3.3V to disable the embedded 5V→3.3V regulator.	
VD5_IN	38	20	P	5V power input for integrated 5V→3.3V regulator.	3
VREG33	39	21	P	5V→3.3V regulator output – a 10µF output ceramic capacitor is required. For internal use only.	3
TEST	40	22	I	Test Mode Enable should be tied to ground for normal operation.	
DRV	42	—	I/O	LED Drive Control – when tied to ground, the support of PORT_INDICATOR (LED) is disabled; otherwise, together with LED[4:1], it controls the illumination of LEDs.	2
LED[1]	43	—	I/O	Port Indicator (LED) Control – one pin for each downstream port. If the pin is tied to ground, it indicates that the device attached to the corresponding port is a *Non-Removable* device and no LED is supported. If connected to the Green and Amber LEDs, the pin controls their illumination according to the Hub Class Specification.	2
LED[2]	44				
LED[3]	45				
LED[4]	46				

Type Abbreviation –

I : Input; O : Output; OD: Output, Open Drain; I/O : Input/Output; P : Power/Ground; UT: USB Transceiver.

Note 1 – Power Control Switch And Over-Current Protection Configuration

Both the *Power Control Mode* and *Over-Current Protection Mode* are configured by the PWRB[4] pin. To select *Ganged Power Control Mode* and *Global Over-Current Protection Mode*, the PWRB[4] should be tied to ground, as shown in the left part of *Figure 5*. In this case, the over-current indicator is sampled by OVCB[1] and the power switch for downstream ports is controlled by PWRB[1]. The rest of the OVCB (4 to 2) must be tied to ground and PWRB[3], PWRB [2] be left unconnected.

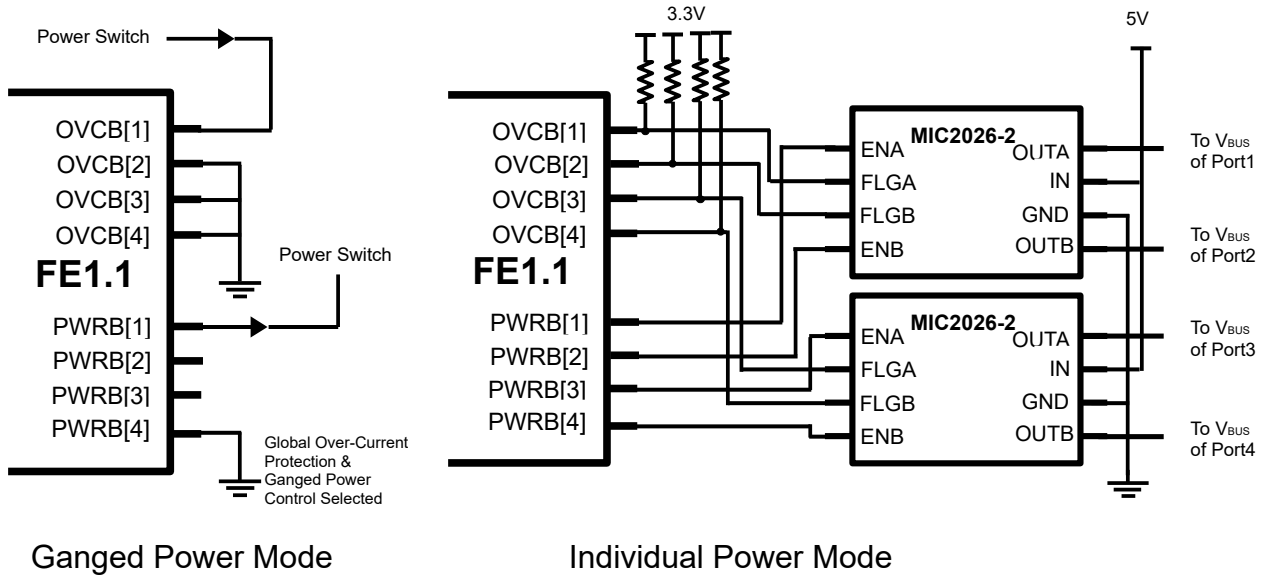


Fig. 5: Power Control & Over-Current Protection Configuration

For more delicate power management of downstream devices, *Individual Power Control Mode* and *Individual Over-Current Protection Mode* can be implemented. As depicted in the right part of *Figure 5*, two Dual-Channel Power Distribution Switch with current sensing and limiting capability are used. In this configuration, FE1.1 will automatically recognize that the *Individual Mode* is selected and report to the host in the Hub Descriptor Table.

Note 2 – LED Configuration

Port Indicators – one Green LED and one Amber LED for each downstream port – are optional and can be configured by the DRV pin. If the LEDs are not required, the DRV pin should be tied to ground to disable this feature, as illustrated in the left part of *Figure 6*. The LED[*n*] pins could either be left unconnected to denote removable downstream devices or tied to ground to identify that the corresponding port is attached to a Non-Removable device, as shown in port 4.

To fully support PORT_INDICATOR as defined in USB Specification Rev. 2.0, the LEDs should be connected according to the right part of *Figure 6*. It is important that the directions of all the LEDs must be connected as shown. Otherwise, the Green/Amber lights will not function as defined in the USB 2.0 specifications. The maximum load current of each LED is 3mA. The LED[*n*] pin can also be tied to ground to indicate that the device attached to port *n* is a Non-Removable device. In this case, no LED should be connected to that pin, as demonstrated by port 4.

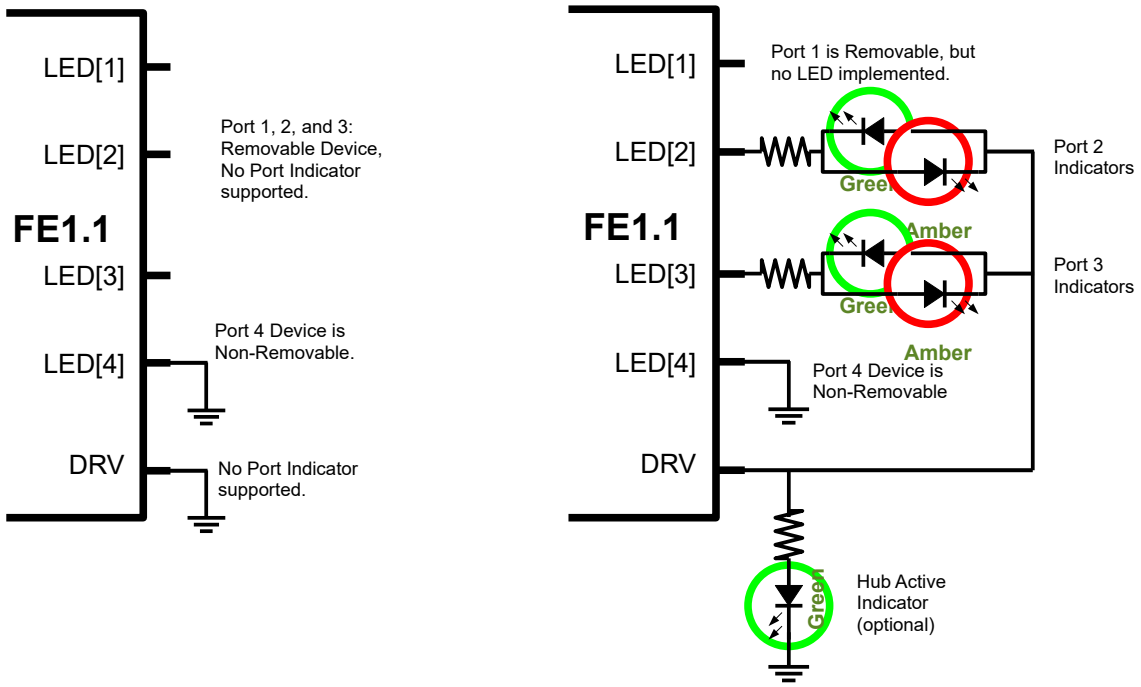


Fig. 6: Port Indicators And Removable Device Configurations

An optional *Hub Active* LED can be implemented between DRV pin and ground. This light will turn on whenever the hub is configured by the host drive or wakes up from suspend mode. It will turn off whenever the hub is unconfigured by the host or switches into suspend mode.

The LED[1] in the right part of *Figure 6* demonstrates that the LED can be omitted without affecting the normal function. That is, the host will still identify the device at the corresponding port, the *Hub Active* LED will illuminate as normal, and port 1 will not be considered Non-Removable.

Note 3 – Power Source

The power source for FE1.1 could be either fed in from VD5_IN or VD33, but not both. The core power (VDC) of FE1.1 must be served by the built-in 3.3V-to-core-power regulator to maintain the performance of its Phase Lock Loop (PLL).

Using 5V power source, the power is fed in VD5_IN, passed through the 5V-to-3.3V regulator, and outputs 3.3V to VREG33. The output capability of VREG33 is designed for FE1.1 use only. No other device should source its power from this pin. VREG33 should connect with a 10µF output ceramic capacitor, then to all the VD33 pins. VREGC is the output for 3.3V-to-core power regulator. With a 10µF output ceramic capacitor, it should connect to all VDC pins of FE1.1.

When 3.3V power source is selected, all VD33 pins of FE1.1 will be served by 3.3V source of the system. VREGC is the output for 3.3V-to-core power regulator. With a 10µF output ceramic capacitor, it should connect to all VDC pins of FE1.1.

It is highly recommended that FE1.1 use the same 3.3V power source as the other interconnected components when 3.3V power is available in the system. Under this scheme, both VD5_IN and VREG33 should be left unconnected.

In the case of QFN24, VREG_PLL is for supplying PLL power only, and with a 1µF decoupling ceramic capacitor, it should connect to PLL_PWR only. It is important that no other components are connected to this path for the sake of PLL performance.

Note 4 – Crystal Requirements

- Frequency accuracy: 12MHz ± 50ppm
- Load capacitance: 16pF ~ 20pF
- Equivalent Series Resistance: 50Ω Max.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-55	150	°C
5V Power Supply Voltage	VD5	0	+5.5	V
3.3V Power Supply Voltage	VD33	0	+3.6	V
ESD Human Body Mode		-2000	2000	V
ESD Charged Device Mode		-500	500	V
Latch Up		-200	200	mA

Note1: This is the rated value that MUST NOT be exceeded, even for a moment, to maintain life and reliability.
Note2: If power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off, clamp circuit is advised.

Recommended Operating Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	0		70	°C
Operating voltage (5V power supply)	VD5	4.5	5.0	5.5	V
Operating voltage (3.3V power supply)	VD33	3.0	3.3	3.6	V
Power Ramp Up (10% ~ 90%)	TRUP	0.2		10	ms
LOW level voltage of digital input	VIL	-0.3		0.8	V
HIGH level voltage of digital input	VIH	2.0		5.5	V
LOW level voltage of digital output@4mA	VOL			0.4	V
HIGH level voltage of digital output@4mA	VOH	2.4			V
XIN input capacitance	Cin		32		pF

Note1: Operating temperature TA is measured in still air.

Extended Operating Ranges

Product with order code of AQFP48AT and AQFN24AT are Final Tested (FT) at Room Temperature, 85°C, and -40°C.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	-40	25	85	°C

Note1: Operating temperature TA is measured in still air.

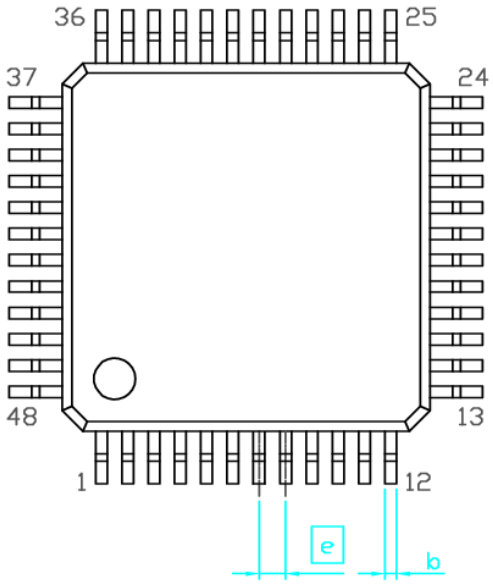
Power Consumption

DC Supply Current

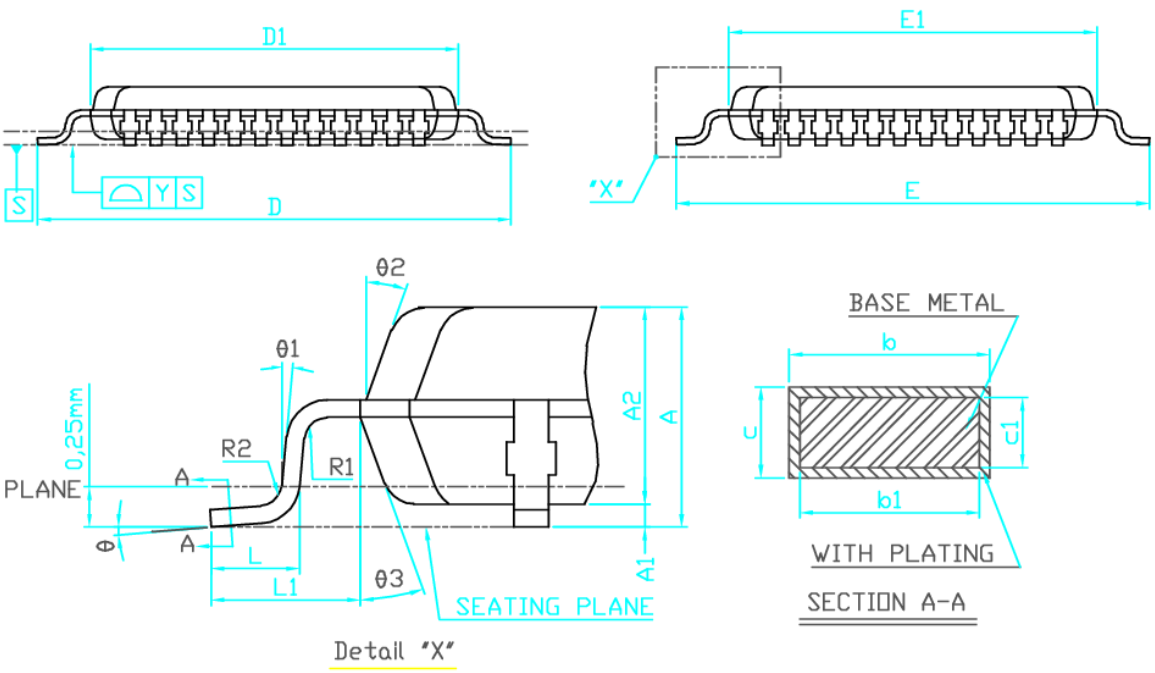
Symbol	Condition			Typical	Unit
	Active	Host	Devices		
I_suspend (**48**-pin **P**ackage)	Suspend			620	uA
I_suspend (**24**-pin **P**ackage)				850	uA
Icc	4	Full-Speed	4x Full-Speed	29	mA
		High-Speed	4x High-Speed	87	mA
		High-Speed	4x Full-Speed	43	mA
	3	Full-Speed	3x Full-Speed	29	mA
		High-Speed	3x High-Speed	76	mA
		High-Speed	3x Full-Speed	42	mA
	2	Full-Speed	2x Full-Speed	29	mA
		High-Speed	2x High-Speed	65	mA
		High-Speed	2x Full-Speed	42	mA
	1	Full-Speed	1x Full-Speed	29	mA
		High-Speed	1x High-Speed	53	mA
		High-Speed	1x Full-Speed	42	mA
	No active	Full-Speed	None	29	mA
		High-Speed	None	42	mA

Note: The power consumption is measured when the bus is in IDLE state – there are no activities other than the Start-Of-Frame (SOF) and INTERRUPT-IN packets for the hub itself on the bus. The peak power consumption varies depending on the system configuration, type of operations, and overall bus utilization.

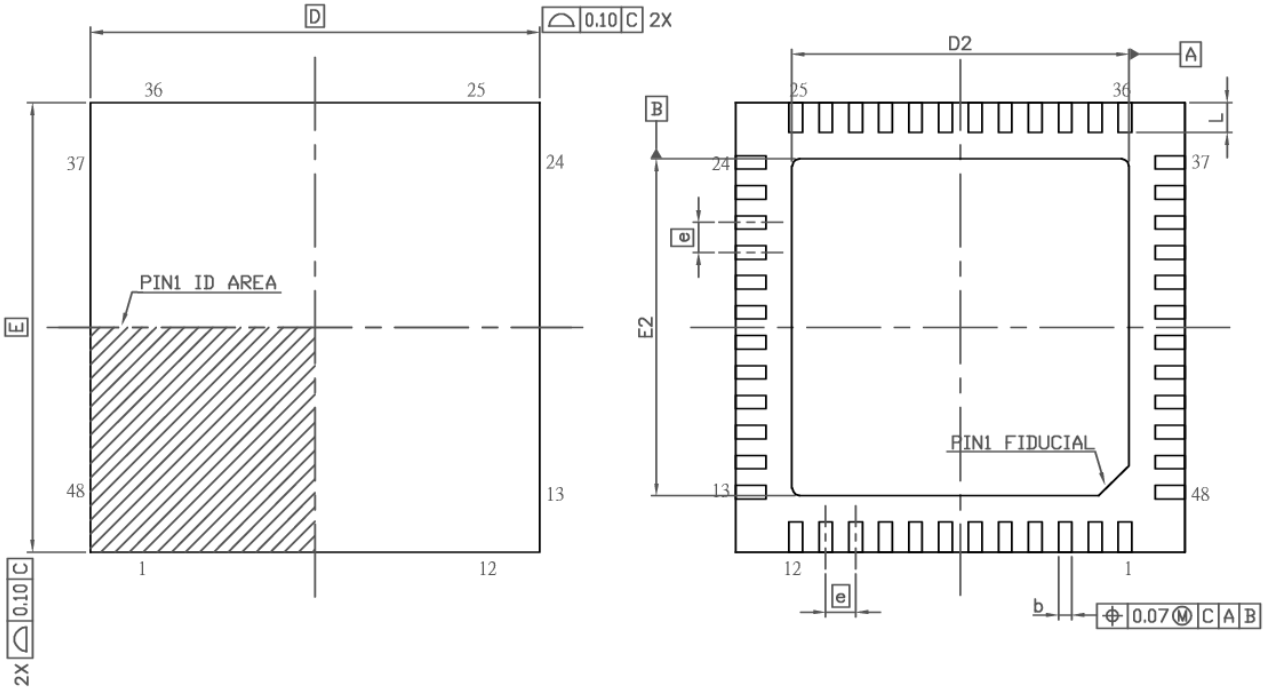
Package Drawing I – 48-pin LQFP

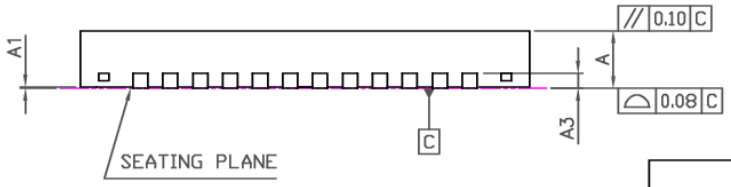


SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63.0
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	1.35	1.40	1.45	53.1	55.1	57.1
b	0.17	0.22	0.27	6.7	8.7	10.6
b1	0.17	0.20	0.23	6.7	7.9	9.1
c	0.09		0.20	3.5		7.9
c1	0.09		0.16	3.5		6.3
D	8.90	9.00	9.10	350.4	354.3	358.3
D1	6.90	7.00	7.10	271.7	275.6	279.5
E	8.90	9.00	9.10	350.4	354.3	358.3
E1	6.90	7.00	7.10	271.7	275.6	279.5
e	0.45	0.50	0.55	17.7	19.7	21.7
L	0.50	0.60	0.70	19.7	23.6	27.6
L1	0.85	1.00	1.15	33.5	39.4	45.3
R1	0.08			3.1		
R2	0.08		0.20	3.1		7.9
Y			0.08			3.1
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°



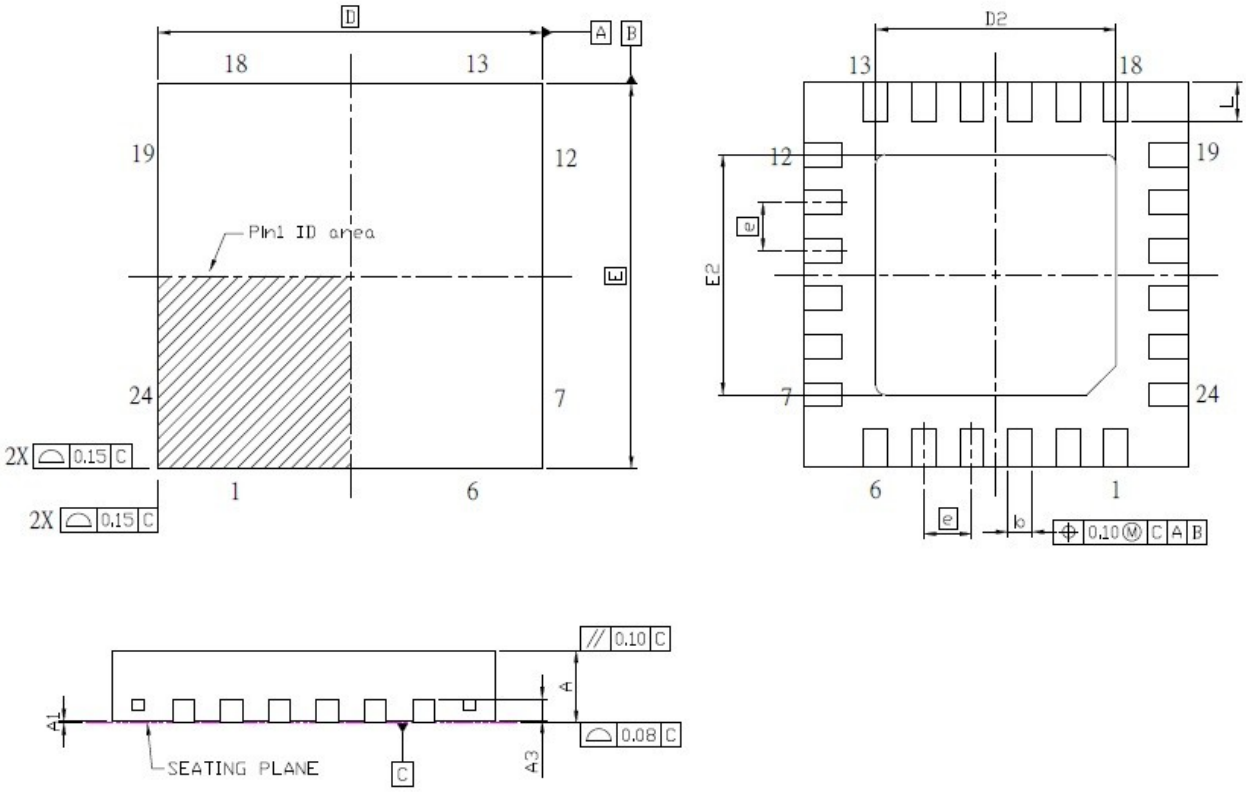
PACKAGE DRAWING II – 48-PIN QFN





SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	32
A1	0	0.02	0.05	0	0.8	2.0
A3	0.203 REF			8 REF		
b	0.15	0.20	0.25	6	8	10
D	5.90	6.00	6.10	232	236	240
D2	4.40	4.50	4.60	173	177	181
E	5.90	6.00	6.10	232	236	240
E2	4.40	4.50	4.60	173	177	181
e	0.40 BSC			16 REF		
L	0.30	0.40	0.50	12	16	20

PACKAGE DRAWING III – 24-PIN QFN



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.5	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8 REF		
b	0.18	0.25	0.30	7.1	9.8	11.8
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	2.40	2.50	2.60	94.5	98.4	102.4
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	2.40	2.50	2.60	94.5	98.4	102.4
e	0.50 BSC			19.7 BSC		
L	0.30	0.40	0.50	11.8	15.7	19.7

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