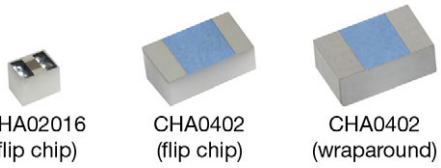
AEC-Q200 Qualified
High Frequency 70 GHz Thin Film Chip Resistor



CHA02016 (flip chip) | CHA0402 (flip chip) | CHA0402 (wraparound)

FEATURES

- Operating frequency 70 GHz
- AEC-Q200 qualified
- Thin film microwave resistors
- Ohmic range: 10 Ω to 500 Ω
- Design kits available
- Modelithics® library available
- Small internal reactance (LC down to 1 x 10^{-24})
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

LINKS TO ADDITIONAL RESOURCES

3D Models | S-Parameters | Simulation Tools | Application Notes | Capabilities and Custom Options | Did You Know? | Infographics | Why It Matters

Those miniaturized components are designed in such a way that their internal reactance is very small. When correctly mounted and utilized, they function as almost pure resistors on a very large range of frequency, DC to 50 GHz for CHA0402, and DC to 70 GHz for CHA02016 from 10 Ω to 500 Ω.

STANDARD ELECTRICAL SPECIFICATIONS

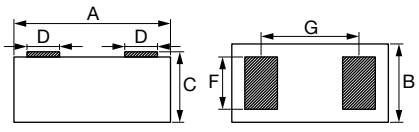
MODEL	SIZE	RESISTANCE RANGE Ω	RATED POWER Pn (1) W	LIMITING ELEMENT VOLTAGE V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
CHA02016	02016	10 to < 50	0.100	30	5	100 (50 upon request)
CHA02016	02016	50 to ≤ 500	0.100	30	2, 5	100 (50 upon request)
CHA02016	02016	50 and 100	0.100	30	1, 2, 5	100 (50 upon request)
CHA0402	0402	10 to < 50	0.300	37	2, 5	100 (50 upon request)
CHA0402	0402	50 to ≤ 500	0.300	37	1, 2, 5	100 (50 upon request)

Note

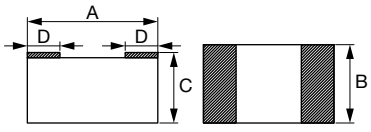
(1) PCB mounting with +70 °C ambient temperature

DIMENSIONS in millimeters (inches)

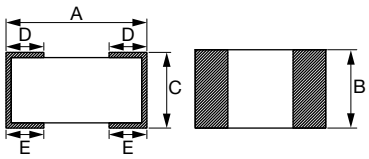
CHA02016 F / CHA02016 P



CHA0402 F

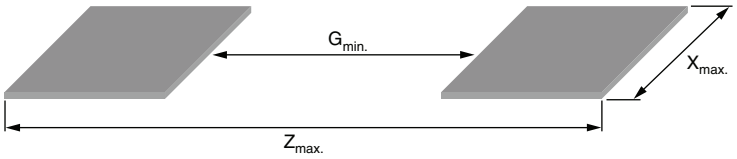


CHA0402 N



CASE SIZE / MODEL / TERMINATION	DIMENSIONS						
	A ± 0.10 (± 0.004)	B ± 0.10 (± 0.004)	C ± 0.127 (± 0.005)	D E when applicable MIN.	D E when applicable MAX.	F ± 0.050 (± 0.002)	G ± 0.050 (± 0.002)
CHA02016 F CHA02016 P CHA02016 M	0.480 (0.020)	0.390 (0.016)	0.420 (0.016)	0.110 (0.004)	0.150 (0.006)	0.260 (0.010)	0.300 (0.012)
CHA0402 F CHA0402 N	1.000 (0.040)	0.600 (0.023)	0.500 (0.020)	0.150 (0.006)	0.350 (0.014)	n/a	n/a

LAND PATTERN FOR F AND P "FLIP CHIP" TERMINATIONS in millimeters (inches)

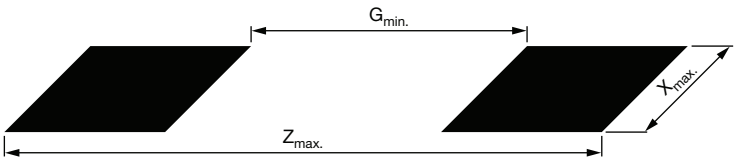


CHIP SIZE	$Z_{max.}$	$X_{max.}$	$G_{min.}$
02016	0.53 (0.021)	0.44 (0.017)	0.15 (0.006)
0402	1.40 (0.055)	0.65 (0.026)	0.40 (0.016)

Note

- Suggested land pattern: according to IPC-7351

LAND PATTERN FOR N WRAPAROUND TERMINATIONS in millimeters (inches)



CHIP SIZE	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0402	1.55 (0.061)	0.15 (0.006)	0.73 (0.029)

Dimension and tolerance of land pattern shall be defined by PCB designer; PCB can be designed according to IPC-7351A "Generic Requirements for Surface Mount Design and Land Pattern Standard"

PERFORMANCE (CHA02016 F/P TERMINATIONS)

TEST PROCEDURES AND REQUIREMENTS

AEC-Q200 CLAUSE	TEST	PROCEDURE	GLOBAL PERFORMANCES	TYPICAL PERFORMANCES (25 Ω TO 250 Ω)
3	High temperature exposure	MIL-STD-202 method 108 1000 h at T = 125 °C, unpowered	± 2 % ± 0.05 Ω	± 0.2 % ± 0.05 Ω
4	Temperature cycling	JESD22 method JA-104 1000 cycles (-55 °C to +155 °C)	± 1.8 % ± 0.05 Ω	± 1.5 % ± 0.05 Ω
7	Biased humidity	MIL-STD-202 method 103 1000 h 85 °C / 85 % RH 10 % of operating power	± 2 % ± 0.05 Ω	± 0.75 % ± 0.05 Ω
8	Operational life	MIL-STD-202 method 108 condition D steady state T = 125 °C at rated power 90' ON / 30' OFF / 1000 h	± 2.5 % ± 0.05 Ω	± 1 % ± 0.05 Ω
13	Mechanical shock	MIL-STD-202 method 213 condition C 100 *g*/6 ms 3.75 m/s 3 shock/direction, 2 directions along 3 axes (18 shocks)	± 0.05 % ± 0.05 Ω	± 0.015 % ± 0.05 Ω
14	Vibration	MIL-STD-202 method 204 5 *g* for 20 min, 12 cycles each of 3 orientations Test from 10 Hz to 2000 Hz	± 0.1 % ± 0.05 Ω	± 0.05 % ± 0.05 Ω
15	Resistance to soldering heat	MIL-STD-202 method 210 condition D Flux used: alpha 611 Solder temp.: 260 °C ± 5 °C Total immersion during 10 s	± 2.5 % ± 0.05 Ω	± 0.5 % ± 0.05 Ω

TEST PROCEDURES AND REQUIREMENTS				
AEC-Q200 CLAUSE	**TEST**	**PROCEDURE**	**GLOBAL PERFORMANCES**	**TYPICAL PERFORMANCES (25 Ω TO 250 Ω)**
17	ESD	AEC-Q200-002	Classification 1C 1000 V_{DC} to 2000 V_{DC}	
18	Solderability	J-STD-002 - Preconditioning 4 h dry heat aging and 235 °C SnPb 5 s - 215 °C SnPb 5 s - 260 °C SnAgCu 10 s	Good tinning (≥ 95 % covered) No visible damage	
20	Flammability	UL 94	Class V-0 No burning	
21	Board flex	AEC-Q200-005	± 0.1 % ± 0.05 Ω	± 0.05 % ± 0.05 Ω
24	Flame retardance	AEC-Q200-001	No flame, no explosion, no temperature higher than 350 °C	

Note

- Performance according to Rev. E of AEC-Q200

PERFORMANCES (CHA0402 F/N TERMINATIONS)

TEST PROCEDURES AND REQUIREMENTS			
AEC-Q200 CLAUSE	**TEST**	**PROCEDURE**	**GLOBAL PERFORMANCES**
3	High temperature exposure	MIL-STD-202 method 108 1000 h at T = 125 °C. Unpowered - measurement at 24 h ± 2 h after test conclusion	± 0.3 % ± 0.05 Ω
4	Temperature cycling	JESD22 method JA-104 1000 cycles (-55 °C to +155 °C)	± 0.3 % ± 0.05 Ω
7	Biased humidity	MIL-STD-202 method 103 1000 h 85 °C / 85 % RH 10 % of operating power. Measurement at 24 h ± 2 h after test conclusion	± 0.55 % ± 0.05 Ω
8	Operational life	MIL-STD-202 method 108 1000 h - power 90 min ON/30 min OFF - 100 % of rated power at 70 °C Measurement at 24 h ± 2 h after test conclusion	± 0.03 % ± 0.05 Ω
13	Mechanical shock	MIL-STD-202 method 213 Figure 1 of method 213. Condition C 100 *g* /6 ms 3.75 m/s 3 shock/direction, 2 directions along 3 axes (18 shocks)	± 0.05 % ± 0.05 Ω
14	Vibration	MIL-STD-202 method 204 5 *g* for 20 min, 12 cycles each of 3 orientations Test from 10 Hz to 2000 Hz	± 0.01 % ± 0.05 Ω
15	Resistance to soldering heat	MIL-STD-202 method 210 Condition K time above 217 °C, 60 s to 150 s	± 0.25 % ± 0.05 Ω
17	ESD	AEC-Q200-002	Classification 1C 1000 V_{DC} to 2000 V_{DC}
18	Solderability	J-STD-002 method B1	Good tinning (≥ 95 % covered) No visible damage
20	Flammability	UL 94 class V-0	Class V-0 no burning
21	Board flex	AEC-Q200-005	± 0.15 % ± 0.05 Ω
24	Flame retardance	AEC-Q200-001	No flame, no explosion, no temperature higher than 350 °C

Note

- Performance according to Rev. E of AEC-Q200

PREFERRED MODELS AND VALUES

Minimum order quantity for waffle pack:

400

Minimum order quantity for tape and reel:

1000

Recommended termination:

F

Recommended tolerance:

2 %

DESIGN KITS

Design kits are available ex stock in CH02016 and CH0402 equivalents: https://www.vishay.com/doc?53014 - Page 5.

There are 20 pieces per recommended value. F termination. 5 % tolerance.

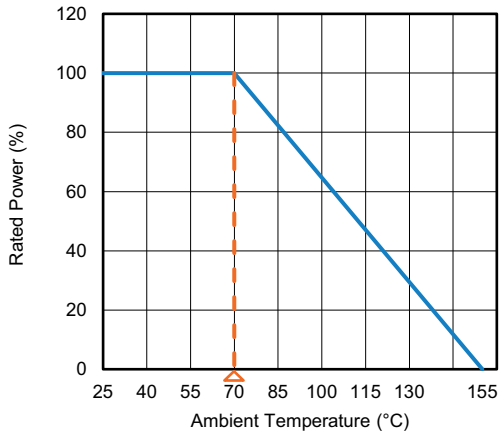
Those kits are packaged in pieces of tape and delivered in ESD bags.

TEST BOARDS

TRL (Thru Reflect Line) and DUT (Device Under Test) evaluation boards (50 Ω or 100 Ω) are available on request.

THERMAL SPECIFICATIONS (CHA0402)

POWER DERATING CURVE



PCB MOUNTING	
CHIP SIZE	RATED POWER (1) (W)
0402	0.300

Note

(1) PCB mounting with +70 °C ambient temperature.
PCB is FR4 base material 100 mm x 150 mm x 1.5 mm, 35 µm Cu-layer

SUGGESTIONS TO INCREASE POWER

PCB MOUNTING AMBIENT +25 °C			
CHIP SIZE	POWER (W)		
	FR4 (1)	ALUMINA (2)	AIN (2)
0402	0.450	1.000	1.200

Notes

(1) Thermal measurement with Optris Xi 400 camera. Test performed with standard FR4 (PCB thickness 1.6 mm, copper thickness 35 µm)

(2) Estimations with PCB thermal resistance knowledge

BACKSIDE CHIP TEMPERATURE +25 °C	
CHIP SIZE	POWER (1) (W)
0402	2.000

Note

(1) Estimations with components thermal resistance knowledge

PACKAGING

Standard packaging is plastic tape and reel for all sizes.

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
		WAFFLE PACK 2" x 2" MAX.	TAPE AND REEL		
			MIN.	MAX.	
02016	400 WP 1000 tape and reel	484	1000	5000	8 mm
0402	400 WP 1000 tape and reel	100			

Note

- See “Codification of Packaging” table for additional details

Flip chip:

Tin / silver terminations: (F termination option): Active face down in tape and reel.
Active face up in waffle pack.

One face:

Gold terminations: (P termination option): Active face up.
Please use M termination code for active face down in tape and reel.

Notes

- CHA02016 with active face down in tape and reel have back-side blue marked to indicate right orientation
- Please refer to Vishay Sfernice Application Note Guidelines for Vishay Sfernice Resistive and Inductive Components for soldering recommendation (document number 52029, section “3. Guidelines for Surface Mounting Components (SMD)”, profile number 3 applies

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by a single cover. To avoid stacked waffle packs when ordered quantity exceeds the maximum number of pieces per package, please consult Vishay Sfernice for specific ordering code.

Tape and Reel

See Part Numbering information to get the quantity desired by tape.

Regarding the CHA02016 size only, up to 5 empty cavities can be found every 1000 parts in the reel. Nevertheless, the number of requested parts will be respected.

GLOBAL PART NUMBER INFORMATION

Part Number Example: CHA02016-100RGFTF (AEC-Q200 qualified CH series, 100 Ω, 2 % tolerance, 5000 pieces reels)

C	H	A	0	2	0	1	6	-	1	0	0	R	G	F	T	F

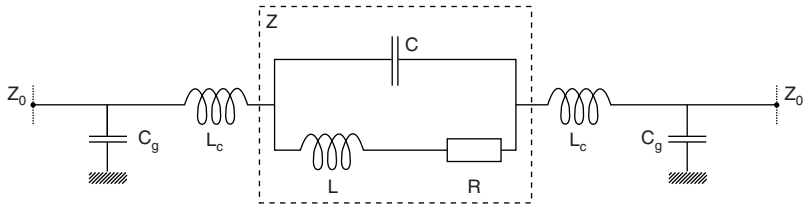
GLOBAL MODEL	SIZE	OHMIC VALUE	TOLERANCE	TERMINATION	PACKAGING
CHA	**02016** **0402**	**10R to 500R**	**F** = 1 % **G** = 2 % **J** = 5 %	**F** (flip chip): SnAg over nickel barrier **N** (W/A): SnAg over nickel barrier (except 02016) **P** (one face) (1): gold bonding pads (except 0402)	For more information see “Codification of Packaging” table

Note

(1) Gold termination for application in hermetic package: can also be mounted on PCB with SnAg solder

CODIFICATION OF PACKAGING	
WAFFLE PACK	
W	400 min.,1 mult.
PLASTIC TAPE	
TD	1000 min., 1000 mult.; delivered in reels of 1000 pcs
TF	5000 min., 5000 mult.; delivered in reels of 5000 pcs

TYPICAL HIGH FREQUENCY PERFORMANCE ELECTRICAL MODEL



C	Internal shunt capacitance
L	Internal inductance
R	Resistance
Z	Internal impedance (R, L, C)
L_c	External connection inductance
C_g	External capacitance to ground

The complex impedance of the chip resistor is given by the following equations:

$$Z = \frac{R + j\omega(L - R^2C - L^2C\omega^2)}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]}$$

$$\frac{[Z]}{R} = \frac{1}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]} \times \sqrt{1 + \left[\frac{\omega(L - R^2C - L^2C\omega^2)}{R}\right]^2}$$

$$\theta = \tan^{-1}\frac{\omega(L - R^2C - L^2C\omega^2)}{R}$$

Notes

- $\omega = 2 \times \pi \times f$
- f: frequency

R, L, and C are relevant to the chip resistor itself.

L_c and C_g also depend on the way the chip resistor is mounted.

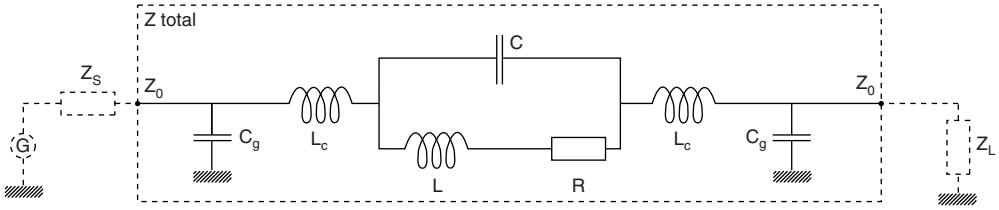
It is important to notice that after assembly the external reactance of L_c and C_g will be combined to internal reactance of L and C. This combination can upgrade or downgrade the HF behavior of the component.

This is why we are displaying three sets of data:

- $\frac{[Z]}{R}$ versus frequency curves which aim to show at a glance the intrinsic HF performance of a given chip resistor
- $\frac{[Z_{total}]}{R}$ versus frequency curves which aim to show the behavior of the chip resistor when mounted

These lines are terminated with adapted source and load impedance respectively Z_s and Z_l with $Z_0 = Z_L = Z_s$ (for other configurations please consult us).

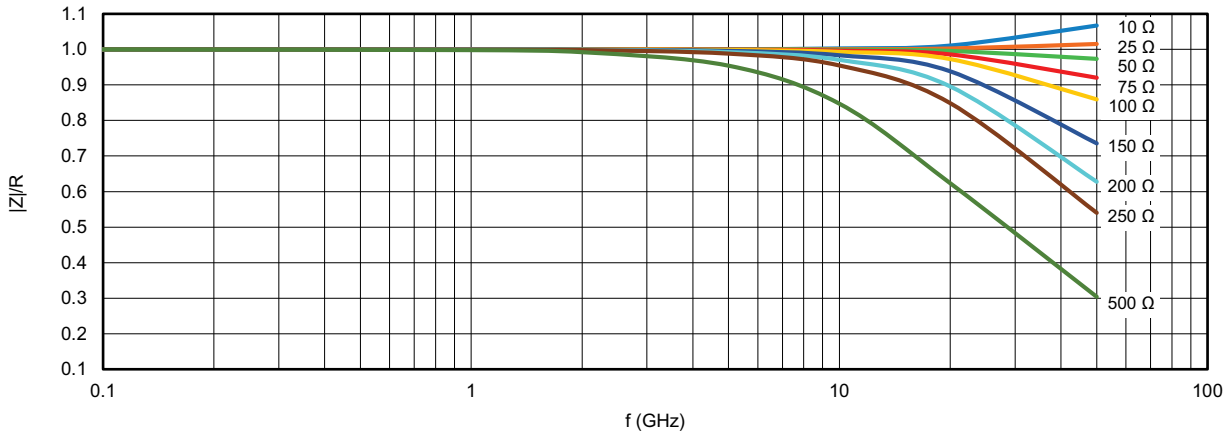
Equivalent circuit for S-parameters:



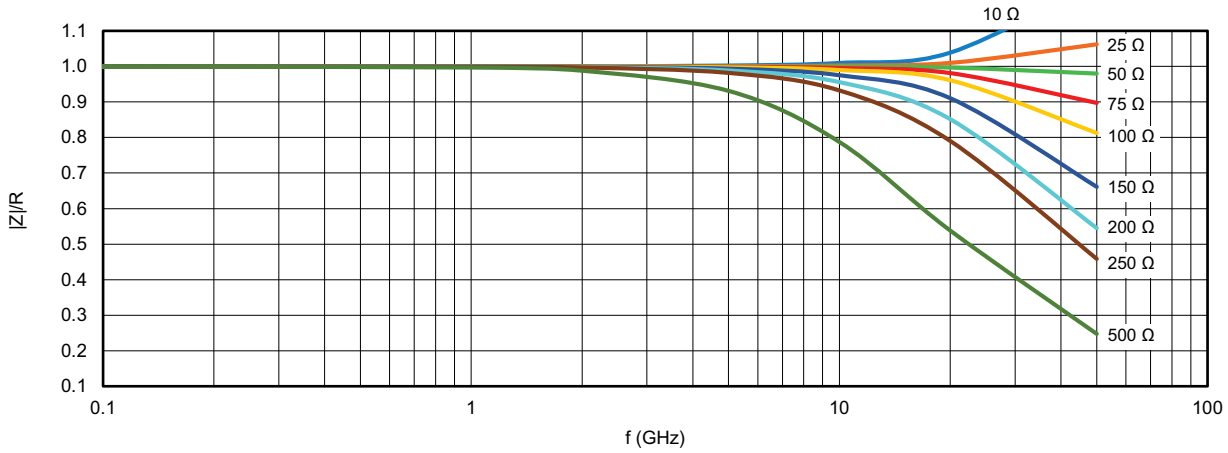
S-parameters are computed taking into account all the resistive, inductive and capacitive elements (Z total) and $Z_0 = Z_L = Z_s = R$.

For simulation purposes, those S-parameter data are available for download here: www.vishay.com/doc?53061

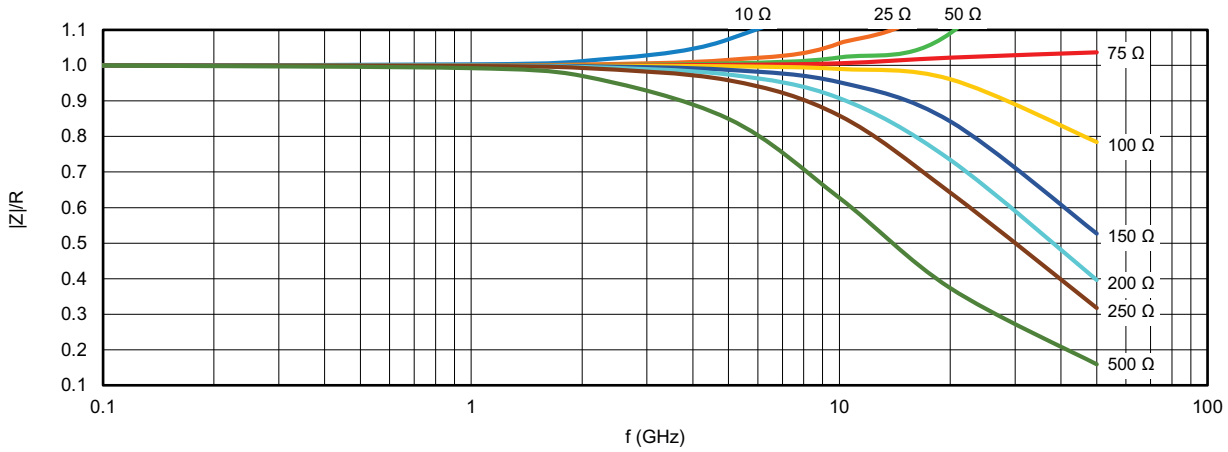
INTERNAL IMPEDANCE CURVES



Internal impedance curve for 02016 size (F and P terminations)

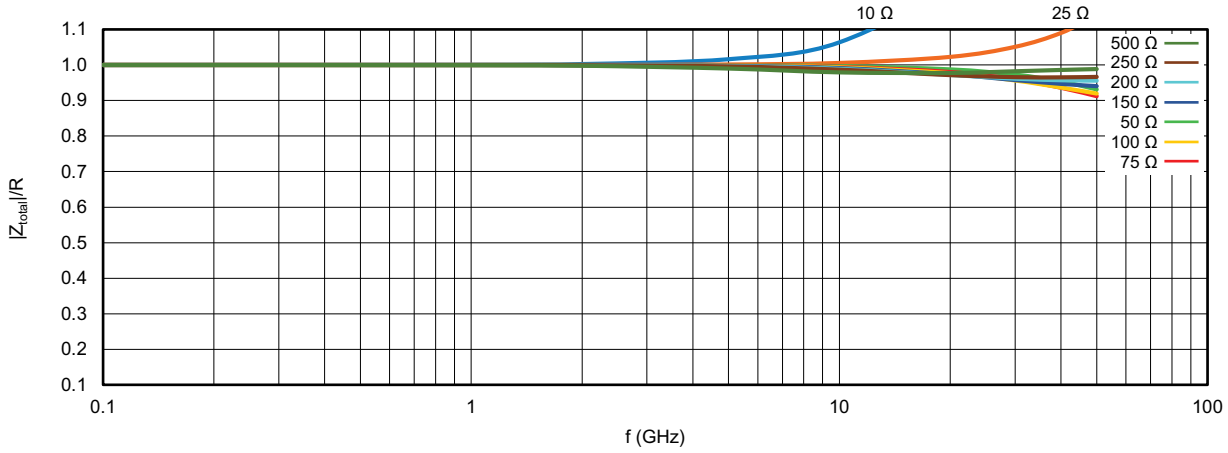


Internal impedance curve for 0402 size (F termination)

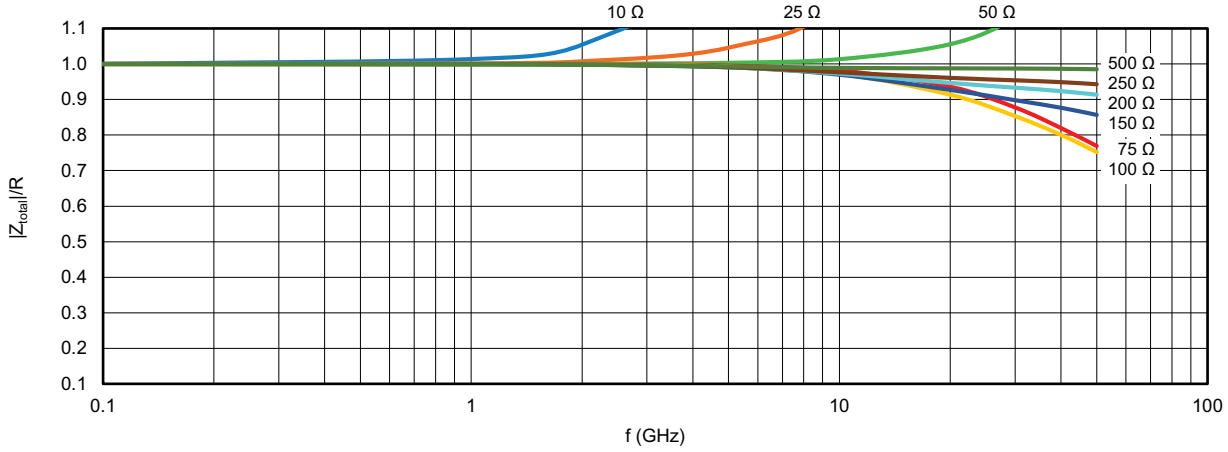


Internal impedance curve for 0402 size (N termination)

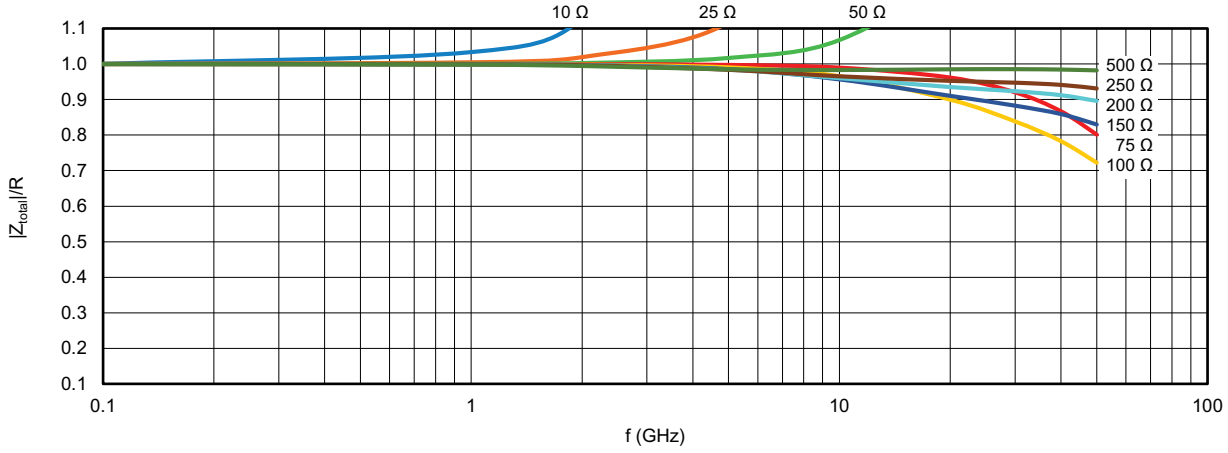
INTERNAL IMPEDANCE CURVES ($|Z_{TOTAL}|$ / R)



Internal impedance curve for 02016 size (F and P terminations)



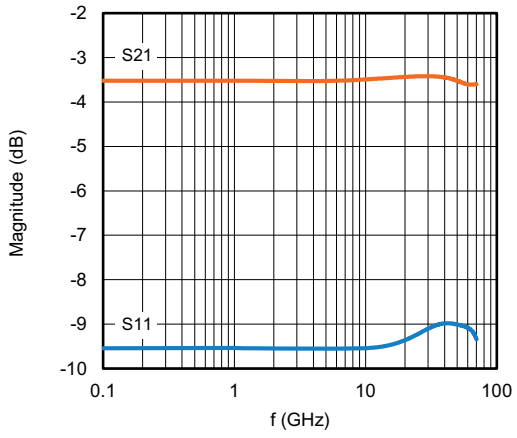
Internal impedance curve for 0402 size (F termination)



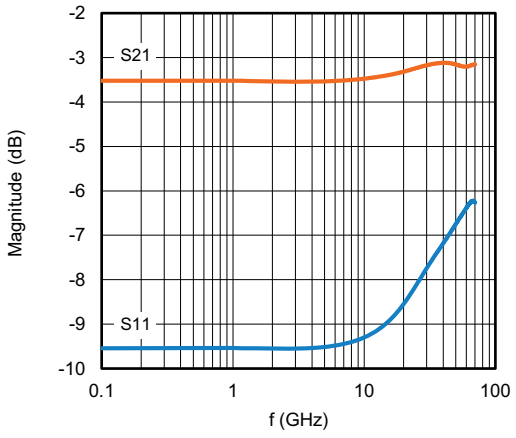
Internal impedance curve for 0402 size (N termination)

S-PARAMETER

CHA02016 (F and P Terminations)

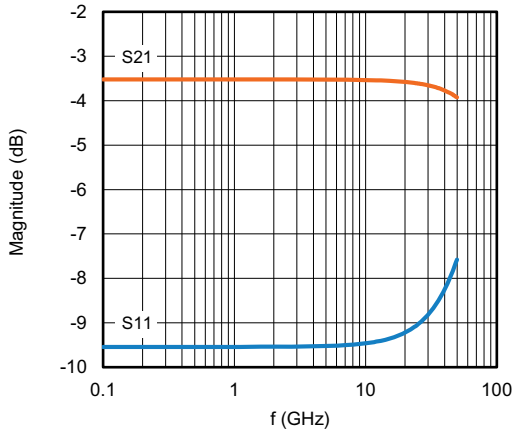


CHA02016 flip chip ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)

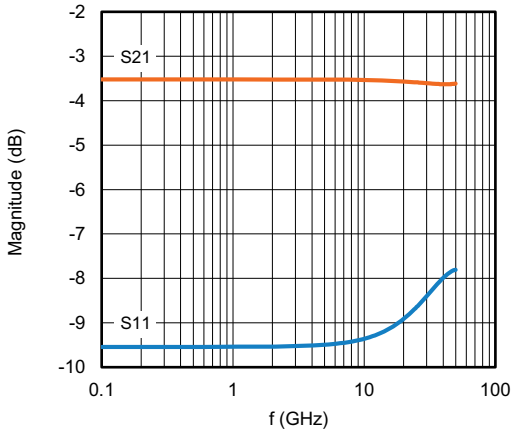


CHA02016 flip chip ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

CHA0402 (F Terminations)

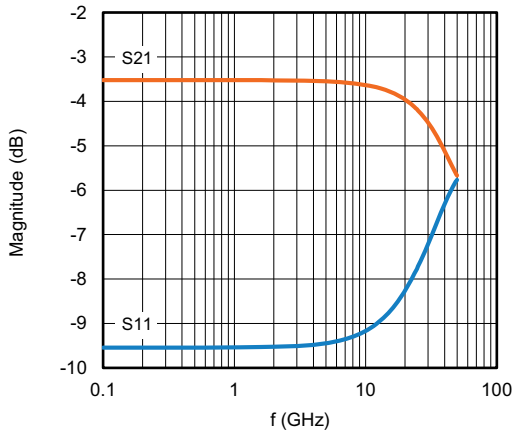


CHA0402 flip chip ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)

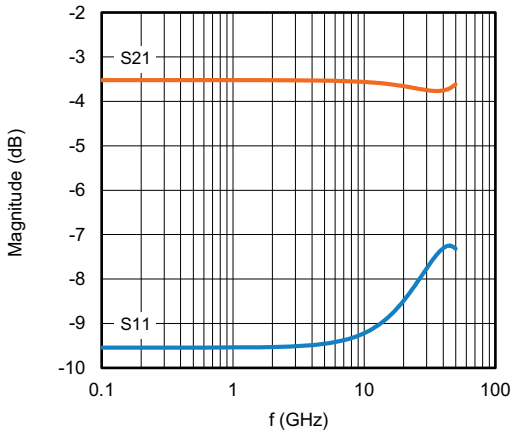


CHA0402 flip chip ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

CHA0402 (N Terminations)



CHA0402 wraparound ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)



CHA0402 wraparound ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

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