Single Channel High Speed Low Side HEMT GaN Driver with Negative Input Capability (20V Supply, 2A peak source and sink current)

1 FEATURES

- 2A Peak Source Current and 2A Peak Sink Current
- Fixed Output Level, High as V6V and Low as GND
- 5.2V - 20V Wide Supply Voltage Range
- Down to -5V Negative Input Voltage Capability
- Fast Propagation Delay: 15ns and 13ns
- Fast Rising and Falling Time: 9ns and 5ns
- Under Voltage Lock Out Protection
- Low Quiescent Current: 104uA
- Output Low When Input Floating

2 APPLICATIONS

- HEMT GaN Device Gate Driver

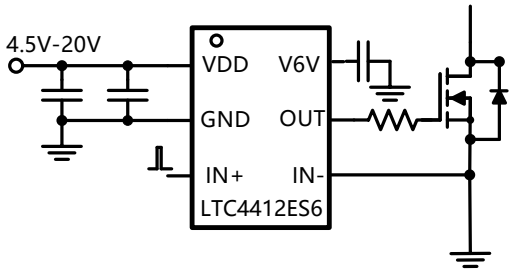
3 ORDERING INFORMATION

TYPE	MARKING	PACKAGE
LTC4412ES6	7251	TSOT23-6L

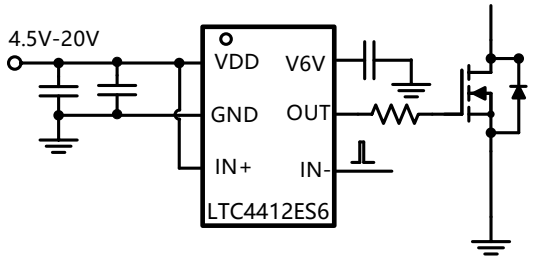
4 DISCRIPTION

The LTC4412ES6, single channel high speed low side gate driver, provides 2A peak source and 2A sink current along with integrated V6V LDO rail-to-rail driving capability for GaN power device. The device features a 15ns input to output rising and 13ns input to output falling propagation delay and 20V power supply rail makes it suitable for high frequency power converter application. The negative input is acceptable down to -5V for enhancing the input noise immunity. The Flexible configuration of the IN+ and IN- input makes LTC4412ES6 either as non-inverting or inverting driver. It operates over a wide temperature range -40°C to 150°C and available in a TSOT23-6L package.

5 TYPICAL APPLICATIONS

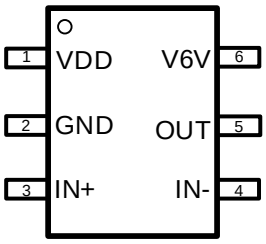


Non-Inverting Input



Inverting Input

6 PIN CONFIGURATION AND FUNCTIONS



LTC4412ES6(Top View)

PIN OUT		I/O	PIN FUNCTION
NAME	NO.		
VDD	1	I	Power supply of gate driver. Must be decoupled by ceramic cap. A 0.1uF, and 1uF or 10uF are recommended.
GND	2	I	Power ground. Must be soldered directly to ground planes for improved thermal performance and electrical contact.
IN+	3	I	Non-inverting logic input, floating logic low. In Non-Inverting configuration, apply PWM signal on IN+. In inverting configuration, connect IN+ to VDD.
IN-	4	I	Inverting logic input, floating logic low. In Non-Inverting configuration, connect IN- to GND. In inverting configuration, apply PWM signal on IN-.
OUT	5	O	Gate driver output.
V6V	6	O	An integrated LDO output, must be decoupled by ceramic cap. A 0.1uF, and 1uF or 10uF are recommended.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Logic Input	IN+, IN-	-5	22	V
Gate Driver Output	OUT	-0.3	22	V
Supply Voltage	VDD	-0.3	22	V
V6V Voltage	V6V	0	6.5	V
Operating junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-65	150	°C

7.2 ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (1)	-1	+1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

7.3 RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	5.2	20	V
$V_{IN+,IN-}$	Input voltage range	-5	20	V
T_J	Operating junction temperature	-40	150	°C

7.4 ELECTRICAL CHARACTERISTICS

V_{DD}=12V, T_J=-40°C~150°C, typical values are tested under T_J=25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{DD}	Operating supply voltage		5.2		20	V
V_{DD_UVLO}	Input UVLO	V_{DD} rising		4.9	5.2	V

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
	Hysteresis			400		mV
I_Q	Quiescent current	IN+=GND, IN-=VDD, V_{DD}=12V		104		uA
INPUTS						
V_{IN+_H}	Input+ logic high threshold			3.1	3.5	V
V_{IN+_L}	Input+ logic low threshold		1.03	1.15		V
V_{IN+_Hys}	Hysteresis			1.95		V
V_{IN-_H}	Input- logic high threshold			3.1	3.5	V
V_{IN-_L}	Input- logic low threshold		1.03	1.15		V
V_{IN-_Hys}	Hysteresis			1.95		V
OUTPUT						
$I_{SINK/SRC}$	Output Sink/Source peak current	C_{Load}=10nF, F_{sw}=1kHz		2		A
V_{OUT_H}	Output high voltage	I_{OUT}= -10mA	5.8	6.1	6.5	V
V_{OUT_L}	Output low voltage	I_{OUT}= -10mA		0.01	0.1	V
R_{OH}	Output pull high resistance	I_{OUT}= - 10mA		9.1	14.7	Ω
R_{OL}	Output pull low resistance	I_{OUT}= 10mA		1.1	2.0	Ω
V_{V6V}	LDO output voltage	VDD=12V, I_{V6V}=0mA	5.8	6.2	6.5	V
		VDD=12V, I_{V6V}=10mA	5.8	6.2	6.5	V
Timing						
T_R	Output rising time	C_{Load}=1nF		9		ns
T_F	Output falling time	C_{Load}=1nF		5		ns
T_{D_IN+}	IN+ to output propagation delay, Rising edge			15		ns
	IN+ to output propagation delay, Falling edge			13		ns
T_{D_IN-}	IN- to output propagation delay, Rising			13		ns
	IN- to output propagation delay, Falling			15		ns
T_{MIN_ON}	Minimum input pulse width	C_{Load}=1nF		15	26	ns

8 TYPICAL CHARACTERISTICS

V_{DD}=12V, Cload=1nF, T_A= 25°C, unless otherwise noted.

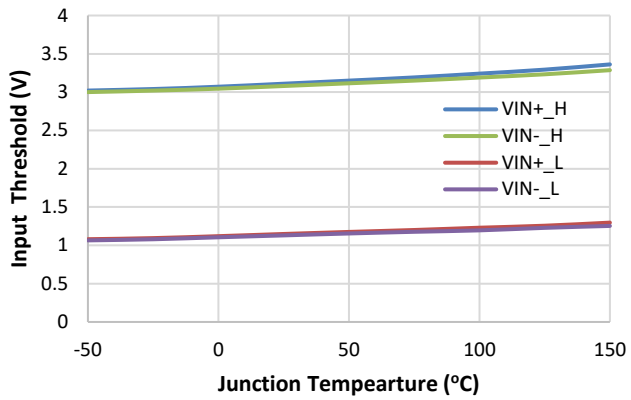


Figure 1. IN Threshold Vs. Temperature

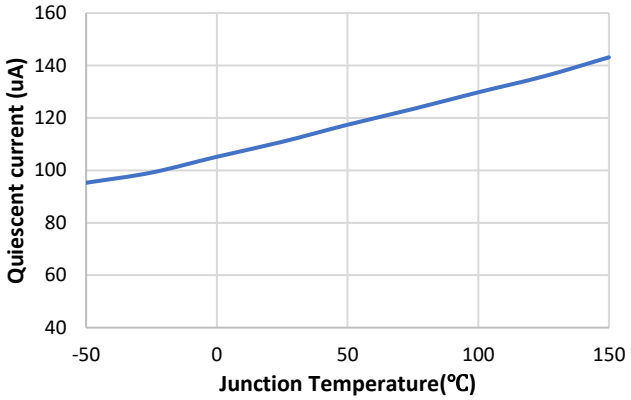


Figure 2. Quiescent Current Vs. Temperature

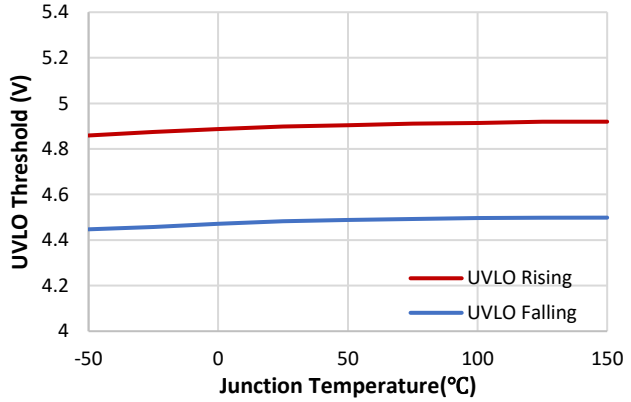


Figure 3. UVLO Vs. Temperature

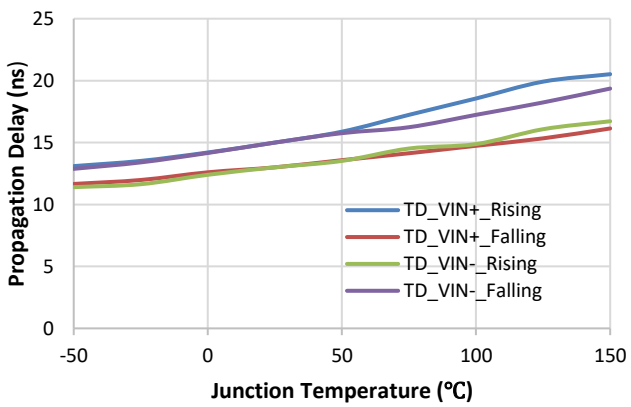


Figure 4. Propagation Delay Vs. Temperature

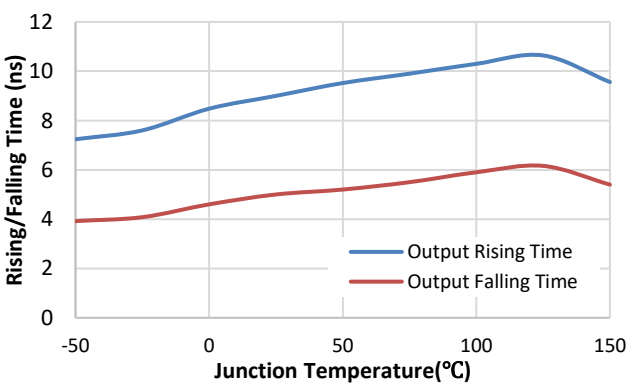


Figure 5. Output Rising/Falling Time Vs. Temperature

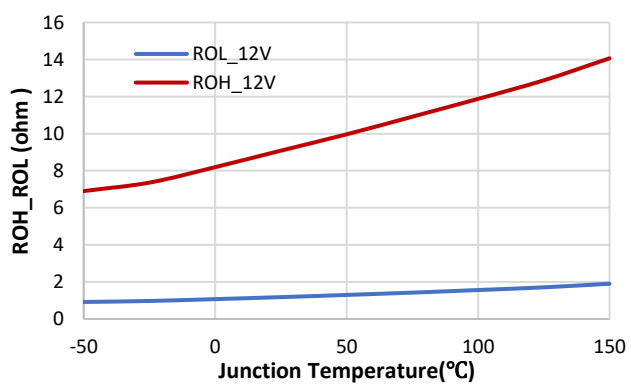


Figure 6. Output Resistance Vs. Temperature

9 FUNCTIONAL BLOCK DIAGRAM

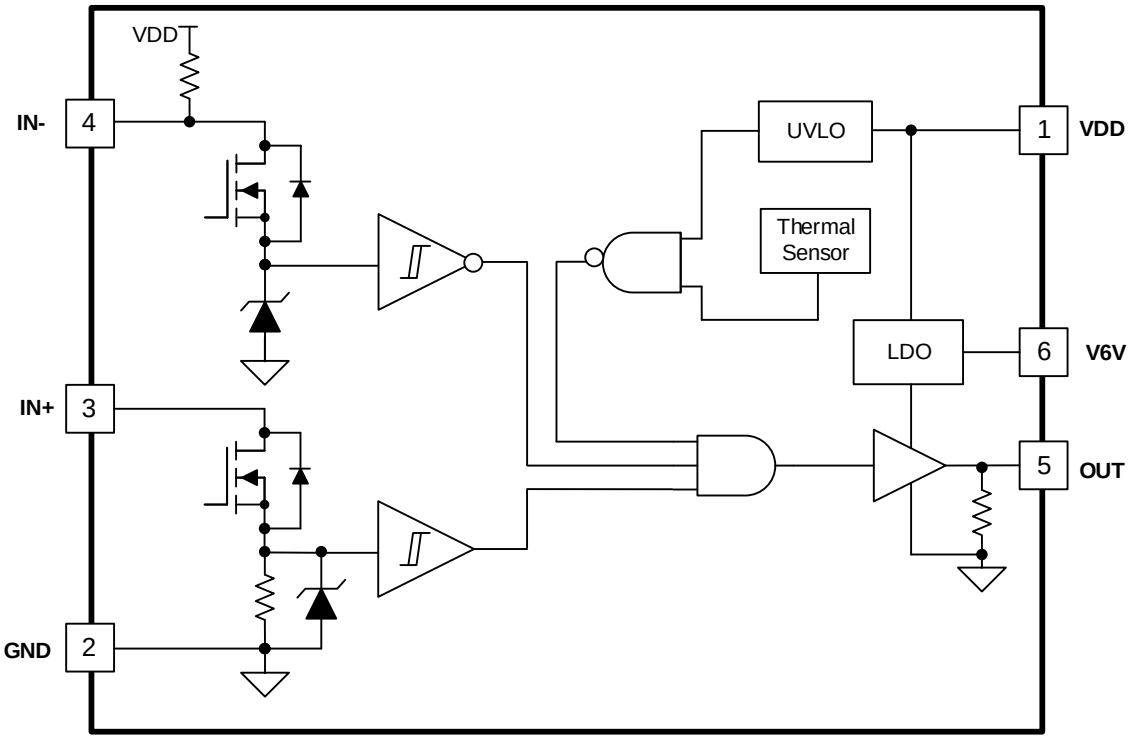


Figure 7. Block Diagram

10 DISCRIPTION

10.1 Overview

The LTC4412ES6 is a single channel, high speed, low side gate driver specially for power GaN HMET with up to 20V wide supply and 2A source/sink peak current along with the input to output rising and falling propagation delay of 15ns and 13ns. The input is able to be down to -5V DC which enhances the driver input stage noise immunity.

A 6.2V LDO is integrated in the gate driver, the LDO supplies the power to the gate of HEMT GaN directly, which simplifies the off-chip components and minimize the PCB board in the layout.

The 6.2V rail-to-rail output improves the LTC4412ES6 output stage robustness during the switching load fast transition.

10.2 VDD Power Supply

The LTC4412ES6 operates under a supply voltage range between 4.5V to 20V. It' s recommended to put two VDD bypass capacitor in parallel to prevent noise problems on supply VDD. It has to put a 0.1uF SMT ceramic capacitor as close as possible between the VDD pin to the GND pin. To avoid the unexpected VDD glitch, a large capacitor (ex. 1uF or 10uF) with relatively low ESR must be connected in parallel with that 0.1uF capacitor. This parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

10.3 VDD Under Voltage Lock Out (UVLO)

The LTC4412ES6 implements the Under Voltage Lock Out (UVLO) with rising threshold of typically 5.2V along with 400mV typical hysteresis. The VDD voltage which is able to down to 5.2V is especially suitable for driving wide band gap power device.

The UVLO holds the output low regardless of the input status when VDD is rising but the level is below the UVLO threshold. The hysteresis prevents output bouncing caused by the noise impact on the power supply. During power up, the driver output remains low until the VDD voltage reaches the UVLO threshold. The magnitude of the OUT-signal rises with VDD till V6V steady state reached.

To achieve the minimum R_{dson} of GaN HEMT, the gate of GaN HEMT needs be as high as 6V. As a result, the recommended minimum VDD of LTC4412ES6 is 8V.

Be aware of that there is 45us delay between VDD UVLO high and V6V supply starting to ramp up. The certain ramp up time of V6V is determined by the internal LDO source current and bypass capacitor between V6V and GND, which also needs to be taken into calculation before the first pulse of PWM built-up.

The inverting operation in Figure 8 and non-inverting operation in Figure 9 show that the output remains low till the UVLO threshold reached, and then the output is in-phase with the input.

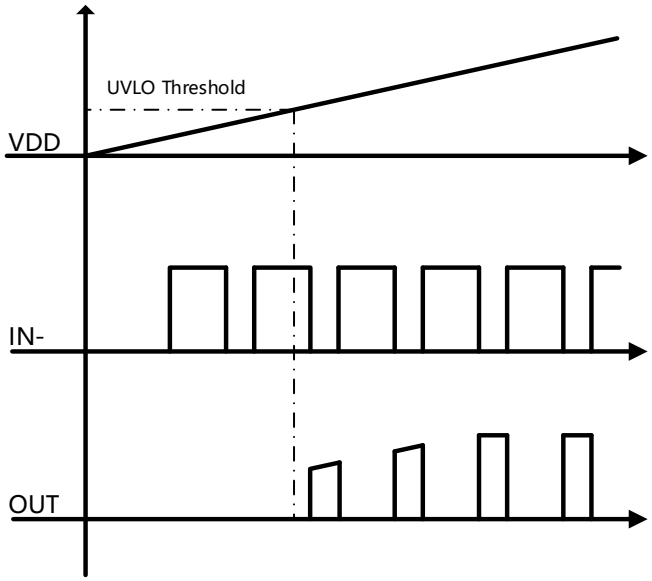


Figure 8. LTC4412ES6 Output (IN- Input) Vs VDD

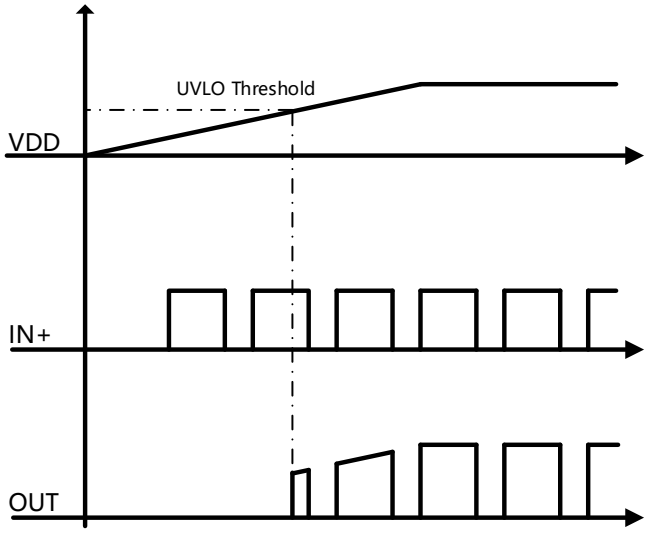


Figure 9. LTC4412ES6 Output (IN+ Input) Vs VDD

10.4 Input Stage

The LTC4412ES6 input is independent of the VDD supply voltage. The typical threshold is 3.1V (high) and 1.15V (low), which make the device easily driven by PWM control signals derived from 5V digital power-controller devices. The device features wider hysteresis compared to typical threshold of 1.95V which offers enhanced noise immunity. It also implements tight control of the input threshold voltage that ensures stable operation across temperature. The low input capacitance on the input pins increases switching speed and reduces the propagation delay.

10.5 Operation Mode

The dual-input design makes the LTC4412ES6 easy to configure the operation mode of either the inverting (IN– pin) mode or the non-inverting (IN+ pin) mode. The output state is held low when the input pins are floating by the internal pull-up or pull-down resistors. As a result, the unused input pin must be biased properly to ensure that driver output is enabled for normal operation. Table 1 is the device logic truth table.

Table 1. The LTC4412ES6 Mode Configuration and Device Logic

Mode	Configuration	IN+	IN-	OUT
Non-Inverting Mode	IN- to GND	L	GND	L
	IN- to GND	H	GND	H
Inverting Mode	IN+ to VDD	VDD	H	L
	IN+ to VDD	VDD	L	H
Others	N/A	Floating	Any	L
	N/A	Any	Floating	L

11 APPLICATION INFORMATION

11.1 Typical Application

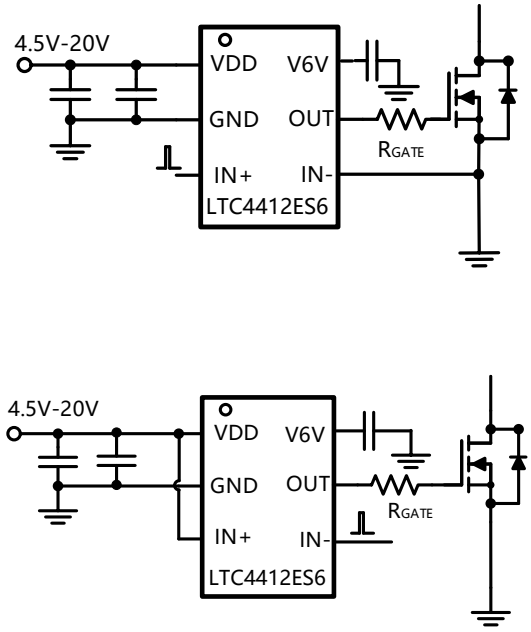


Figure 9. Single Channel Driver Non-Inverting and Inverting Application

11.2 Driver Power Dissipation

Generally, the power dissipation depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The LTC4412ES6 is designed with very low quiescent current.

The power loss of LTC4412ES6 caused by pure capacitive load is:

$$P_G = C_{Load} * V_{v6v}^2 * f_{SW} \quad (1)$$

Where

- V_{v6v} is LDO output voltage with typical 6.2V
- C_{Load} is the output capacitance
- f_{SW} is the switching frequency

This equation (1) is also able to be adopted to calculate the switching load of power MOSFET, where gate charge Qg determines the capacitor charges.

$$Q_g = C_{LOAD} \times V_{v6v} \quad (2)$$

Normally power device manufacturers provide specifications with the typical and maximum Qg, in nC, to switch the device under specified conditions.

$$P_G = Q_g * V_{v6v} * f_{SW} \quad (3)$$

Where

- Q_g is the gate charge of the power device
- f_{SW} is the switching frequency
- V_{DD} is LDO output voltage with typical 6.2V

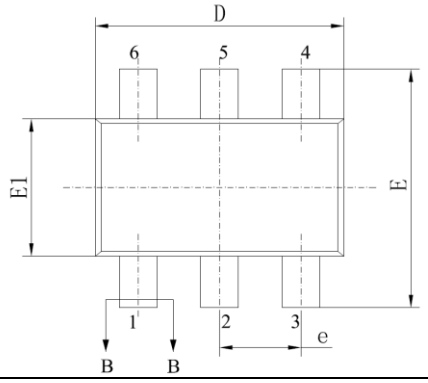
Sometimes, circuit designers put a resistor R_{GATE} between the driver output pin and the gate terminal of power device to slow down the power device transition. The power dissipation of the driver shows as below:

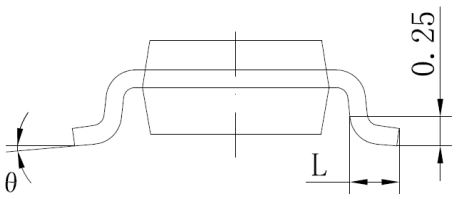
$$P_G = \frac{1}{2} * Q_g * V_{v6v} * f_{SW} * \left(\frac{R_{OL}}{R_{OL} + R_{GATE}} + \frac{R_{OH}}{R_{OH} + R_{GATE}}\right) \quad (3)$$

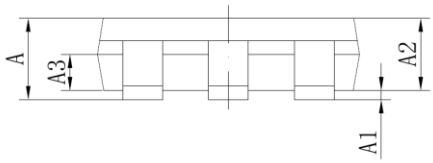
Where

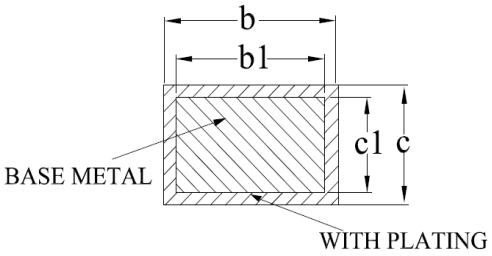
- R_{OH} is the equivalent pull up resistance of LTC4412ES6
- R_{OL} is the equivalent pull down resistance of LTC4412ES6
- R_{GATE} is the gate resistance between driver output and gate of power device.

PACKAGE INFORMATION (TSOT23-6L Package)









SECTION B-B

Symbol	Millimeter		
	Min	Nor	Max
A	-	-	0.95
A1	0	-	0.10
A2	0.75	0.80	0.85
A3	0.35	0.40	0.45
b	0.38	-	0.46
b1	0.37	0.40	0.43
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
L	0.30	0.40	0.50
θ	0	-	8°