



QNHCHIP

QN4812

Product Specification

QN4812

30V Dual N-Channel MOSFET



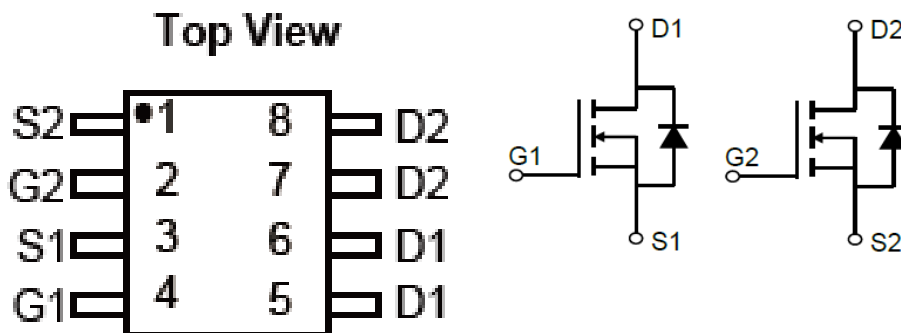
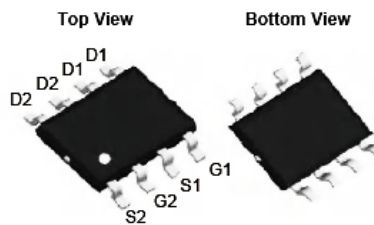
FEATURES

- 30V, 8A
 - $R_{DS(ON)} < 23m\Omega @ V_{GS} = 10V$
 - $R_{DS(ON)} < 26m\Omega @ V_{GS} = 4.5V$
 - $R_{DS(ON)} < 36m\Omega @ V_{GS} = 2.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management

Pin Description



Schematic Diagram

NO.	Symbol	Description
1	S2	SOURCE 2
2	G2	GATE 2
3	S1	SOURCE 1
4	G1	GATE 1
5	D1	DRAIN 1
6	D1	DRAIN 1
7	D2	DRAIN 2
8	D2	DRAIN 2



Absolute Maximum Ratings

(@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units	
V_{DS}	Drain-to-Source Voltage	30	V	
V_{GS}	Gate-to-Source Voltage	± 12	V	
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	8	A
		$T_A = 100^\circ\text{C}$	5	
I_{DM}	Pulsed Drain Current ⁽¹⁾	32	A	
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	16	mJ	
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	1.8	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	70	$^\circ\text{C}/\text{W}$	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$	



Electrical Characteristics

($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 12\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.6	1.0	1.3	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS}=10\text{V}, I_D=4.2\text{A}$	-	21	23	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=4\text{A}$	-	24	26	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_D=1\text{A}$	-	34	36	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$	-	462	-	pF
C_{oss}	Output Capacitance		-	65	-	pF
C_{rss}	Reverse Transfer Capacitance		-	44	-	pF
Q_g	Total Gate Charge	$V_{GS}=0\sim 4.5\text{V}, V_{DS}=15\text{V}, I_D=3\text{A}$	-	9	-	nC
Q_{gs}	Gate Source Charge		-	2	-	nC
Q_{gd}	Gate Drain ("Miller") Charge		-	2.1	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DD}=15\text{V}, I_D=3\text{A}, R_{GEN}=3\Omega$	-	4	-	ns
t_r	Turn-On Rise Time		-	11	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	24	-	ns
t_f	Turn-Off Fall Time		-	2	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	8	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	32	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}, I_S=8\text{A}$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F=3\text{A}, di/dt=100\text{A}/\mu\text{s}$	-	8.4	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	3.3	-	nC

Notes:

- Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
- E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=15\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=8\text{A}$
- $R_{\theta JA}$ is measured with the device mounted on a 1 inch² pad of 2oz copper FR4 PCB
- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$



Typical Performance Characteristics

Figure 1: Output Characteristics

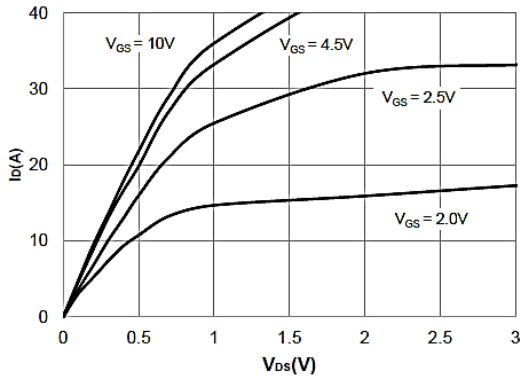


Figure 2: Typical Transfer Characteristics

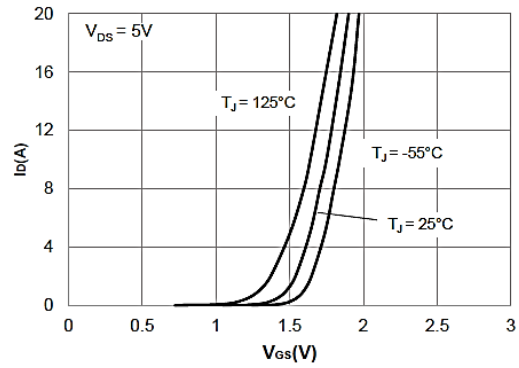


Figure 3: On-resistance vs. Drain Current

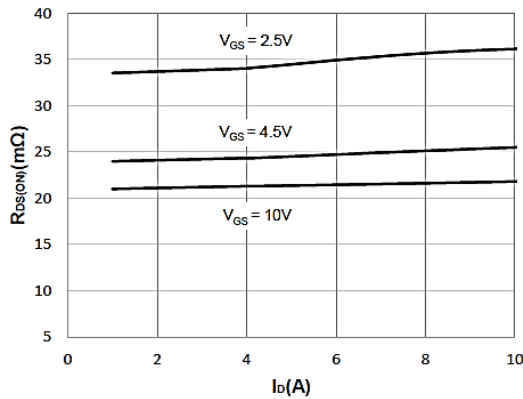


Figure 4: Body Diode Characteristics

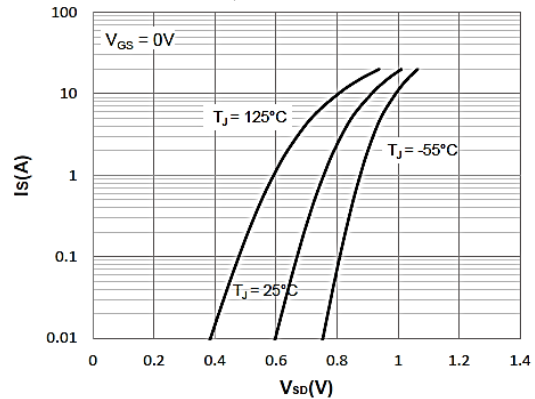


Figure 5: Gate Charge Characteristics

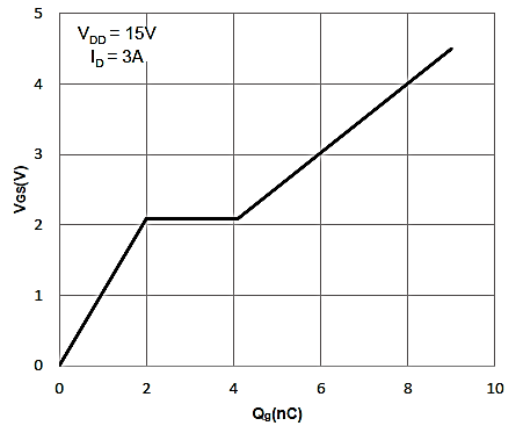


Figure 6: Capacitance Characteristics

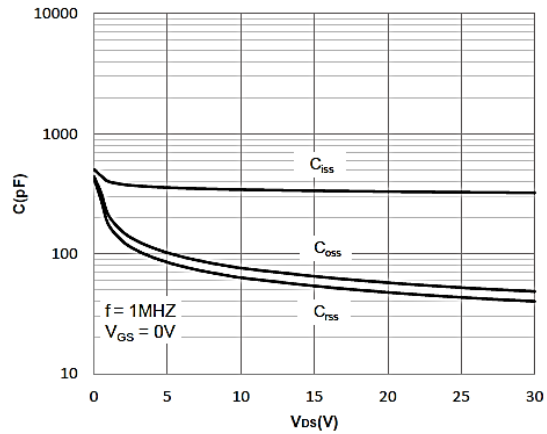


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

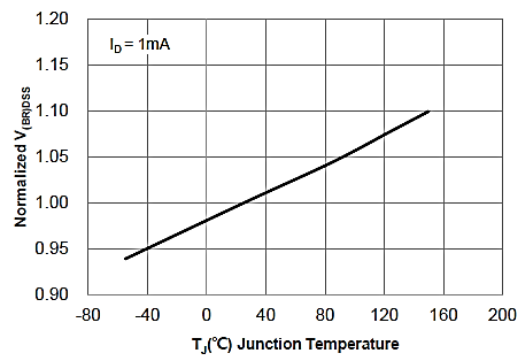


Figure 8: Normalized on Resistance vs. Junction Temperature

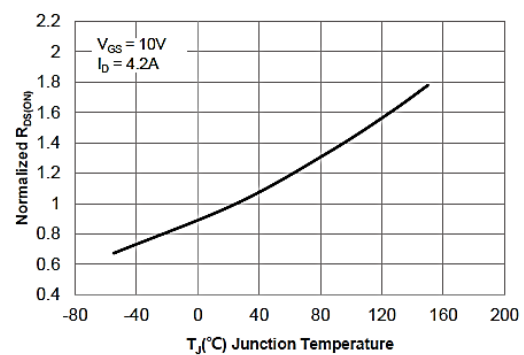




Figure 9: Maximum Safe Operating Area

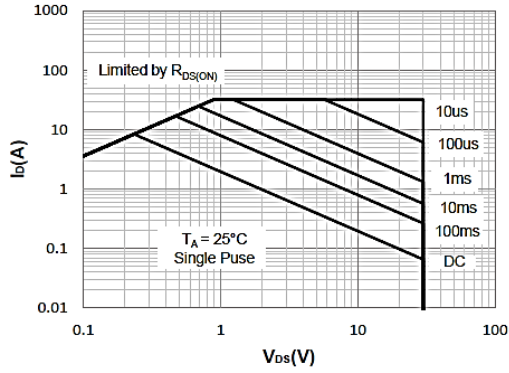


Figure 10: Maximum Continuous Driian Current vs. Ambient Temperature

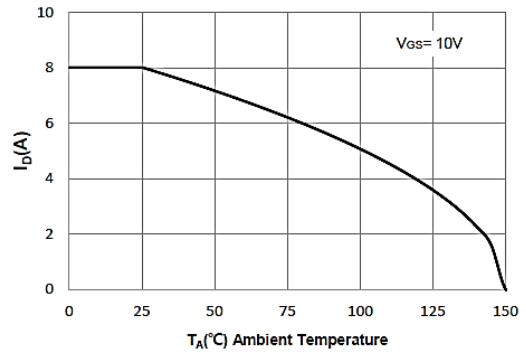


Figure 11: Normalized Maximum Transient Thermal Impedance

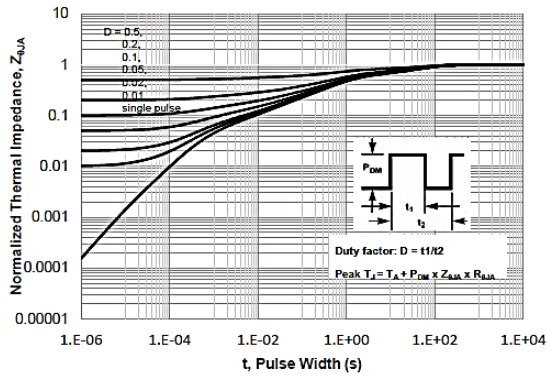
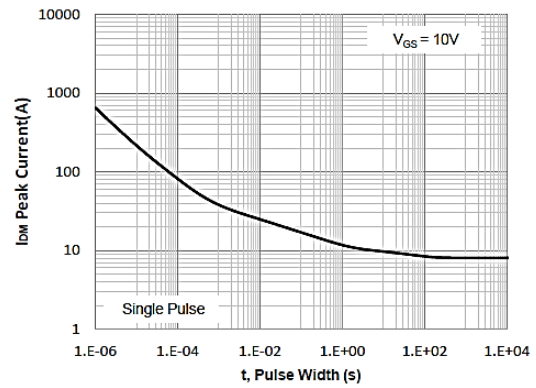


Figure 12: Peak Current Capacity





Test Circuit

Figure 1: Gate Charge Test Circuit & Waveform

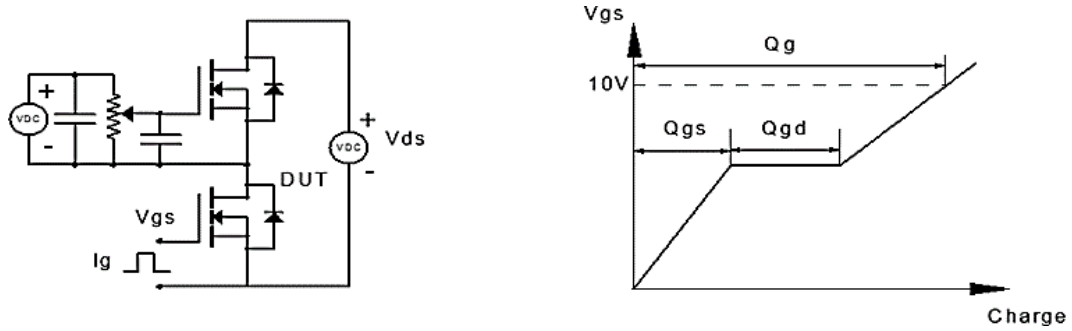


Figure 2: Resistive Switching Test Circuit & Waveform

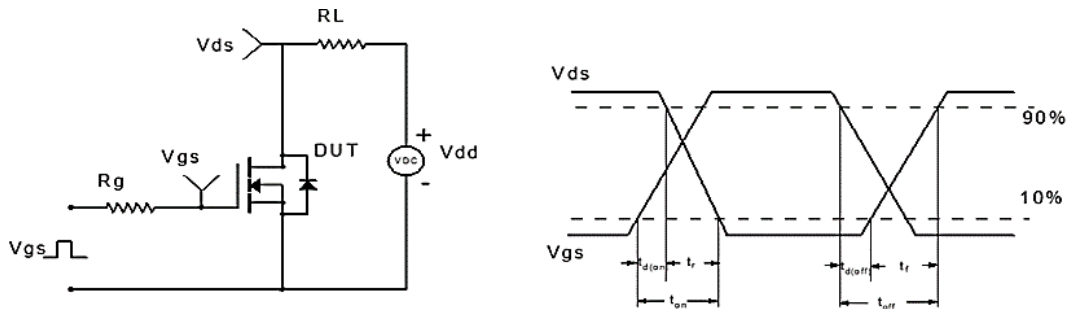


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

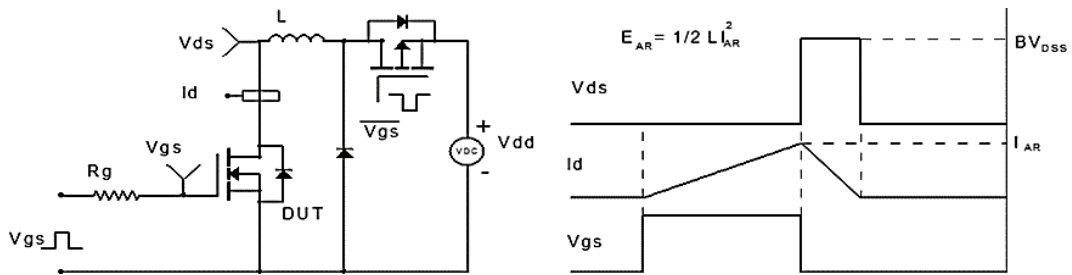
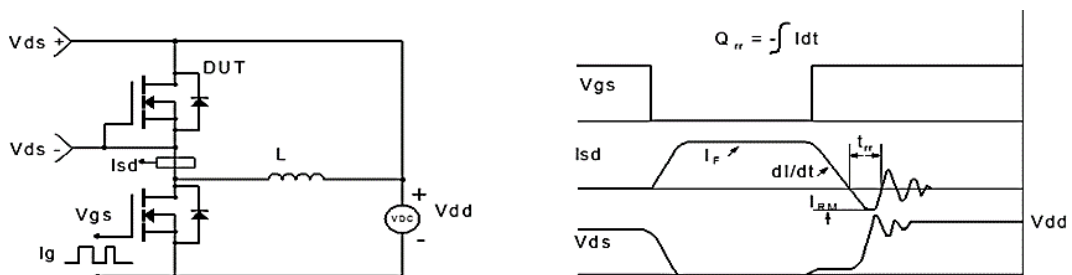


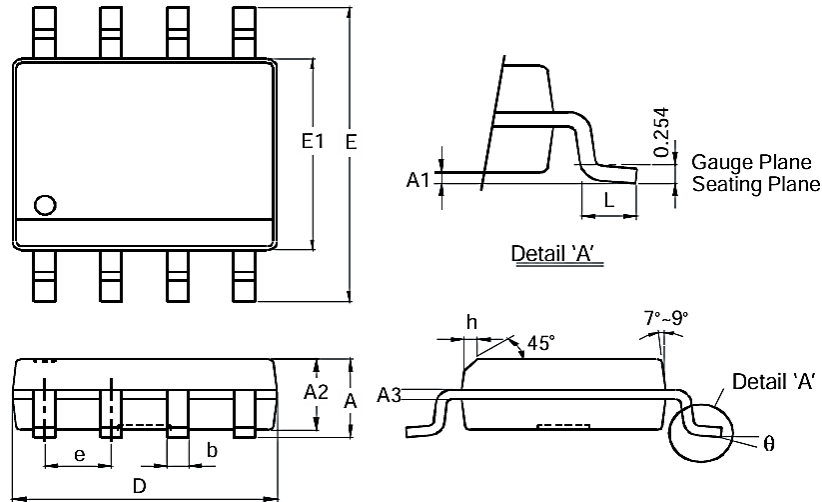
Figure 4: Diode Recovery Test Circuit & Waveform





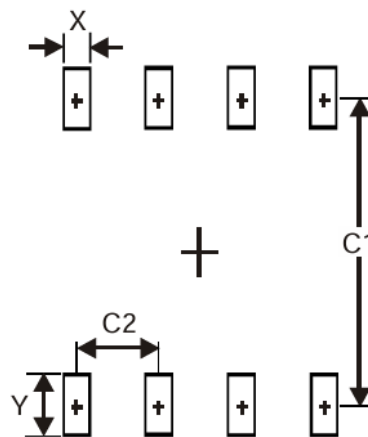
Package Mechanical Data

SOP-8



Dim	Min(mm)	Max(mm)
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°

suggested Pad Layout



Dimensions	Value(mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27



Ordering information

Order Code	Package	V _{DS} (V)	I _D (A)	R _{DS(ON)} (m Ω)	
QN4812	SOP-8	30	8	V _{GS} =10V	< 23
				V _{GS} =4.5V	< 26
				V _{GS} =2.5V	< 36