



QNHCHIP

QN16ND18AX

Product Specification

QN16ND18AX

12V Dual N-Channel MOSFET



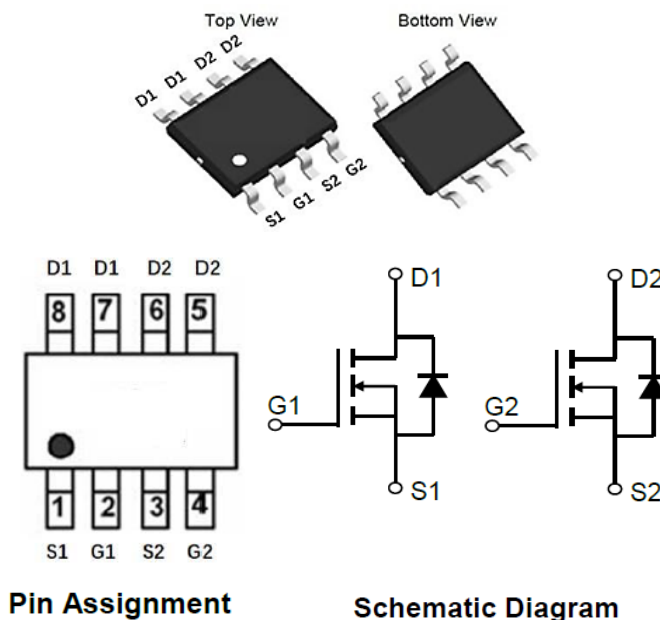
FEATURES

- 12V, 7A
 $R_{DS(ON)}$ TYP.=10.5m Ω @ $V_{GS} = 4.5V$
 $R_{DS(ON)}$ TYP.=13.5m Ω @ $V_{GS} = 2.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management

Pin Description



NO.	Symbol	Description
1	S1	SOURCE 1
2	G1	GATE 1
3	S2	SOURCE 2
4	G2	GATE 2
5	D2	DRAIN 2
6	D2	DRAIN 2
7	D1	DRAIN 1
8	D1	DRAIN 1



Absolute Maximum Ratings

(@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units	
V_{DS}	Drain-to-Source Voltage	12	V	
V_{GS}	Gate-to-Source Voltage	± 12	V	
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	7	A
		$T_A = 100^\circ\text{C}$	4.2	
I_{DM}	Pulsed Drain Current ⁽¹⁾	28	A	
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	16	mJ	
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	1.6	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	80	$^\circ\text{C}/\text{W}$	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$	



Electrical Characteristics

($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	12	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=12\text{V}, V_{GS}=0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 12\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.4	0.7	1.0	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS}=4.5\text{V}, I_D=3.5\text{A}$	-	10.5	14.5	m Ω
		$V_{GS}=2.5\text{V}, I_D=2\text{A}$	-	13.5	18.5	m Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=6\text{V}, f=1\text{MHz}$	-	760	-	pF
C_{oss}	Output Capacitance		-	105	-	pF
C_{rss}	Reverse Transfer Capacitance		-	89	-	pF
Q_g	Total Gate Charge	$V_{GS}=0\sim 4.5\text{V}, V_{DD}=6\text{V}, I_D=3\text{A}$	-	9	-	nC
Q_{gs}	Gate Source Charge		-	1.5	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	2.5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	$V_{GS}=4.5\text{V}, V_{DD}=6\text{V}, I_D=3\text{A}, R_{GEN}=3\Omega$	-	5	-	ns
t_r	Turn-On Rise Time		-	16	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	23	-	ns
t_f	Turn-Off Fall Time		-	7	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	7	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	28	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}, I_S=7.0\text{A}$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F=3\text{A}, di/dt=100\text{A}/\mu\text{s}$	-	7	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	2	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=10\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=7\text{A}$
3. $R_{\theta JA}$ is measured with the device mounted on a 1 inch² pad of 2oz copper FR4 PCB
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



Test Circuit

Figure 1: Gate Charge Test Circuit & Waveform

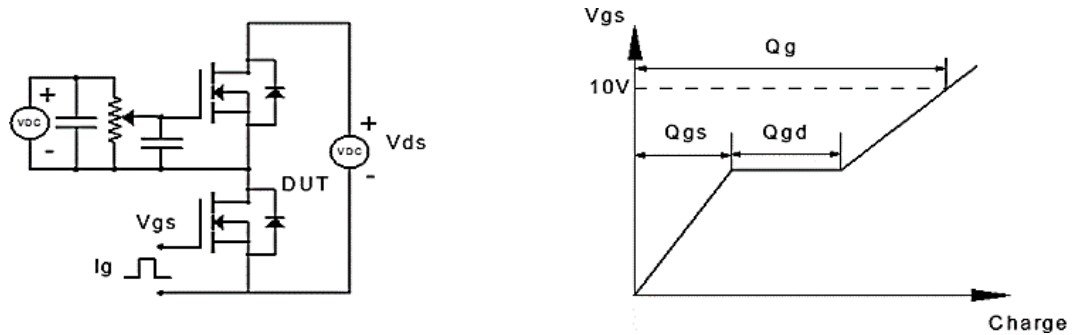


Figure 2: Resistive Switching Test Circuit & Waveform

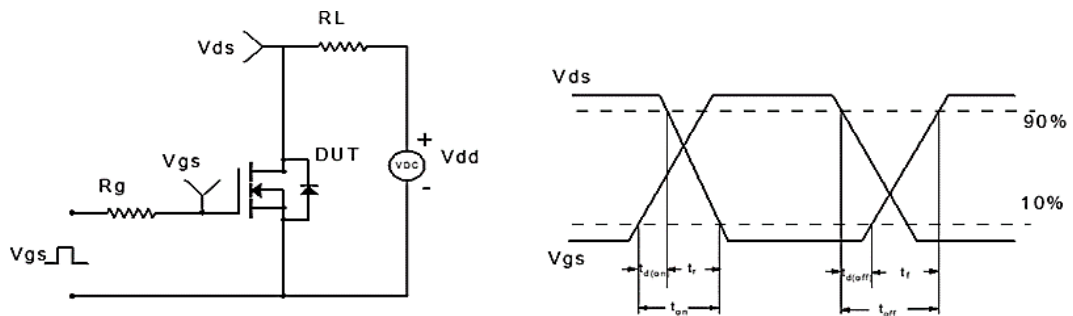


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

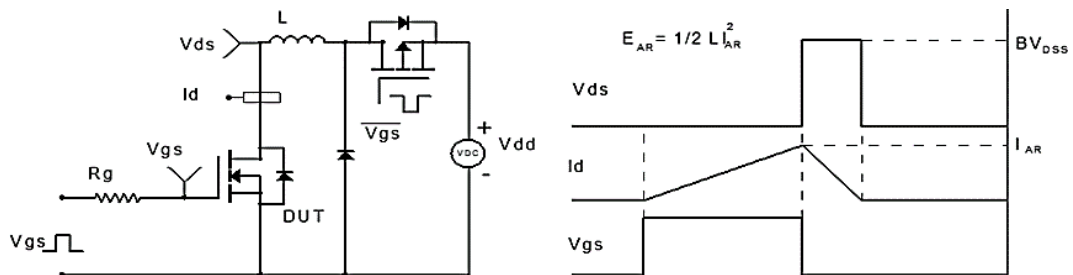
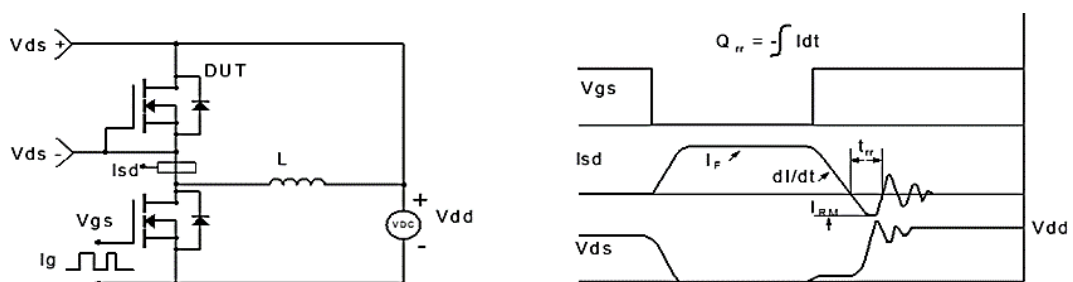


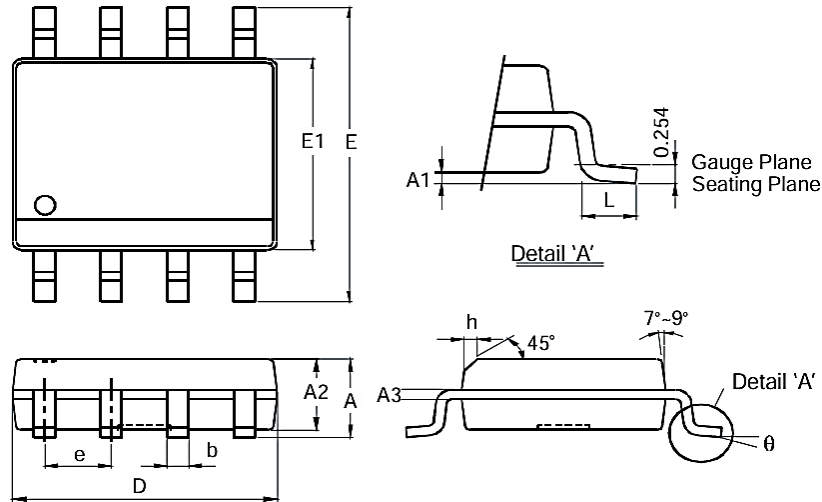
Figure 4: Diode Recovery Test Circuit & Waveform





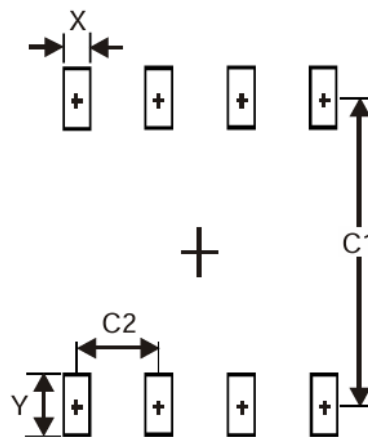
Package Mechanical Data

SOP-8



Dim	Min(mm)	Max(mm)
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°

suggested Pad Layout



Dimensions	Value(mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27



Ordering information

Order Code	Package	V _{DS} (V)	I _D (A)	R _{DS(ON)} (m Ω)	
QNC12ND11AX	SOP-8	12	7	V _{GS} =4.5V	10.5
				V _{GS} =2.5V	13.5