



QNHCHIP

QND120N02AJ

Product Specification

QND120N02AJ

20V N-Channel MOSFET



Description

- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge

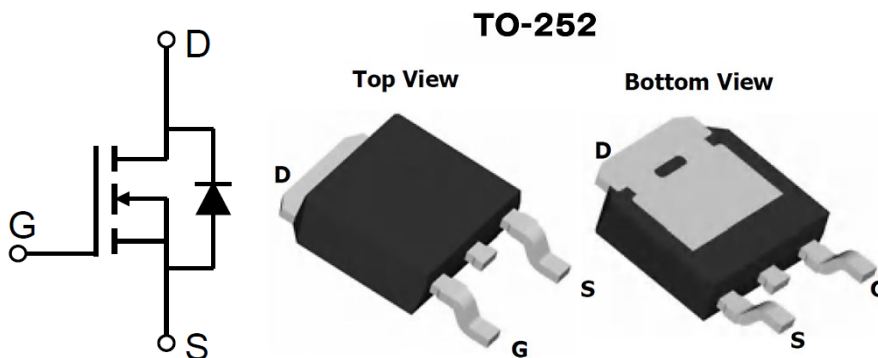
FEATURES

- 20V, 90A
 $R_{DS(ON)}$ TYP= 2.2m Ω @ $V_{GS} = 4.5V$
 $R_{DS(ON)}$ TYP= 2.9m Ω @ $V_{GS} = 2.5V$
- Lead free and Green Device Available
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management

Pin Description



NO.	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE



Absolute Maximum Ratings

(@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units	
V_{DS}	Drain-to-Source Voltage	20	V	
V_{GS}	Gate-to-Source Voltage	± 12	V	
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	90	A
		$T_C=100^\circ\text{C}$	57	
I_{DM}	Pulsed Drain Current ⁽¹⁾	360	A	
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	156	mJ	
P_D	Power Dissipation	$T_C=25^\circ\text{C}$	54	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽²⁾	32	$^\circ\text{C}/\text{W}$	
$R_{\theta JC}$	Thermal Resistance, Junction to Case ⁽³⁾	2.32	$^\circ\text{C}/\text{W}$	
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$	



Electrical Characteristics

($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}, V_{GS}=0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 12\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.6	0.9	1.3	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS}=4.5\text{V}, I_D=30\text{A}$	-	2.2	3.6	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_D=20\text{A}$	-	2.9	4.9	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=10\text{V}, f=1\text{MHz}$	-	3476	-	pF
C_{oss}	Output Capacitance		-	528	-	pF
C_{rss}	Reverse Transfer Capacitance		-	464	-	pF
Q_g	Total Gate Charge	$V_{GS}=0\sim 8\text{V}, V_{DS}=10\text{V}, I_D=30\text{A}$	-	65	-	nC
Q_{gs}	Gate Source Charge		-	8	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	12	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DD}=10\text{V}, I_D=30\text{A}, R_{GEN}=3\Omega$	-	8	-	ns
t_r	Turn-On Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	73	-	ns
t_f	Turn-Off Fall Time		-	80	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	90	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	360	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=20\text{A}, di/dt=100\text{A}/\mu\text{s}$	-	16	-	ns
Q_{rr}	Reverse Recovery Charge		-	5.6	-	nC

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=10\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=25\text{A}$.

3. $R_{\theta JA}$ is measured with the device mounted on a 1 inch² pad of 2oz copper FR4 PCB

4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



Typical Performance Characteristics

Figure 1: Output Characteristics

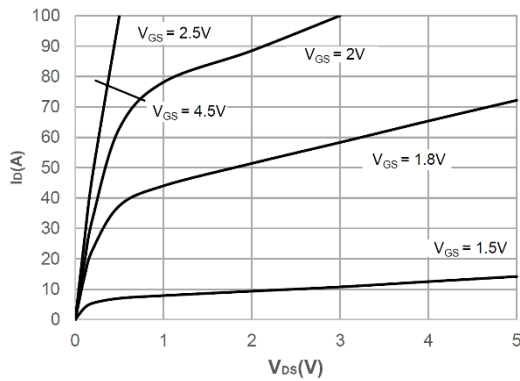


Figure 2: Typical Transfer Characteristics

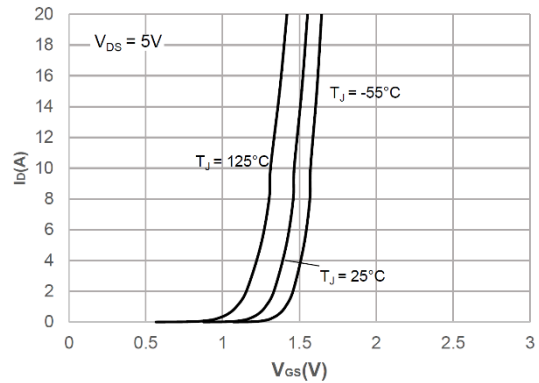


Figure 3: On-resistance vs. Drain Current

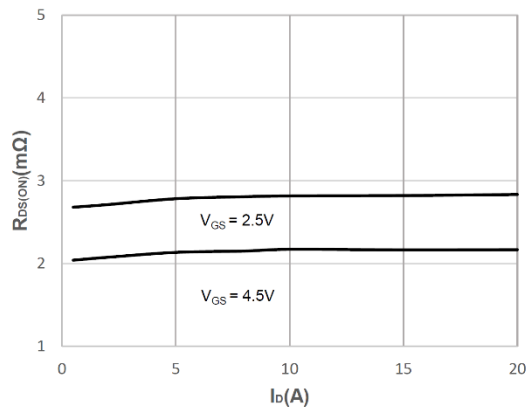


Figure 4: Body Diode Characteristics

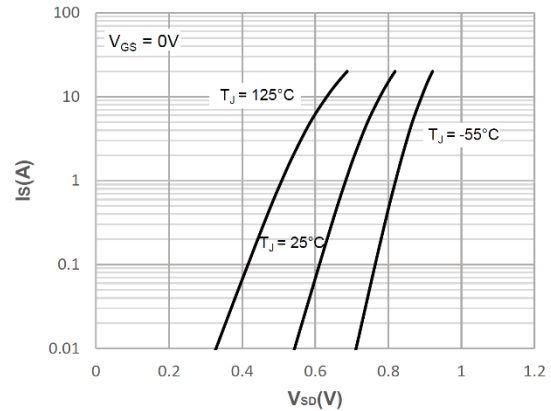


Figure 5: Gate Charge Characteristics

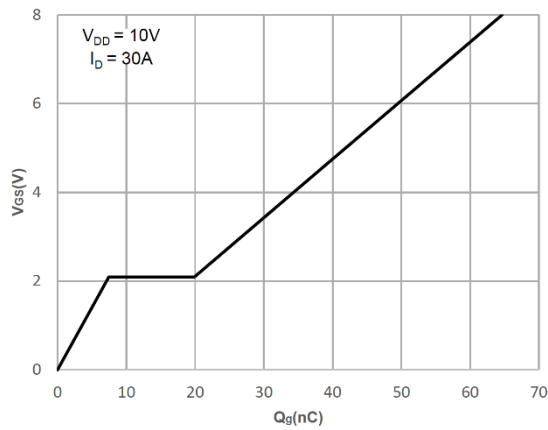


Figure 6: Capacitance Characteristics

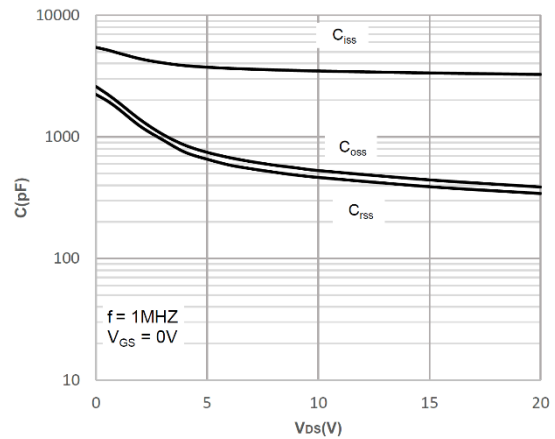


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

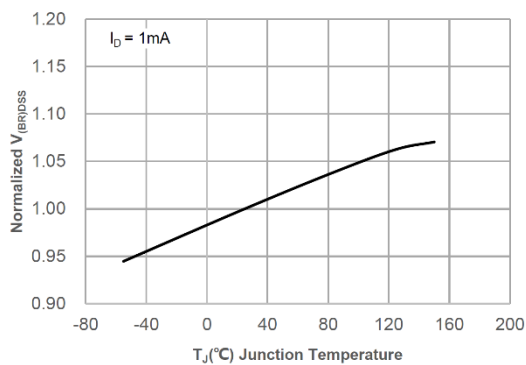


Figure 8: Normalized on Resistance vs. Junction Temperature

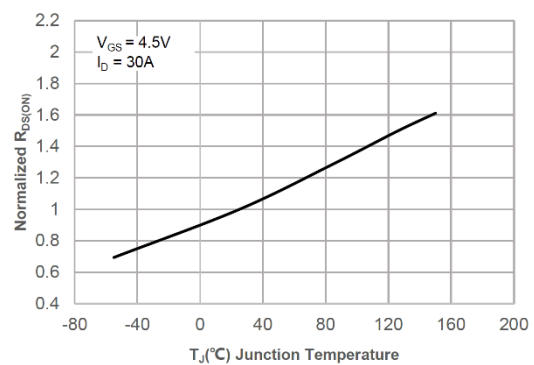




Figure 9: Maximum Safe Operating Area

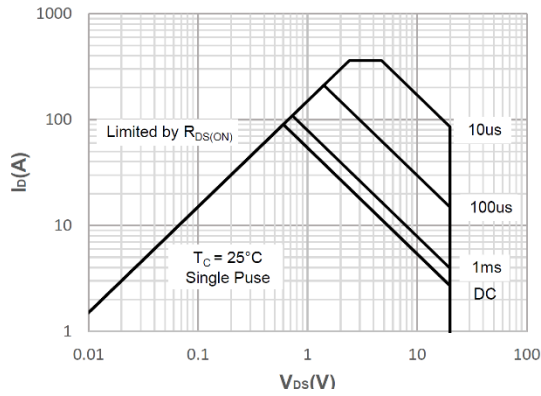


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

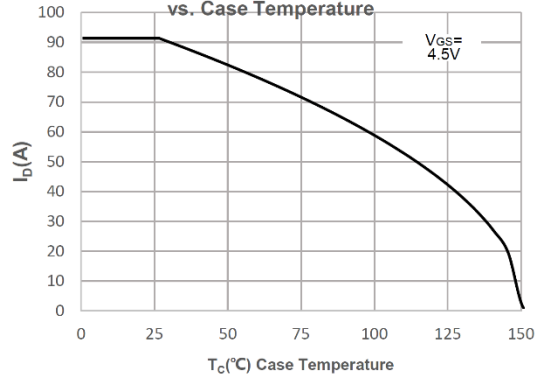


Figure 11: Normalized Maximum Transient Thermal Impedance

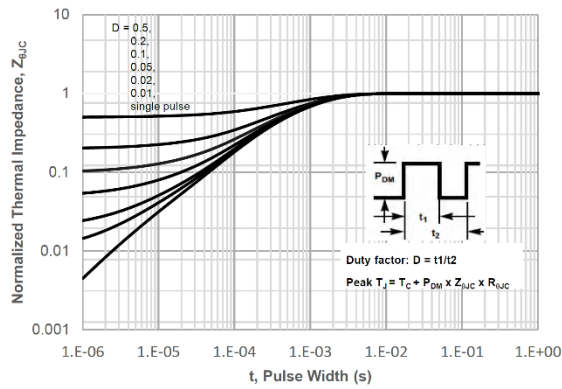
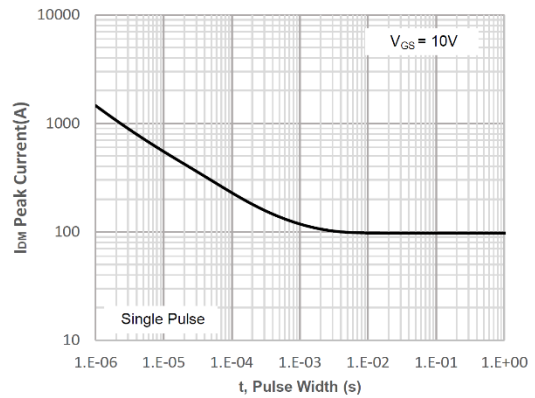


Figure 12: Peak Current Capacity





Test Circuit

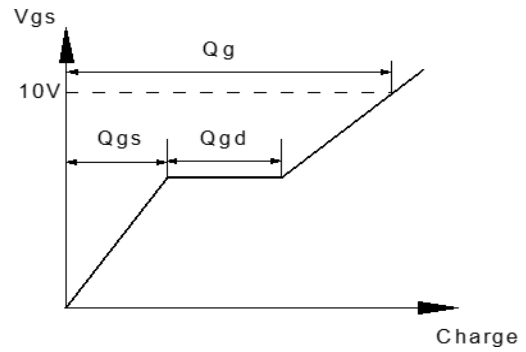
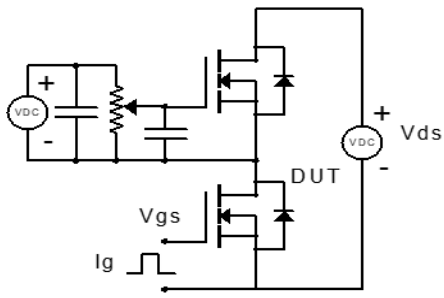


Figure 1: Gate Charge Test Circuit & Waveform

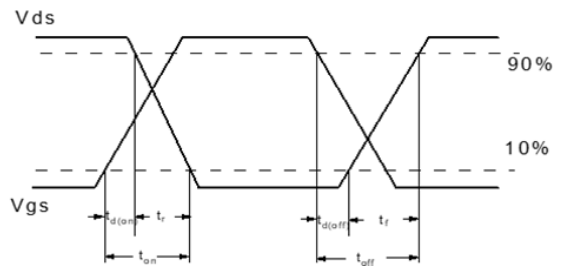
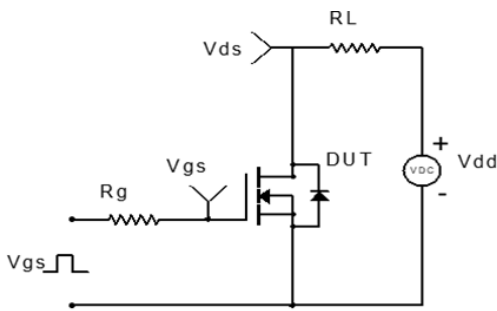


Figure 2: Resistive Switching Test Circuit & Waveform

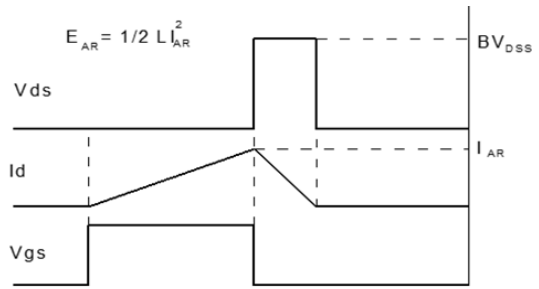
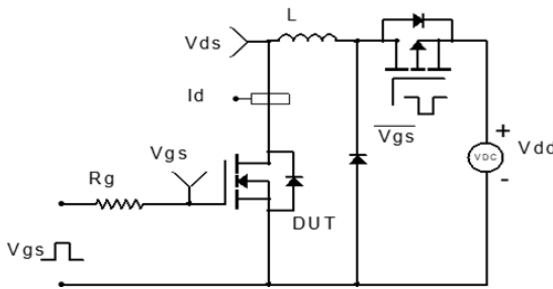


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

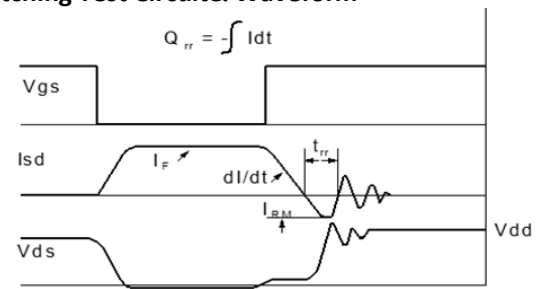
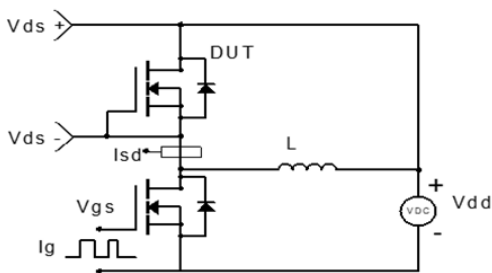
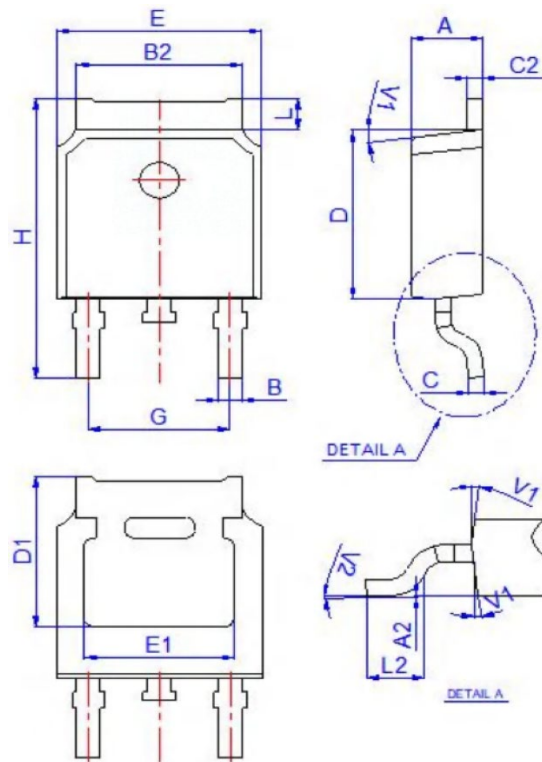


Figure 4: Diode Recovery Test Circuit & Waveform



Package Mechanical Data(TO-252-3L)



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.10	2.50	0.083	0.098
A2	0	0.10	0	0.004
B	0.66	0.86	0.026	0.034
B2	5.18	5.48	0.202	0.216
C	0.40	0.60	0.016	0.024
C2	0.44	0.58	0.017	0.023
D	5.90	6.30	0.232	0.248
D1	5.30 REF		0.209 REF	
E	6.40	6.80	0.252	0.268
E1	4.63		0.182	
G	4.47	4.67	0.176	0.184
H	9.50	10.70	0.374	0.421
L	1.09	1.21	0.043	0.048
L2	1.35	1.65	0.053	0.065
V1	7°		7°	
V2	0°	6°	0°	6°

Ordering information

Order Code	Package	V _{DS} (V)	I _D (A)	R _{DS(ON)} (m Ω)	
QND120N02AJ	TO-252	20	90	V _{GS} =4.5V	2.2
				V _{GS} =2.5V	2.9