



QNHCHIP

QN4838

Product Specification

QN4838

30V Dual N-Channel MOSFET



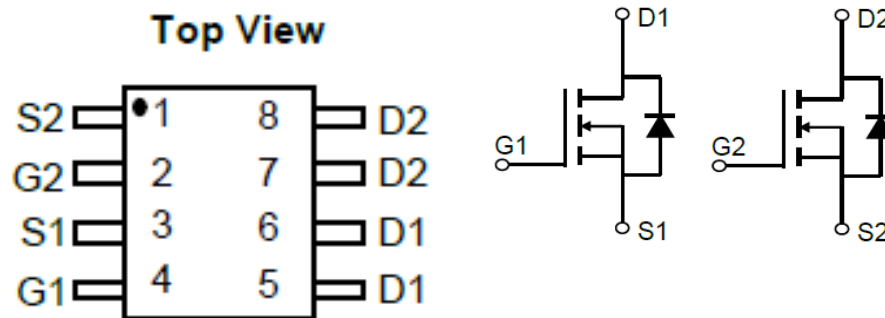
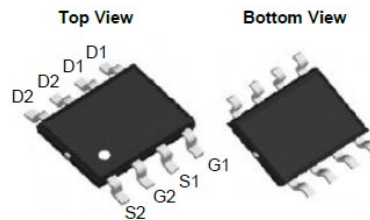
FEATURES

- 30V, 12A
 $R_{DS(ON)}$ Typ= 11m Ω @ $V_{GS} = 10V$
 $R_{DS(ON)}$ Typ= 15.5m Ω @ $V_{GS} = 4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

- Load Switch
- PWM Application
- Power Management

Pin Description



Schematic Diagram

NO.	Symbol	Description
1	S2	SOURCE 2
2	G2	GATE 2
3	S1	SOURCE 1
4	G1	GATE 1
5	D1	DRAIN 1
6	D1	DRAIN 1
7	D2	DRAIN 2
8	D2	DRAIN 2



Absolute Maximum Ratings

(@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_A=25^\circ\text{C}$	12
		$T_A=100^\circ\text{C}$	8
I_{DM}	Pulsed Drain Current ⁽¹⁾	48	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	36	mJ
P_D	Power Dissipation	$T_A=25^\circ\text{C}$	1.9
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	66	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$



Electrical Characteristics

($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.1	1.3	2.2	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 12\text{A}$	-	11	12.3	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$	-	15.5	20.5	$\text{m}\Omega$
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f = 1\text{MHz}$	-	799	-	pF
C_{oss}	Output Capacitance		-	96	-	pF
C_{rss}	Reverse Transfer Capacitance		-	80	-	pF
Q_g	Total Gate Charge	$V_{GS}=0\sim 10\text{V}, V_{DD}=15\text{V}, I_D=12\text{A}$	-	16	-	nC
Q_{gs}	Gate Source Charge		-	4	-	nC
Q_{gd}	Gate Drain ("Miller") Charge		-	4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DD}=15\text{V}, I_D=12\text{A}, R_{GEN}=3\Omega$	-	6	-	ns
t_r	Turn-On Rise Time		-	16	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	17	-	ns
t_f	Turn-Off Fall Time		-	5	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	12	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	48	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}, I_S=12\text{A}$	-	-	1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F=12\text{A}, di/dt=100\text{A}/\mu\text{s}$	-	9	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	3	-	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2. E_{AS} condition: Starting $T_J=25^\circ\text{C}$, $V_{DD}=15\text{V}$, $V_G=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=12\text{A}$
3. $R_{\theta JA}$ is measured with the device mounted on a 1 inch² pad of 2oz copper FR4 PCB
4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



Typical Performance Characteristics

Figure 1: Output Characteristics

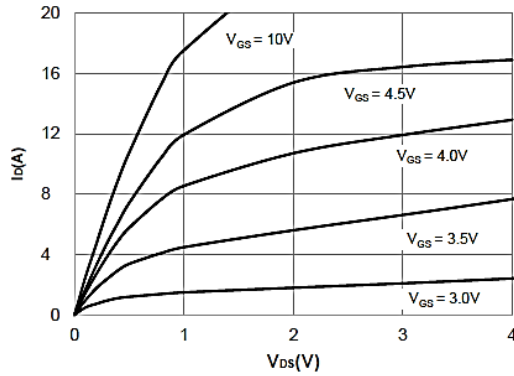


Figure 2: Typical Transfer Characteristics

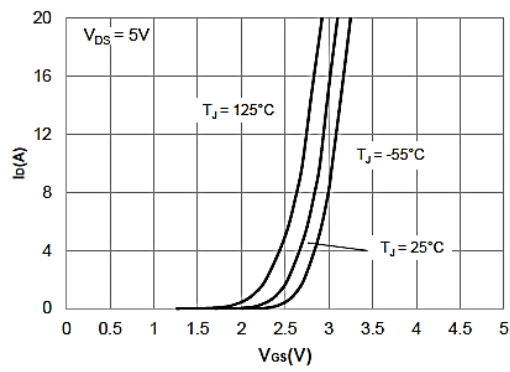


Figure 3: On-resistance vs. Drain Current

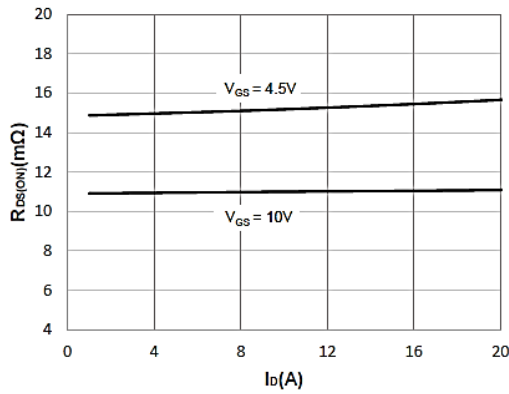


Figure 4: Body Diode Characteristics

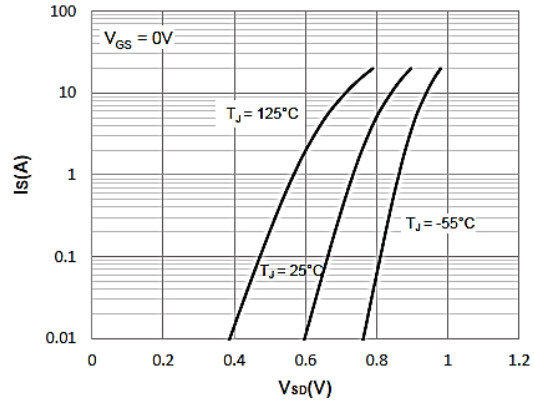


Figure 5: Gate Charge Characteristics

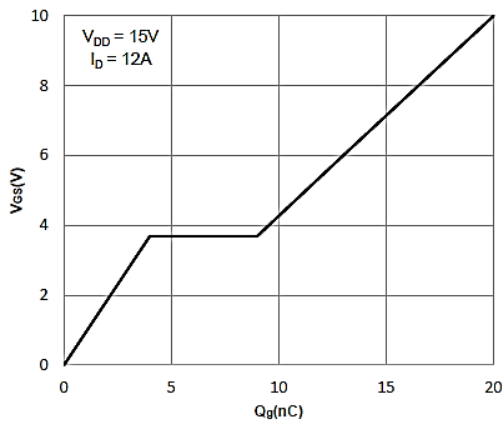


Figure 6: Capacitance Characteristics

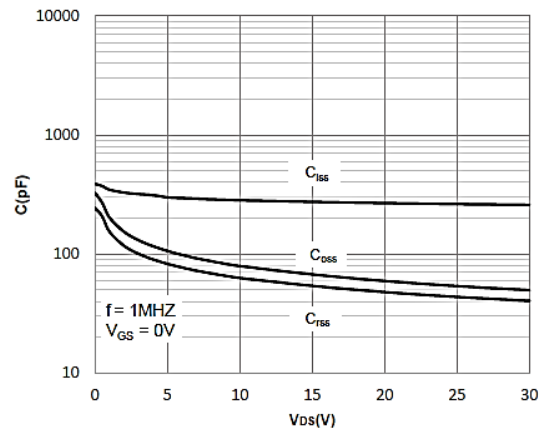


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

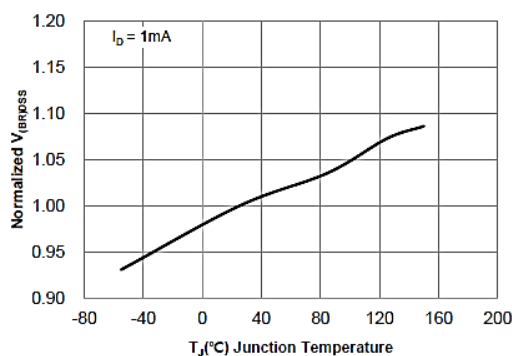


Figure 8: Normalized on Resistance vs. Junction Temperature

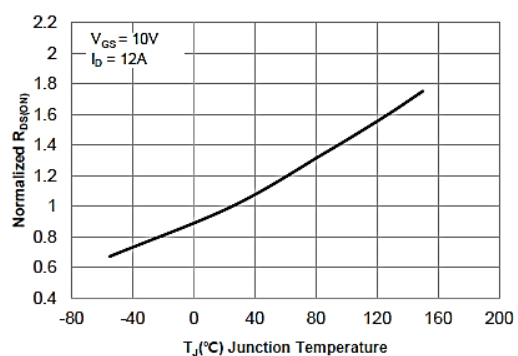




Figure 9: Maximum Safe Operating Area

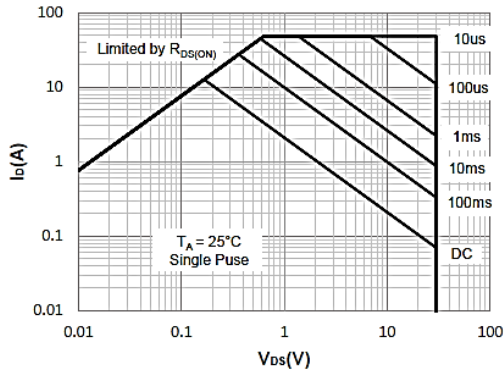


Figure 10: Maximum Continuous Driian Current vs. Ambient Temperature

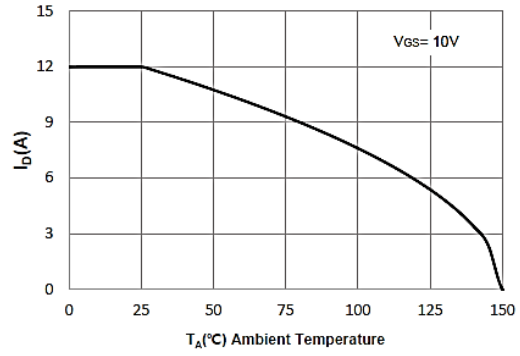


Figure 11: Normalized Maximum Transient Thermal Impedance

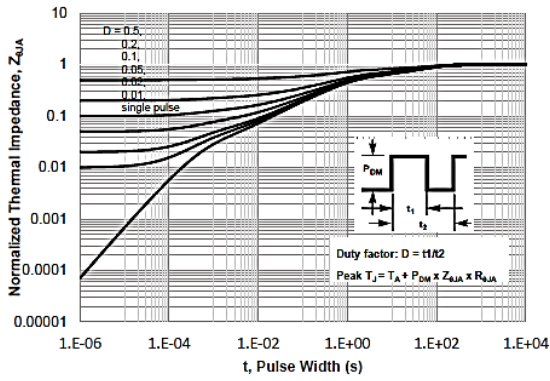
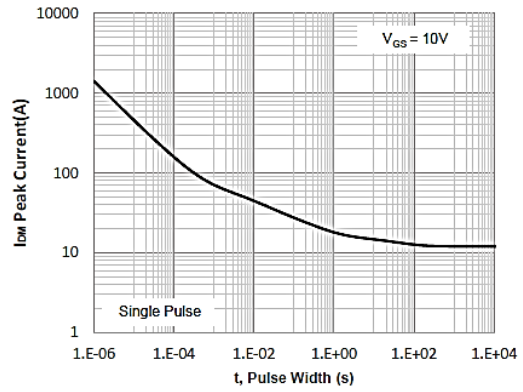


Figure 12: Peak Current Capacity





Test Circuit

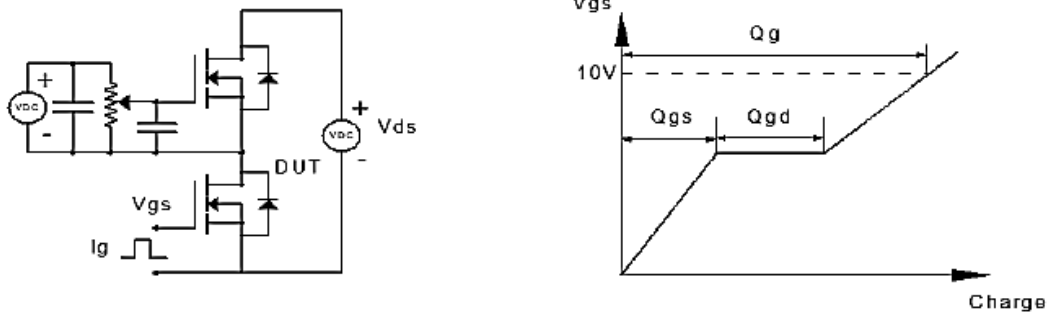


Figure 1: Gate Charge Test Circuit & Waveform

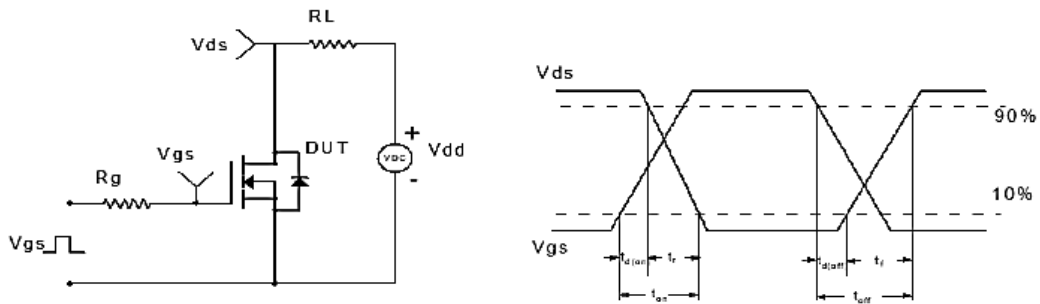


Figure 2: Resistive Switching Test Circuit & Waveform

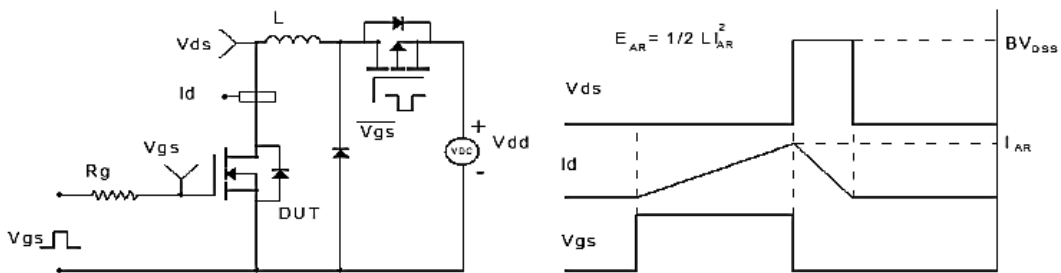


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

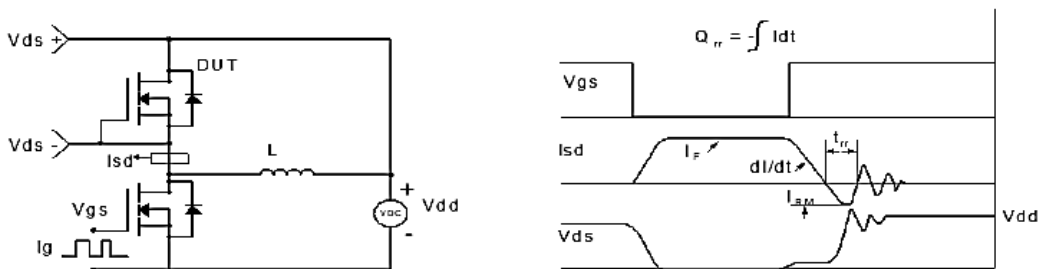
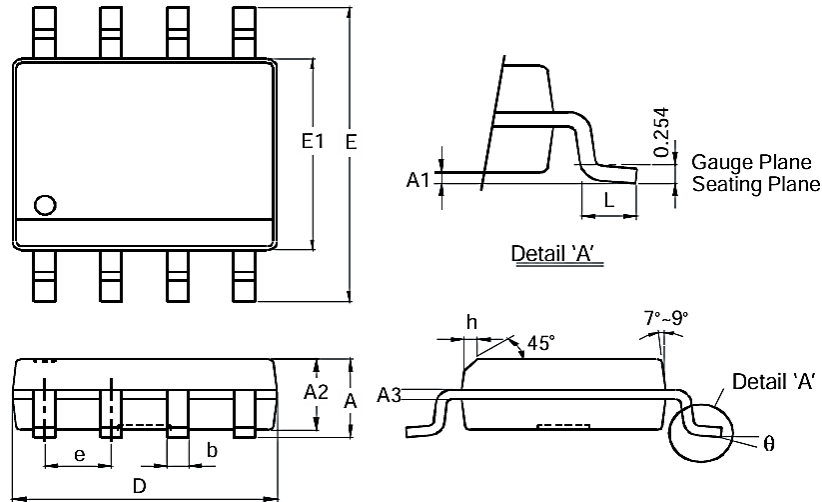


Figure 4: Diode Recovery Test Circuit & Waveform



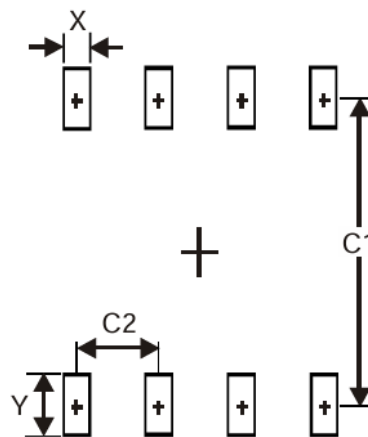
Package Mechanical Data

SOP-8



Dim	Min(mm)	Max(mm)
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°

suggested Pad Layout



Dimensions	Value(mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27



Ordering information

Order Code	Package	V _{DS} (V)	I _D (A)	R _{DS(ON)} (m Ω)	
QN4838	SOP-8	30	12	V _{GS} =10V	11
				V _{GS} =4.5V	15.5