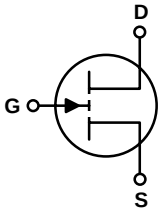
INN200EQ080A

1. General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in En-FCQFN with 3.0 mm x 5.0 mm package size.

2. Features

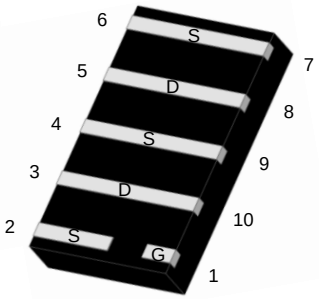


- GaN-on-Silicon E-mode HEMT technology
- Topside Cooling En-FCQFN
- Very low gate charge
- Ultra-low on resistance
- Very small footprint

3. Applications

- High frequency DC-DC converter
- Wireless Power
- AC/DC Chargers
- Mobile power bank
- Class D audio

Top view



Bottom view

4. Key performance parameters

Table 1 Key performance parameters at T_J = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	200	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	8	mΩ
$Q_{G,typ}$ @ V_{DS} = 100V	11	nC
$I_{DS,Pulse}$(T_J = 25 °C)	120	A
Q_{OSS} @ V_{DS} = 100V	86	nC

5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
1	Gate	Driver Gate
2,4,6,7,9	Source	Source
3,5,8,10	Drain	Power Drain

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN200EQ080A	En-FCQFN 3X5	P02

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6. Maximum ratings

at T_J = 25 °C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
$V_{DS(tr)}$	Drain-to-Source Voltage [1] (V_{GS} = 0 V, 1h total time, $T_A = T_{JMAX}$)	240	V
I_D	Continuous current (V_{GS} = 5 V, T_C=25 °C, $R_{\theta JC}$ = 0.36°C/W)	120	A
	Continuous current (V_{GS} = 5 V, T_C=100 °C, $R_{\theta JC}$ = 0.36°C/W)	85	A
	Continuous current (V_{GS} = 5 V, T_A=25 °C, $R_{\theta JA}$ = 37.53°C/W)	13	A
	Pulsed(T_J = 25°C, T_{Pulse} = 100 µs)	120	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	°C

Note:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation;

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.36	°C/W	-
$R_{\theta JB}$	Thermal Resistance, Junction to Board	2.08	°C/W	-
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [2]	37.53	°C/W	-
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL3

Note:

2. $R_{\theta JA}$ is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.

8. Electric characteristics

at T_J = 25 °C, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{DSS}	Drain Source Leakage	-	1.5	100	uA	V_{GS} = 0 V, V_{DS} = 200 V
I_{GSS}	Gate-to-Source Forward Leakage	-	1.5	100	uA	V_{GS} = 5 V
	Gate-to-Source Forward Leakage	-	4	1000	uA	V_{GS} = 6 V
	Gate-to-Source Reverse Leakage	-	0.1	100	uA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.1	V	V_{DS} = V_{GS}, I_D = 6.5 mA
$R_{DS(on)}$	Drain-Source On-state Resistance [3]	-	6	8	mΩ	V_{GS} = 5 V, I_D = 20 A
V_{SD}	Source-Drain Forward Voltage	-	1.5	-	V	I_S = 5 A, V_{GS} = 0 V

Note:

3. $R_{DS(on)}$ is measured without prior drain bias or switching stress.

Table 7 Dynamic characteristics [4]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	1250	-	pF	V_{GS} = 0 V, V_{DS} = 100 V
C_{OSS}	Output Capacitance	-	550	-		V_{GS} = 0 V, V_{DS} = 100 V
C_{RSS}	Reverse Transfer Capacitance	-	7	-		V_{GS} = 0 V, V_{DS} = 100 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	660	-		V_{GS} = 0 V, V_{DS} = 0 V to 100 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	760	-		V_{GS} = 0 V, V_{DS} = 0 V to 100 V
R_G	Gate resistance	-	2	-	Ω	f = 5 MHz, open drain
Q_G	Total Gate Charge	-	11	14	nC	V_{GS} = 5 V, V_{DS} = 100 V, I_D=20 A
Q_{GS}	Gate to Source Charge	-	2.5	-		V_{DS} = 100 V, I_D=20 A
Q_{GD}	Gate to Drain Charge	-	2	-		V_{DS} = 100 V, I_D=20 A
$Q_{G(TH)}$	Gate Charge at Threshold	-	1.5	-		V_{DS} = 100 V, I_D=20 A
Q_{OSS}	Output Charge	-	86	-		V_{GS} = 0 V, V_{DS} = 100 V
Qrr	Reverse recovery charge	-	0	-		V_{DS} = 0V, I_S = 20A

Note:

4. Defined by design. Not subject to production test.

9. Electric characteristics diagrams

at T_J = 25 °C, unless specified otherwise

Fig. 1 Typical Output Characteristics (T_J=25°C)

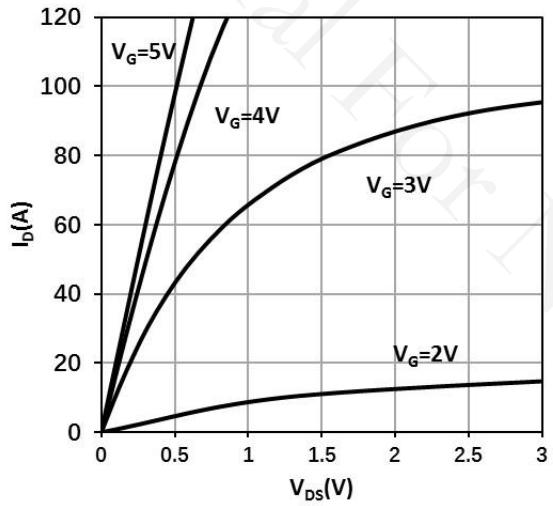


Fig. 2 Typical Output Characteristics (T_J=125°C)

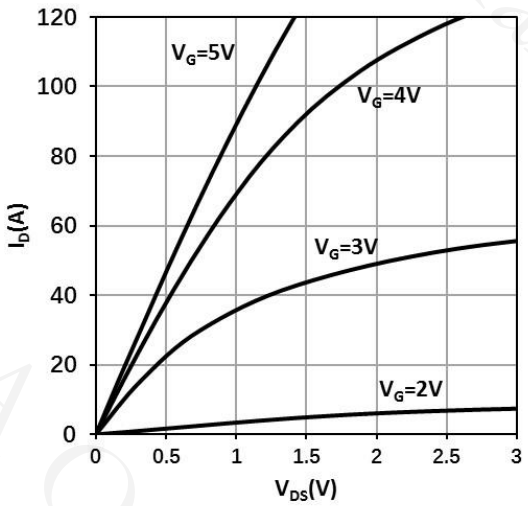


Fig. 3 Typical Drain On-state Resistance (T_J=25°C)

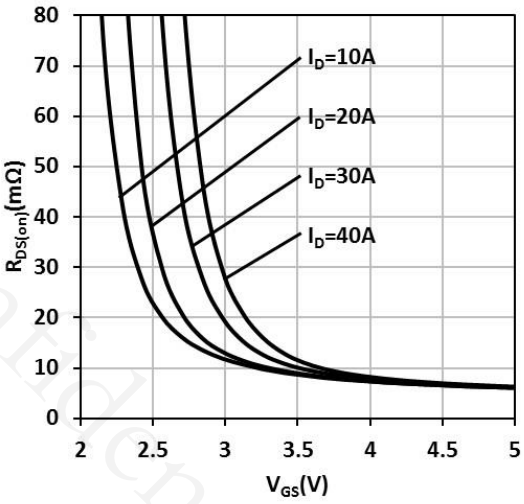


Fig. 4 Typical Drain On-state Resistance (T_J=125°C)

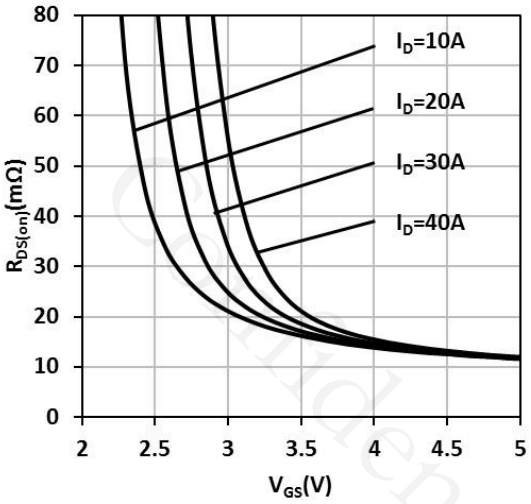


Fig. 5 Normalized On-State Resistance vs. Temp.

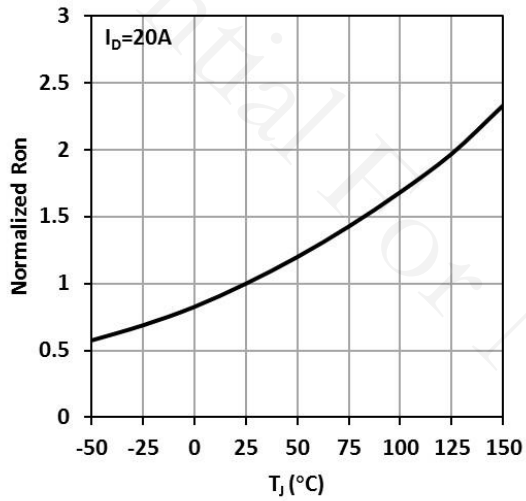


Fig. 6 Typical Transfer Characteristics

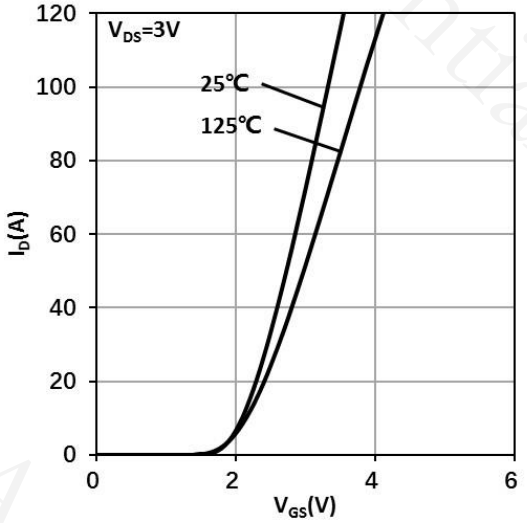


Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0, T_J$=25°C)

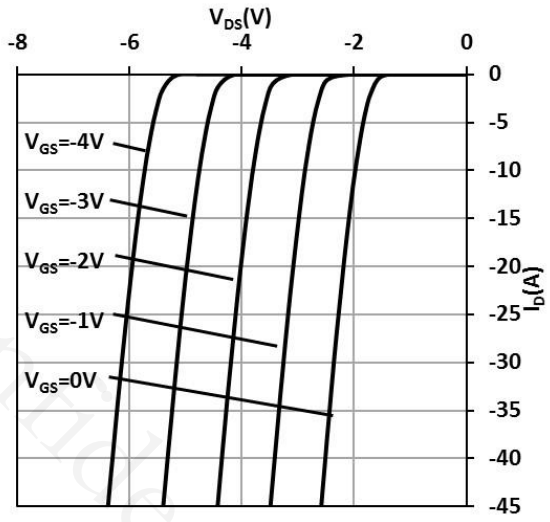


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0, T_J$=25°C)

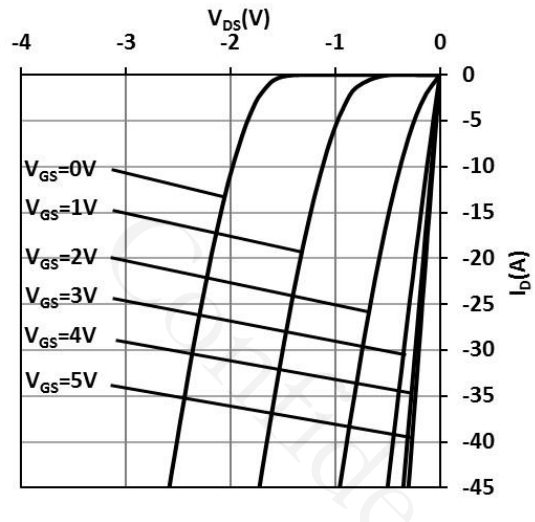


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0$, T_J=125°C)

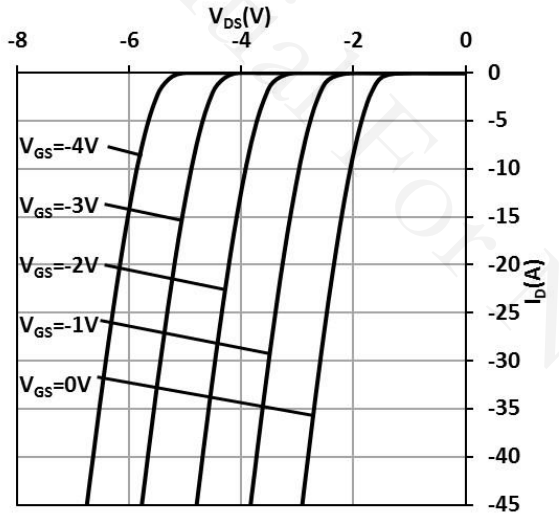


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0$, T_J=125°C)

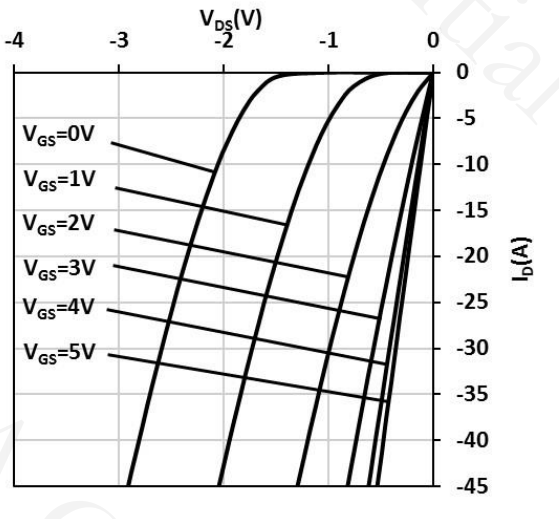


Fig. 11 Typ. Capacitances Characteristics

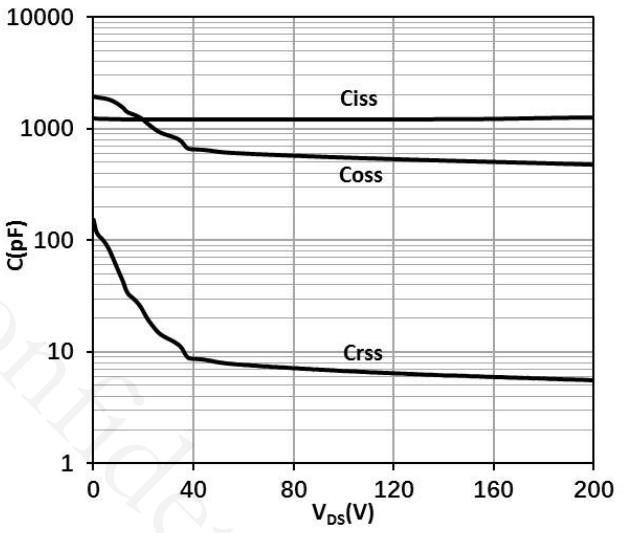


Fig. 12 Typ. Gate Charge

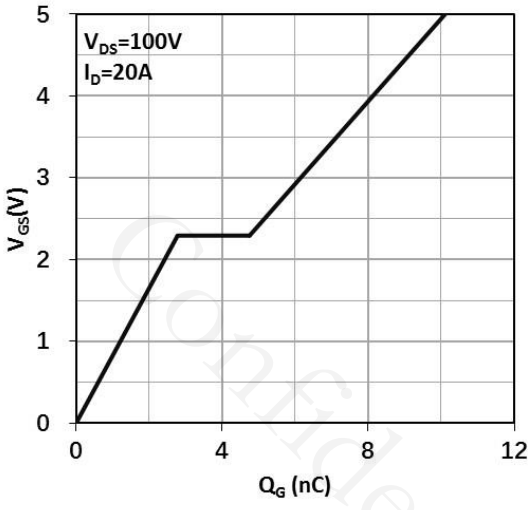


Fig. 13 Normalized Threshold Voltage vs. Temp.

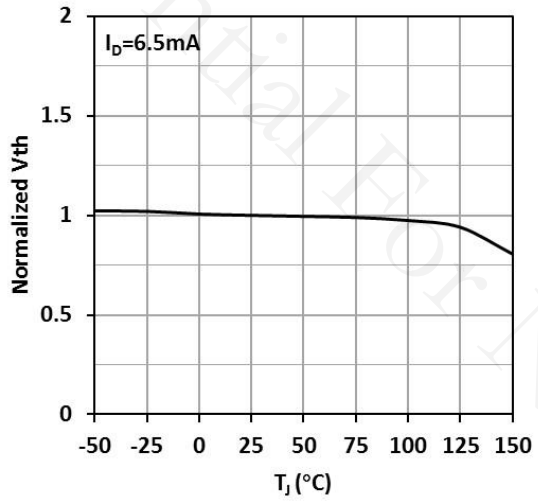


Fig. 14 Output Charge

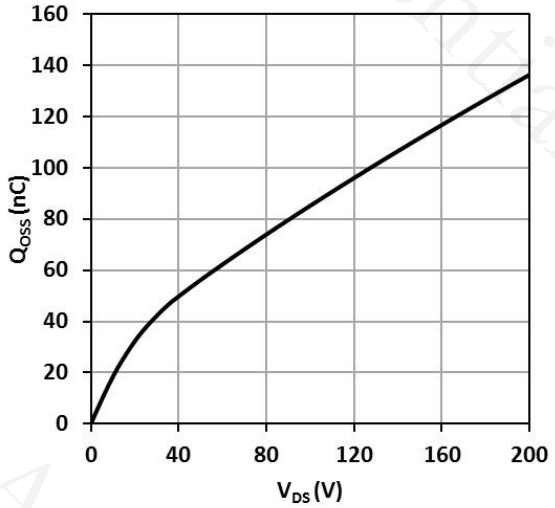


Fig. 15 Output Capacitance Stored Energy

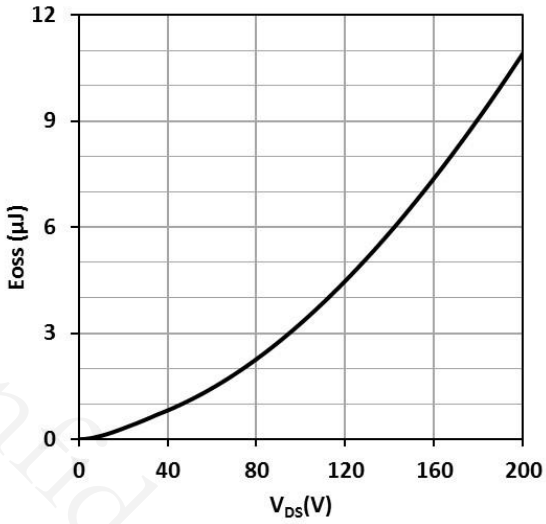


Fig. 16 Power Dissipation

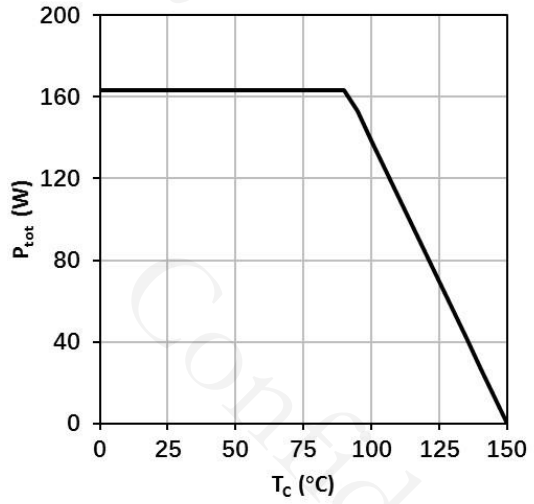


Fig. 17 Safe Operating Area

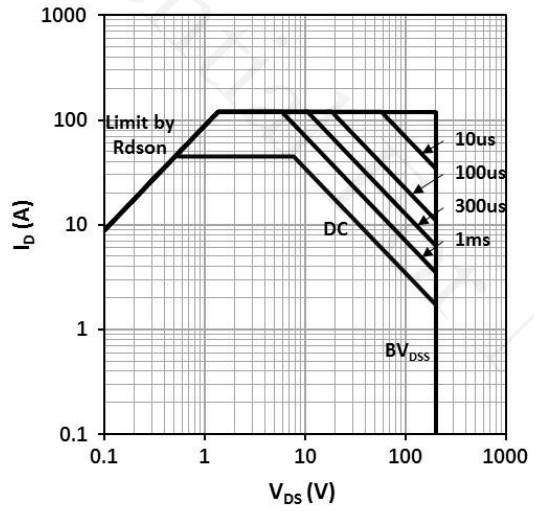
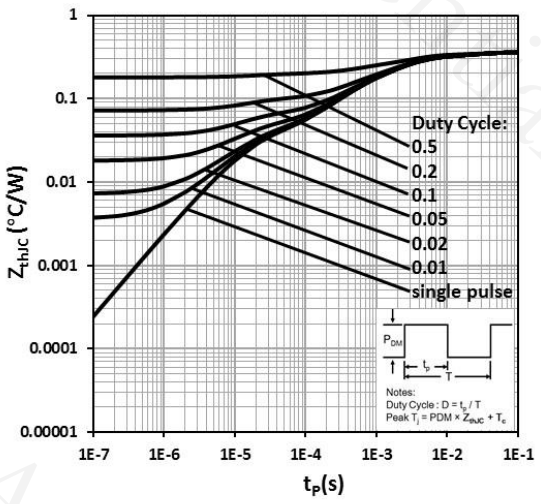
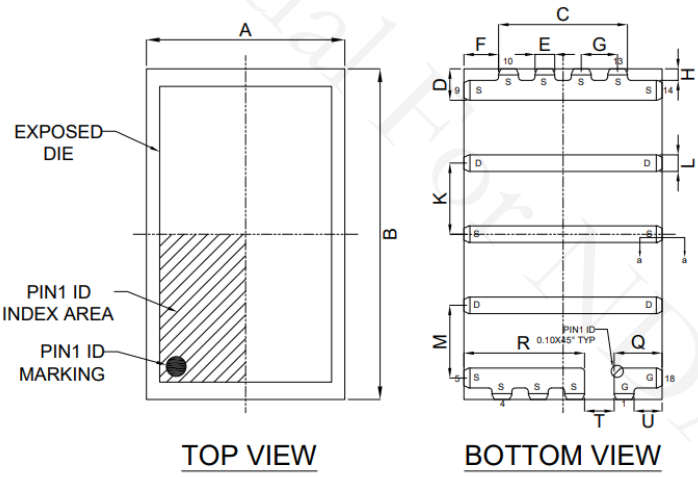


Fig. 18 Max. Transient Thermal Impedance

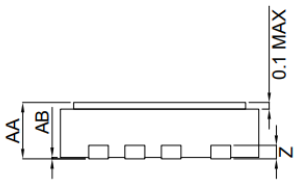


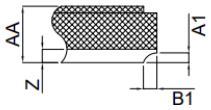
10. Package Outlines

Package Reference



SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	2.9	3.0	3.1	
B	4.9	5.0	5.1	
C	1.85	1.95	2.05	
D	0.375	0.475	0.575	4X
E	0.25	0.30	0.35	12X
F	0.525 REF			2X
G	0.550 BASIC			5X
H	0.175 REF			4X
K	1.075 BASIC			4X
L	0.20	0.25	0.30	6X
M	1.100 BASIC			4X
Q	0.625	0.725	0.825	
R	1.725	1.825	1.925	
T	0.40	0.45	0.50	
U	0.425 REF			2X
Z	0.203 REF			
AA	0.75	0.85	0.95	
AB	0.00	0.02	0.05	
A1	0.075	-	0.18	
B1	0.01	-	0.09	

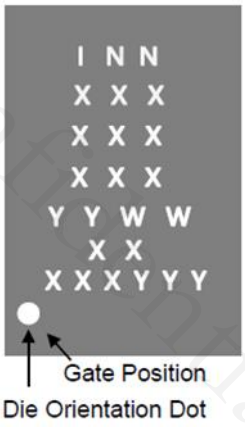




NOTE:

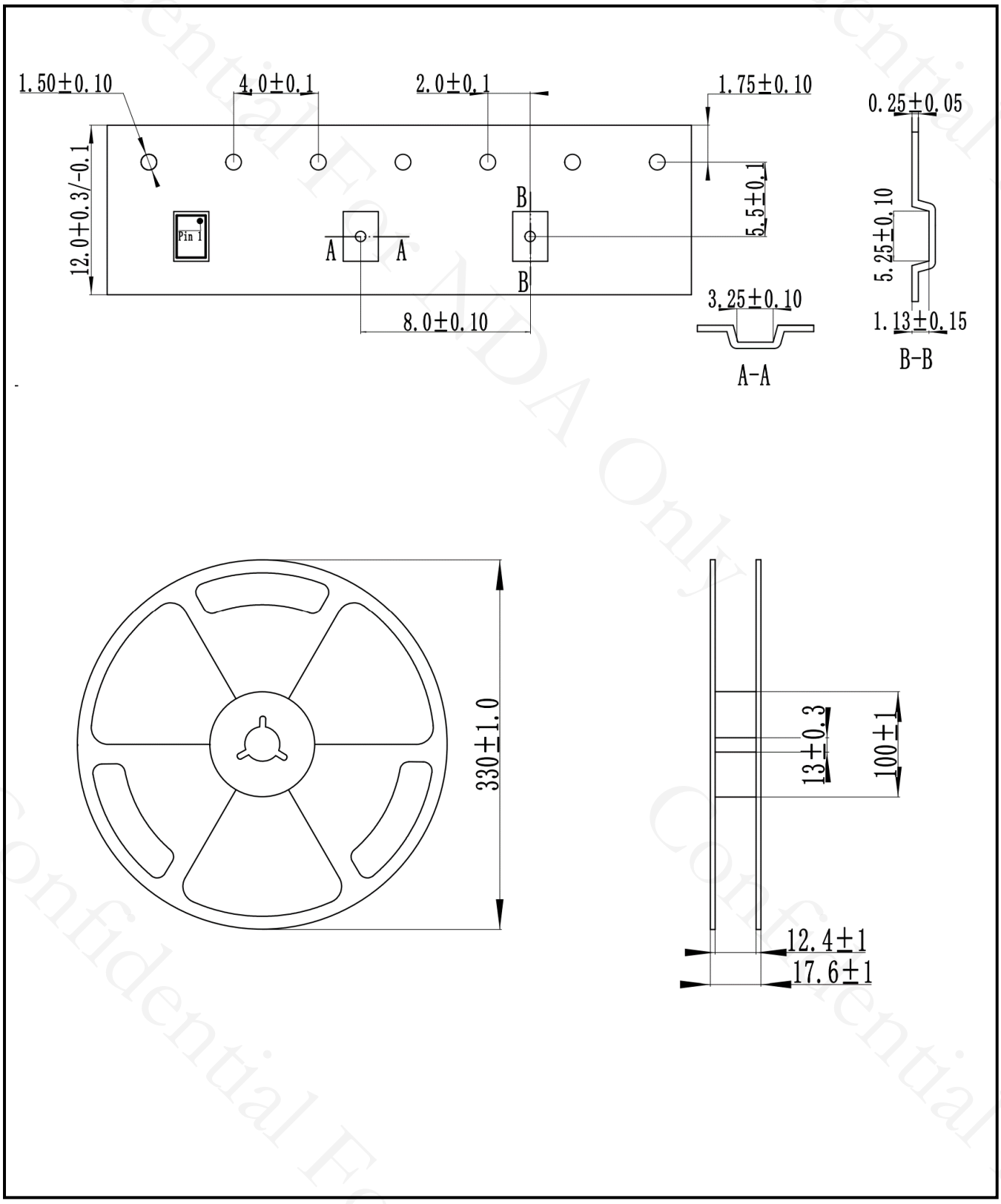
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

Marking Reference：



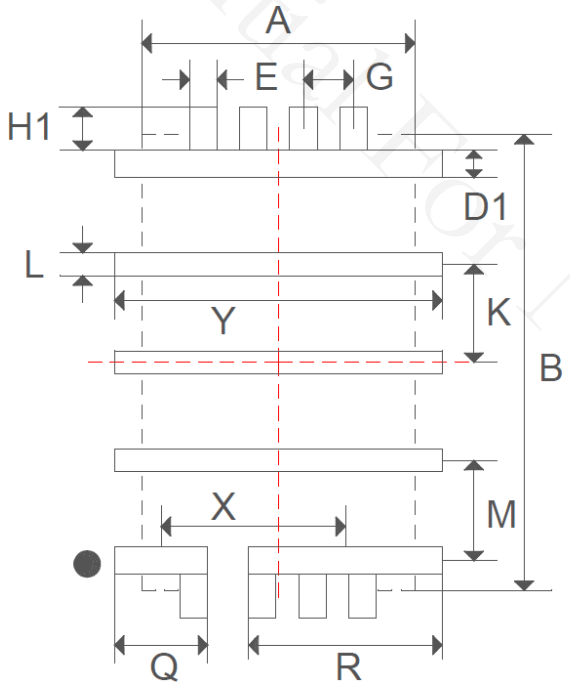
Row	Description	Example
Row1	Company name	INN
Row2	Product code	XXX
Row3	Lot Code	XXX
Row4		XXX
Row5	Date code	YYWW
Row6	Wafer ID	XX
Row7	Location ID	XXXYYY

11. Reel information



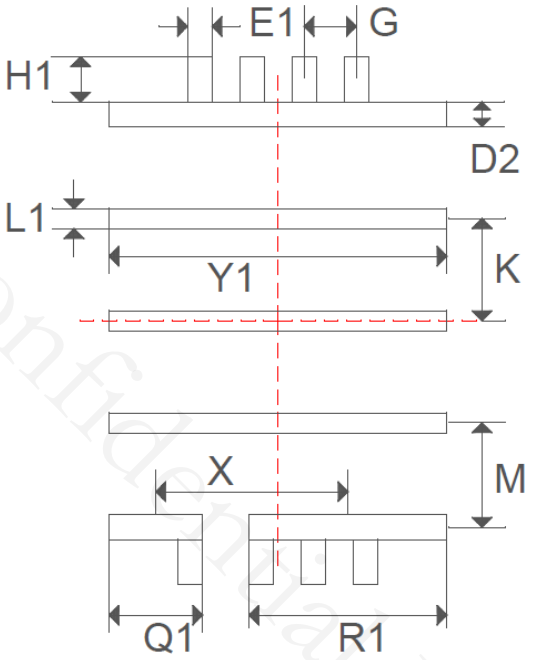
12. Land pattern

Recommended land pattern



Symbol	Millmeter	Note
A	3.0	
B	5.0	
D1	0.3	3X
E	0.3	8X
G	0.55	5X
H1	0.475	8X
K	1.075	2X
L	0.25	3X
M	1.1	3X
Q	1.025	
R	2.125	
X	2.025	
Y	3.6	4X

Recommended Stencil drawing



Symbol	Millmeter	Note
D2	0.26	3X
E1	0.26	8X
G	0.55	5X
H1	0.475	8X
K	1.075	2X
L1	0.21	3X
M	1.1	3X
Q1	0.985	
R1	2.085	
X	2.025	
Y1	3.56	4X

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.1	2023-12-12	Version V0.1 setup
0.2	2024-02-23	Update POD
0.5	2024-06-28	1. Update Dynamic characteristics 2. Add Electric characteristics diagrams 3. Add land pattern
0.9	2025-03-18	1. Update Dynamic characteristics 2. Update Electric characteristics diagrams 3. Update Reel information 4. Update Thermal characteristics 5. Add $V_{DS(tr)}$ in table 4.

Important Notice

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