200V Half-Bridge GaN Driver with Dual PWM Inputs

1. Features

- 200V Integrated Half Bridge Gate Driver
- 5V Tightly Regulated High-Side and Low-Side Driver Supplies with UVLO Protection
- Split Outputs for Adjustable Turn-On/-Off Speeds
- 2A Pullup and 4A Pulldown Driver Capability
- Dual PWM Logic Inputs with Interlocking
- Integrated Bootstrap Diode
- Fast Propagation Delay (25ns Typical)
- Excellent Delay Matching (1ns Typical)
- SW and PGND: DC/Transient up to ±5V
- 140uA Low Quiescent Current
- 15-Lead QFN 4mmx4mm Package

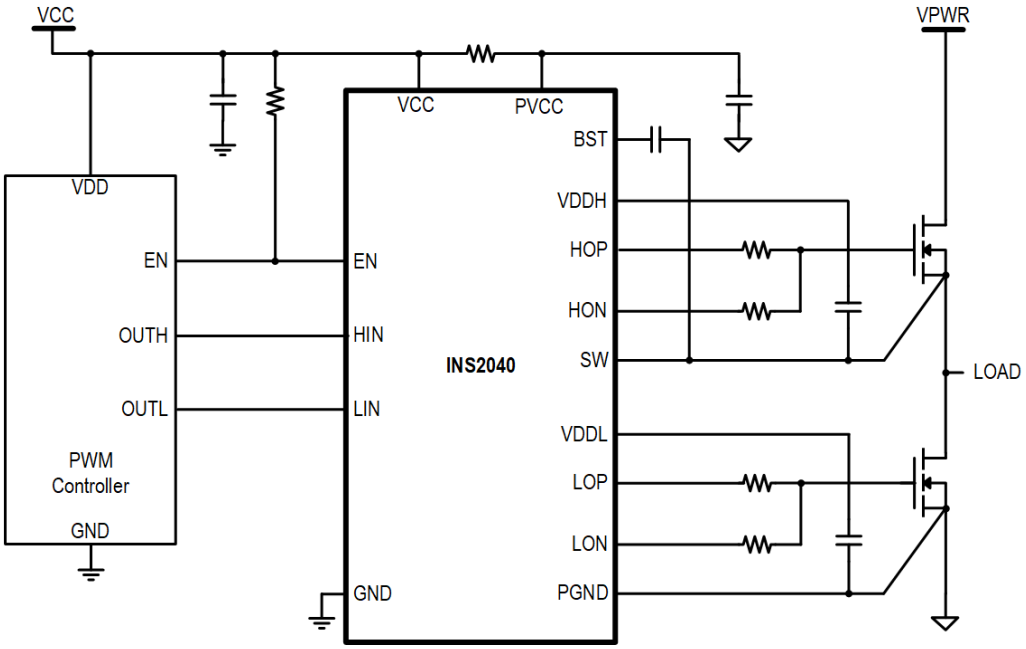
2. Applications

- High Voltage Half Bridge or Full Bridge Converters
- Totem Pole PFC, LLC, AHB, Active Clamp Flyback
- Motor Driver for Home Appliances, Factory Automation, and Industrial Inverters
- Battery Formation, Solar Micro Inverters

3. Description

The INS2040 is designed to drive both high-side and low-side GaN FETs in a half-bridge topology. It has two logic inputs to control high-side and low-side drivers with interlocking, and both drivers have split outputs to adjust turn-on and turn-off speeds separately. An 250V internal bootstrap diode charges the high-side bootstrap capacitor from PVCC when the low-side driver turns on. To protect the gate of the GaN FET against excessive voltage stress, both drivers employ a dedicated 5V LDO maintaining the same drive voltage accurately. Fast propagation delay and excellent delay matching is provided even though SW and PGND are separated with -5V to 200V and -5V to 5V common mode voltage range. INS2040 offers important protections including independent supply undervoltage lockout and over temperature protection. The strong driving capability and excellent delay matching make the INS2040 suitable for high power and high frequency applications.

4. Typical Application



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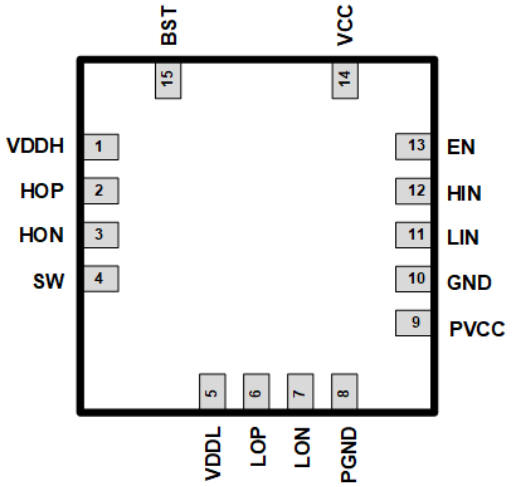
5. Revision history

Major changes since the last revision

Revision	Date	Description of changes
0.5	2024-09-20	Preliminary datasheet
0.8		Pre-release datasheet
1.0		Final release datasheet

6. Pin Configuration and Functions



15-Lead QFN (4mm x 4mm) Package – Top View

Pin Number	Pin Name	Description
1	VDDH	High-Side Driver Supply. Locally bypass this pin to SW with a ceramic capacitor.
2	HOP	High-Side Gate Driver Pullup Output. Connect to the gate of the high-side GaN FET. Use a resistor to adjust the turn-on speed.
3	HON	High-Side Gate Driver Pulldown Output. Connect to the gate of the high-side GaN FET. Use a resistor to adjust the turn-off speed.
4	SW	Switch Node and High-Side Gate Driver Return Pin.
5	VDDL	Low-Side Driver Supply. Locally bypass this pin to PGND with a ceramic capacitor.
6	LOP	Low-Side Gate Driver Pullup Output. Connect to the gate of the low-side GaN FET. Use a resistor to adjust the turn-on speed.
7	LON	Low-Side Gate Driver Pulldown Output. Connect to the gate of the low-side GaN FET. Use a resistor to adjust the turn-off speed.
8	PGND	Power Ground and Low-Side Gate Driver Return Pin.
9	PVCC	Dedicated Power Supply for Gate Drivers. Connect to VCC pin or an external voltage source. Locally bypass this pin to PGND with a ceramic capacitor.
10	GND	Signal Ground. Kelvin connects this pin to PGND.
11	LIN	Low-Side Gate Driver Control Input. This pin has an internal 333kΩ pulldown resistor.
12	HIN	High-Side Gate Driver Control Input. This pin has an internal 333kΩ pulldown resistor.
13	EN	Enable Pin. This pin has an internal 333kΩ pulldown resistor. If the EN pin is pulled down, the driver outputs are immediately disabled.
14	VCC	IC Supply. Locally bypass this pin to GND with a ceramic capacitor.
15	BST	High-Side Gate Driver Bootstrap Floating Supply. Locally bypass this pin to SW with a ceramic capacitor.

7. Absolute Maximum Ratings

All pins are referenced to GND pin unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device lifetime.

Parameter	Min	Max	Unit
BST Voltage	-0.3	248	V
SW Voltage	-6	220	V
PVCC Voltage	-0.3	28	V
(BST-SW) Voltage	-0.3	28	V
(VDDH-SW) Voltage	-0.3	7.5	V
HOP, HON Voltage	SW-0.3	VDDH+0.3	V
(PVCC-PGND) Voltage	-0.3	28	V
(VDDL-PGND) Voltage	-0.3	7.5	V
LOP, LON Voltage	PGND-0.3	VDDL+0.3	V
PGND Voltage	-6	6	V
VCC Voltage	-0.3	28	V
EN, HIN, LIN Voltage	-0.3	28	V
SW Node Slew Rate		200	V/ns
Operating Junction Temperature T_J	-40	150	˚C
Storage Temperature	-55	150	˚C

8. ESD Ratings

Parameter	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 (3)	±2000	V
Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (4)	±1000	V

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
SW Voltage	-5	200	V
(BST-SW) Voltage		25	V
(PVCC-PGND) Voltage	9.5	25	V
PGND Voltage	-5	5	V
VCC Voltage	9.5	25	V
EN, HIN, LIN Voltage	0	25	V
Operating Junction Temperature T_J	-40	125	˚C

10. Thermal Information

Symbol	Parameter	INS2040QC	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	TBA	˚C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top)	TBA	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	TBA	˚C/W

11. Electrical Characteristics

T_J = 25°C, VCC = PVCC = BST =15V, PGND = SW = GND, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Power Supply						
VCC quiescent current	I_{Q_VCC}		57	100	uA	EN = 0V, LIN = HIN = 0V
VCC operating current	I_{OP_VCC}		1	1.5	mA	$f_{LIN/HIN}$ = 500kHz
PVCC quiescent current	I_{Q_PVCC}		45	100	uA	EN = 0V, LIN = HIN = 0V
PVCC operating current	I_{OP_PVCC}		1.6	2.5	mA	f_{LIN} = 500kHz
VCC UVLO rising threshold	V_{UVR_VCC}	7.5	8.0	8.5	V	
VCC UVLO falling threshold	V_{UVF_VCC}	7.0	7.5	8.0	V	
VCC UVLO Hysteresis	V_{HYS_VCC}		0.5		V	
PVCC UVLO rising threshold	V_{UVR_PVCC}	6.0	6.5	7.0	V	
PVCC UVLO falling threshold	V_{UVF_PVCC}	5.5	6.0	6.5	V	
PVCC UVLO Hysteresis	V_{HYS_PVCC}		0.5		V	
Bootstrap Power Supply						
BST leakage current	I_{LKG_BST}			10	uA	BST = SW = 200 V
BST quiescent current	I_{Q_BST}		40	75	uA	EN = 5V, LIN = HIN = 0V
BST operating current	I_{OP_BST}		1.5	2.5	mA	f_{HIN} = 500kHz
BST UVLO rising threshold	V_{UVR_BST}	6.0	6.5	7.0	V	
BST UVLO falling threshold	V_{UVF_BST}	5.5	6.0	6.5	V	
BST UVLO Hysteresis	V_{HYS_BST}		0.5		V	
Bootstrap diode forward voltage			0.7 1.1		V V	I_{BST} = -100uA I_{BST} = -10mA
Gate Driver Power Supply						
VDDH−SW regulated voltage	V_{DDH}	4.75	5	5.25	V	0 mA < I_{LOAD} < 10 mA
VDDL−PGND regulated voltage	V_{DDL}	4.75	5	5.25	V	
VDDH UVLO rising threshold	V_{UVR_VDDH}	4.0	4.25	4.5	V	
VDDH UVLO falling threshold	V_{UVF_VDDH}	3.75	4	4.25	V	
VDDL UVLO rising threshold	V_{UVR_VDDL}	4.0	4.25	4.5	V	
VDDL UVLO falling threshold	V_{UVF_VDDL}	3.75	4	4.25	V	
Input Logic						
Input high level voltage threshold	V_{INH}	2.5			V	
Input low level voltage threshold	V_{INL}			0.8	V	
Input voltage hysteresis	V_{HYS_IN}		0.5		V	
Input pulldown resistance	R_{IN}		333		kΩ	
High-Side and Low-Side Gate Driver						
Output pull-up resistance	R_{UP}		1.5	3	Ω	I_{HOP} or I_{LOP} = -10mA
Output pull-down resistance	R_{DN}		0.5	1	Ω	I_{HON} or I_{LON} = 10mA
Output peak source current(1)	I_{OSRC}		2		A	C_{LOAD} = 200 pF, R_{GATE} = 1Ω
Output peak sink current(1)	I_{OSNK}		4		A	C_{LOAD} = 200 pF, R_{GATE} = 1Ω
Over Temperature Protection						

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Thermal shutdown rising threshold(1)	T_{SDR}	150	160		°C	
Thermal shutdown hysteresis(1)	T_{HYS}		50		°C	

12. Switching Characteristics

T_J = 25°C, VCC = PVCC = BST =15V, PGND = SW = GND, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Minimum input pulse width that changes the output(1)	T_{IPW}		5	10	ns	
Gate output rise time(1)	T_R		2	4	ns	C_L = 330pF, 10% to 90%
Gate output fall time(1)	T_F		1.5	3	ns	C_L = 330pF, 90% to 10%
Low-side turn-off propagation delay	T_{LPHL}		25	50	ns	LIN falling to LO falling
Low-side turn-on propagation delay	T_{LPLH}		25	50	ns	LIN rising to LO rising
High-side turn-off propagation delay	T_{HPHL}		25	50	ns	HIN falling to HO falling
High-side turn-on propagation delay	T_{HPLH}		25	50	ns	HIN rising to HO rising
Delay matching LO on and HO off(1)	T_{MON}		1	5	ns	
Delay matching LO off and HO on(1)	T_{MOFF}		1	5	ns	

(3) Not 100% tested and guaranteed by design.

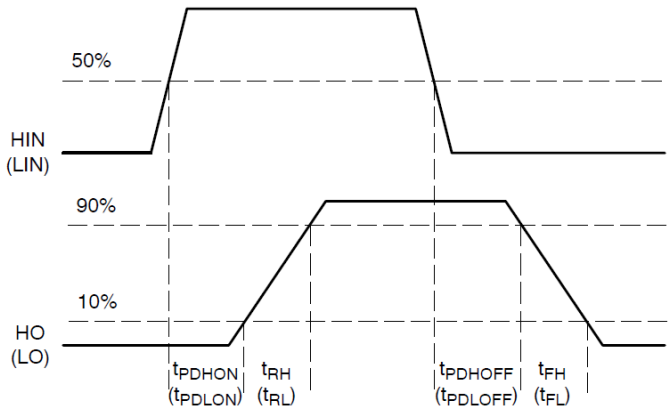


Fig. 1. Switching Timing Diagram

13. Typical Characteristics

Fig. 2. Supply Operating Current vs. Frequency, VCC=PVCC=BST=15V	Fig. 3. Supply Quiescent Current vs. Temperature
Fig. 4. Supply Operating Current vs. Temperature	Fig. 5. VCC UVLO Thresholds vs. Temperature
Fig. 6. PVCC UVLO Thresholds vs. Temperature	Fig. 7. BST UVLO Thresholds vs. Temperature

Fig. 8. BST Leakage Current vs. Temperature	Fig. 9. VDDH-SW regulated voltage vs. Temperature
Fig. 10. VDDL-PGND regulated voltage vs. Temperature	Fig. 11. VDDH UVLO Thresholds vs. Temperature
Fig. 12. Input Logic Thresholds vs. Temperature	Fig. 13. Input Logic Pulldown Resistance vs. Temperature

Fig. 14. LOP/LON (HOP/HON) Resistance vs. Temperature	Fig. 15. LIN to LOP Propagation Delay vs. Temperature
Fig. 16. HIN to HOP Propagation Delay vs. Temperature	Fig. 17. Propagation Delay Matching vs. Temperature
Fig. 18. LOP Rise Time and LON Fall Time vs. Temperature	Fig. 19. HOP Rise Time and HON Fall Time vs. Temperature

14. Block Diagram

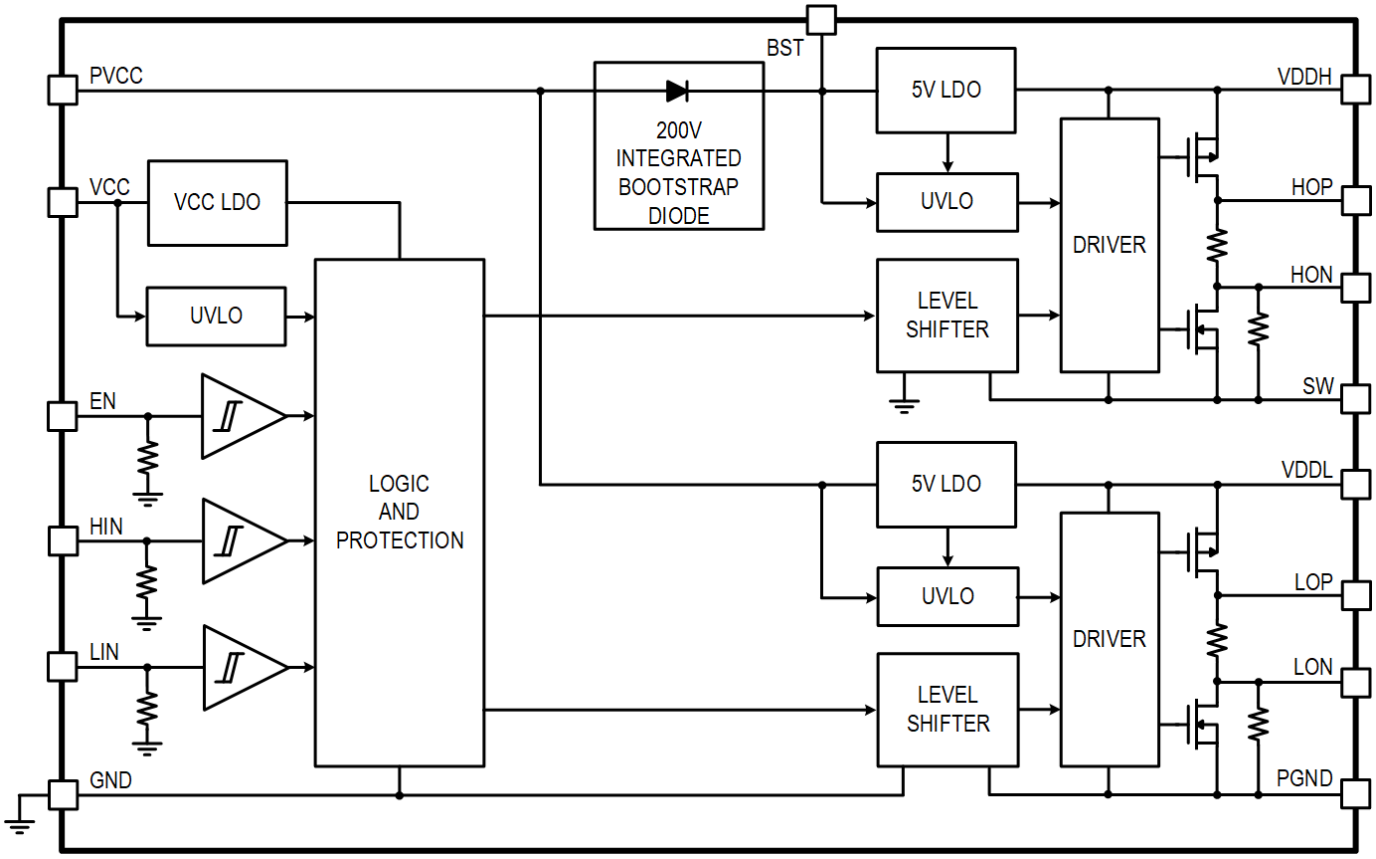


Fig. 20. Block Diagram

15. Function Description

The INS2040 is a high-performance, half-bridge gate driver designed to drive high-side and low-side GaN FETs. The high-side GaN FET and the low-side GaN FET are driven by the split outputs of HOP and HON and LOP and LON, respectively, depending on the independent input signals of HIN and LIN. The INS2040 offers high-side and low-side driver interlocking operation to prevent shoot-though. To meet strict requirement of GaN FET gate voltage, both drivers employ a dedicated 5V LDO to maintain the same drive voltage accurately. The INS2040 offers fast propagation delays and excellent delay matching with advanced level shift technology providing -5V to 200V of common mode voltage range for SW and -5V to 5V of common mode voltage range for PGND. In addition, the level shift has high dv/dt immunity up to 200V/ns. An 250V internal bootstrap diode makes up a high-side bootstrap voltage together with the external bootstrap capacitor connected between BST and SW pins. The INS2040 is well suited for high power and high frequency applications since it supports a strong driving capability. Its operation is best understood by referring to the Block Diagram in Fig. 20.

Supply Rails

The INS2040 has three supply rails VCC, PVCC and BST. The VCC supplies current only to the internal logic circuit. The PVCC is the power source to charge the bootstrap capacitor through the internal bootstrap diode as well as providing bias directly to the internal low-side LDO, VDDL. The PVCC pin can be connected either to the same supply voltage of the VCC pin or to a separated voltage source. Additionally, because PVCC is referenced to PGND, the low-side gate driver return pin, it is completely isolated from VCC, which is referenced to GND. This isolation helps to prevent the noise-sensitive input logic stage from being affected by the driver's switching noise. The BST is the high-side bootstrap voltage serving as the input to the internal high-side LDO, VDDH. All three supplies have independent UVLO to prevent malfunction when each supply voltage maintains an under-voltage condition.

Bootstrap Diode

The INS2040 has an 250V integrated bootstrap diode reducing the need for external components. It provides BST floating supply for the high-side driver voltage, VDDH. The bootstrap capacitor is charged from PVCC and PGND to BST and SW when the low-side GaN FET is fully turned on, and it completely disconnects to BST when the high-side GaN FET is turned on.

Signal Ground (GND) and Power Ground (PGND)

GND is the ground for all internal logic circuits, and PGND is low-side driver return pin. Internally, the GND and PGND pins are isolated. For GaN FET including a source Kelvin return, a direct connection should be made from PGND pin to its Kevin return as shown in Fig. 21. The dedicated PGND pin of the INS2040 enables low-side driver to float above the current sensing voltage, V_{CS}. The low-side driver can withstand static voltages -5V to 5V of common mode voltage. This means that the low-side GaN FET gate-source voltage is not lost, and the full 5V VDDL voltage is available.

Internal Low-Dropout (LDO) Regulator

The INS2040 integrates two independent LDOs dedicated to gate voltage of high-side and low-side GaN FET. These LDOs provide 5V at the VDDH pin and VDDL pin from the BST pin and PVCC pin respectively. The tightly regulated 5V output maximizes power efficiency while ensuring the reliability of the GaN FET. The VDDH LDO and VDDL LDO can each float within -5V to 200V and -5V to 5V common mode voltage range, respectively. VDDH pin and VDDL pin must be bypassed to SW pin and PGND pin with a minimum of 1μF ceramic capacitor.

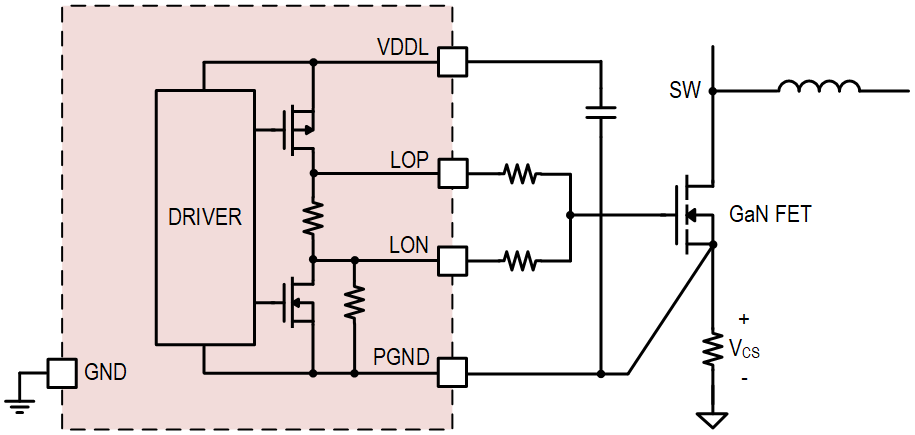


Fig. 21. Kelvin Gate Return Connection with Current Sense Resistor

Undervoltage Lockout (UVLO)

The INS2040 features an undervoltage lockout (UVLO) on both VCC and the floating voltage from BST to SW (BST-SW). When VCC is below its UVLO threshold, typical 7.5V, the INS2040 enters VCC UVLO mode and turns off both driver outputs and ignores both inputs. When VCC is above the UVLO rising, typical 8V, the INS2040 will normally operate. When BST-SW is below its UVLO threshold, typical 6V, the INS2040 enters BST UVLO mode and turns off the high-side driver and ignores the high-side input while the low-side driver operates normally. When BST-SW is above the UVLO rising, typical 6.5V, the high-side will return to normal operation. In addition, the INS2040 includes UVLO protection for both internal regulators with a falling threshold of typical 4V and a rising threshold of typical 4.25V. In VDDH UVLO mode, the high-side driver is turned off and the low-side driver operates normally. In VDDL UVLO mode, the opposite occurs. When each UVLO condition is cleared, a cycle-by-cycle, edge-triggered logic function is used to prevent shortened or erroneous control pulses from being processed by the output. The UVLO operation of the INS2040 is shown in Fig. 22.

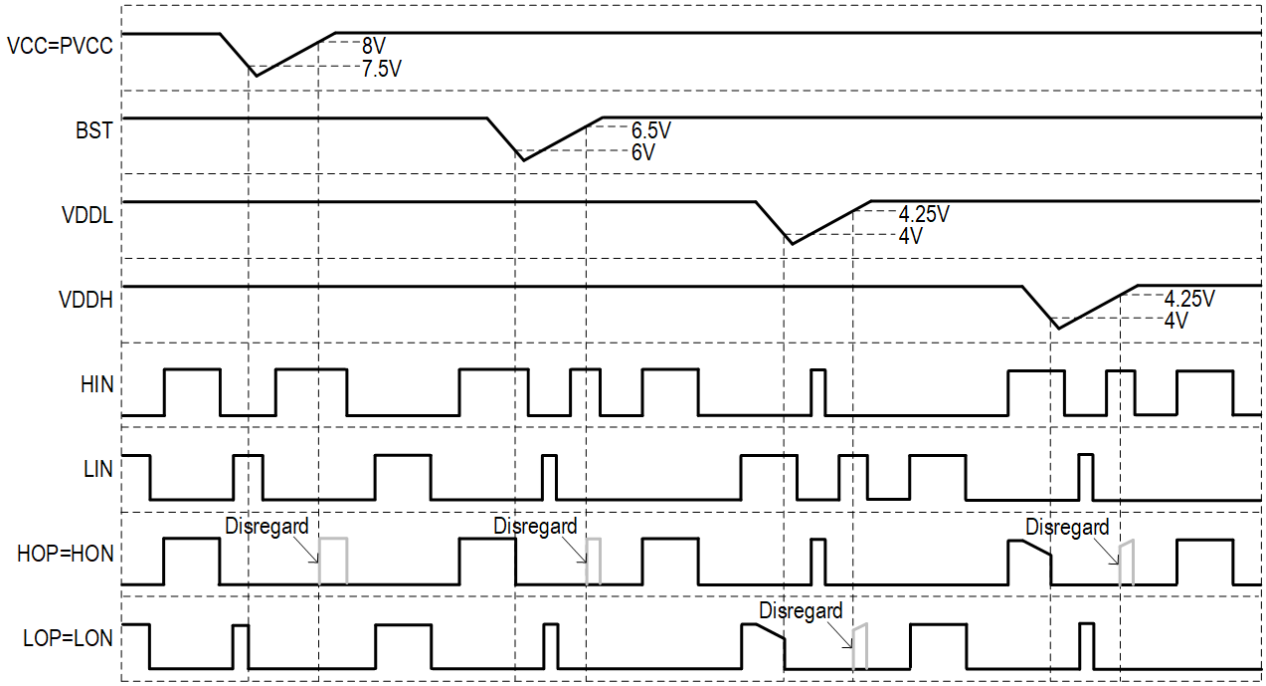


Fig. 22. Timing Diagram of ULVO Protection

Split Gate Driving Output

It is often practiced reducing gate drive pull-up strengths in driving GaN FET switches by adding an external gate resistor, to prevent the large dv/dt induced switching spikes that deteriorates reliability and EMI. Then again, strong pull-down gate drive is always required because the fast slew rate of drain of GaN FET node may pull up the gate of the GaN FET and falsely turn it on. The INS2040 features independent split gate drive for both the high-side and low-side, which allows the use of a large pull-up resistor and low pull-down resistor to achieve optimized efficiency, reliability, and EMI performance.

Level Shift

The INS2040 incorporates an advanced level-shift circuit for the high-side driver. The level shift transfers the signal from the power domain of VCC and GND to the power domain of BST and SW, with tight delay matching to the low-side driver and high noise immunity to the high dv/dt slew rate of SW voltage. The INS2040 provides a delay matching of a typical 1ns and supports high SW voltage slew rate of the maximum 200V/ns.

Input and Output

The INS2040 has two independent inputs that are compatible with Transistor-Transistor Logic (TTL). Both inputs have the upper and the lower thresholds of minimum 2.5V and maximum 0.8V, respectively. The input HIN controls the high-side driver outputs (HOP and HON) while the input LIN controls the low-side driver outputs (LOP and LON). Both inputs provide the input deglitching delay time of a typical 5ns to prevent any false triggering condition. Both inputs have the internal pull-down resistor of a typical 333kΩ. During both inputs are high, the anti-shoot-through function turns off both driver outputs as shown in Fig. 23.

Enable (EN)

To ensure a default disabled output state, the EN pin is internally pulled down. Similar to HIN and LIN, EN is a TTL compatible input. When the EN pin voltage is higher than the upper threshold of minimum 2.5V, enables the outputs, placing the INS2040 into an active ready state. For normal operation, the EN pin should be pulled up to VCC with the pull-up resistor. However, in applications where the EN is actively controlled, the EN can be driven directly. When the EN pin voltage pulled low, both inputs are ignored, and both driver outputs are immediately turned off. When EN is toggled high, during normal operation, a cycle-by-cycle, edge-triggered logic function is used to prevent shortened or erroneous control pulses from being processed by the output. Table 1 shows the truth table of inputs.

Table 1. Input and Output Logic Table

HIN	LIN	EN	HOP	HON	LOP	LON
L	L	H	Open	L	Open	L
L	H	H	Open	L	H	Open
H	L	H	H	Open	Open	L
H	H	H	Open	L	Open	L
Open	Open	H	Open	L	Open	L
X	X	L	Open	L	Open	L

Note: When an output is “Open”, it is connected to another split output through the internal 10kΩ resistor.

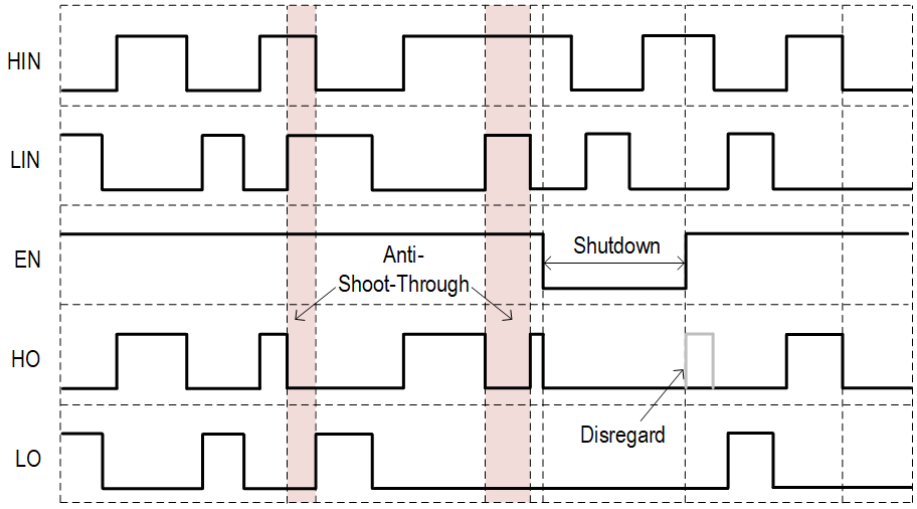


Fig. 23. Timing Diagram of Enable and Anti-Shoot-Through Function

Over Temperature Protection (OTP)

The INS2040 employs over temperature protection (OTP). If the junction temperature reaches around typical 160°C, both outputs are turned off, while both inputs are ignored. When the temperature is recovered to below typical 110°C, INS2040 will operate normally.

16. Package Information

To be added

17. Tape and Reel Information

18. Recommended Land Pattern

QFN4X4-15L Package:

19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
INS2040QC	QFN4x4-15L	2040QC	MSL3	13” 2500PCS/reel

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