



QNHCHIP

QND22N10G

# Product Specification

**QND22N10G**

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100V N-Channel SGT MOSFET



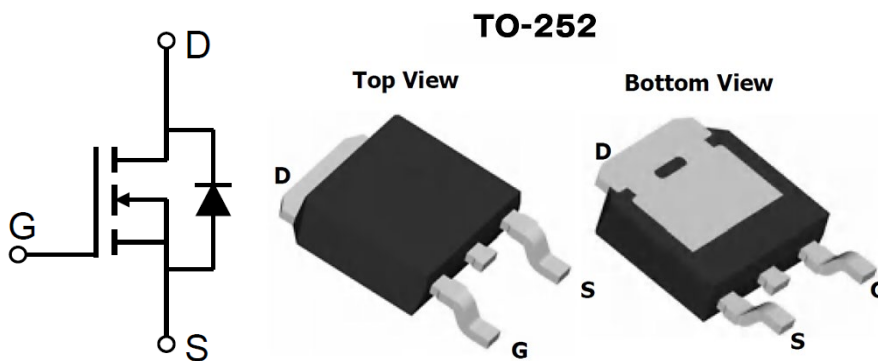
## FEATURES

- 100V, 8A  
 $R_{DS(ON)} < 130m\Omega @ V_{GS} = 10V$   
 $R_{DS(ON)} < 160m\Omega @ V_{GS} = 4.5V$
- Advanced Split Gate Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge

## Applications

- Load Switch
- PWM Application
- Power Management

## Pin Description



NO.	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE



## Absolute Maximum Ratings

(@  $T_C = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_C = 25^\circ\text{C}$	8
		$T_C = 100^\circ\text{C}$	5
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	32	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>(2)</sup>	6.25	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	32
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.9	$^\circ\text{C}/\text{W}$
$T_J, T_{STG}$	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$



## Electrical Characteristics

( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1.0	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0\text{V}$ , $V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	1.0	1.65	2.5	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance <sup>(3)</sup>	$V_{GS} = 10\text{V}$ , $I_D = 3\text{A}$	-	95.0	130.0	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}$ , $I_D = 1\text{A}$	-	120.0	160.0	$\text{m}\Omega$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{V}$ , $V_{DS} = 50\text{V}$ , $f = 1\text{MHz}$	-	200	-	pF
$C_{oss}$	Output Capacitance		-	30	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	3	-	pF
$Q_g$	Total Gate Charge	$V_{GS} = 0 \sim 10\text{V}$ , $V_{DS} = 50\text{V}$ , $I_D = 3\text{A}$	-	4	-	nC
$Q_{gs}$	Gate Source Charge		-	0.9	-	nC
$Q_{gd}$	Gate Drain ("Miller") Charge		-	1.1	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{V}$ , $V_{DD} = 50\text{V}$ , $I_D = 3\text{A}$ , $R_{GEN} = 3\Omega$	-	12.6	-	ns
$t_r$	Turn-On Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	20	-	ns
$t_f$	Turn-Off Fall Time		-	27.8	-	ns
<b>Drain-Source Diode Characteristics and Max Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	8	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	32	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}$ , $I_S = 3\text{A}$	-	-	1.2	V

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
2.  $E_{AS}$  condition: Starting  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 30\text{V}$ ,  $V_G = 10\text{V}$ ,  $R_G = 25\Omega$ ,  $L = 0.5\text{mH}$ ,  $I_{AS} = 5\text{A}$
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 0.5\%$ .



## Typical Performance Characteristics

Figure 1: Output Characteristics

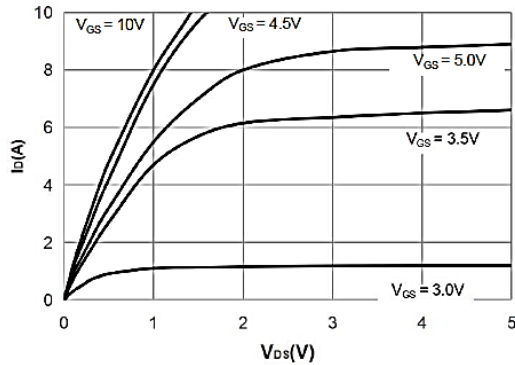


Figure 2: Typical Transfer Characteristics

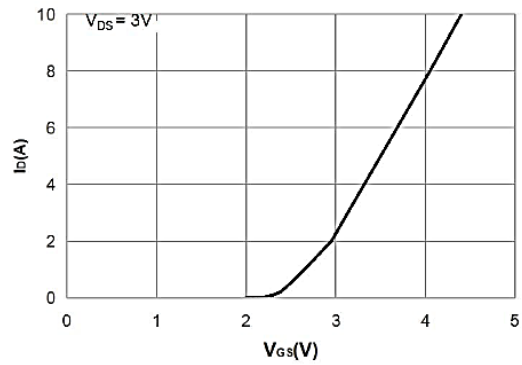


Figure 3: On-resistance vs. Drain Current

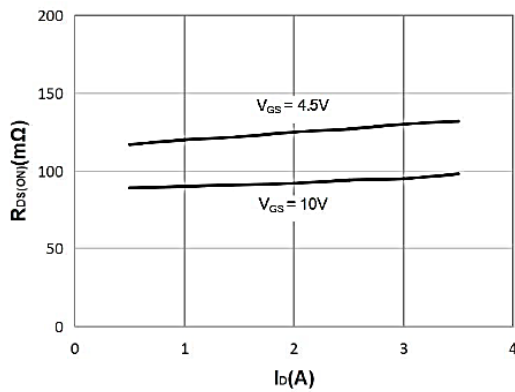


Figure 4: Body Diode Characteristics

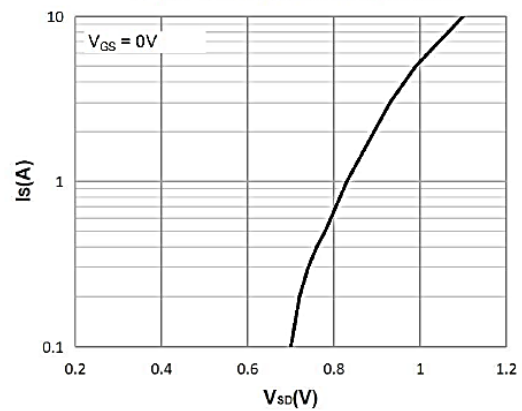


Figure 5: Gate Charge Characteristics

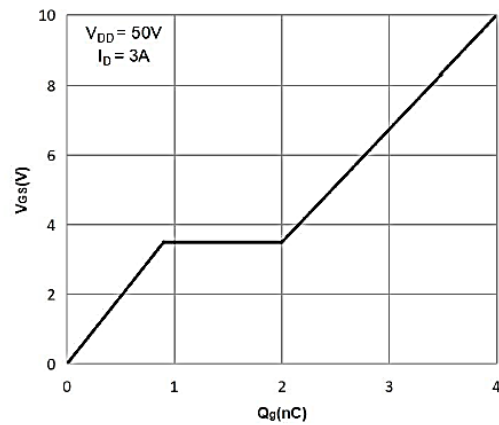


Figure 6: Capacitance Characteristics

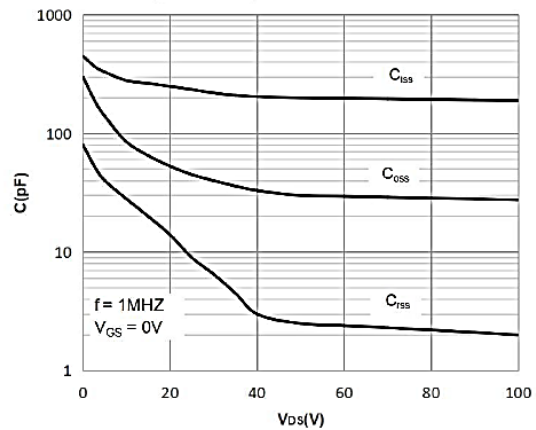




Figure 7: Normalized Breakdown voltage vs. Junction Temperature

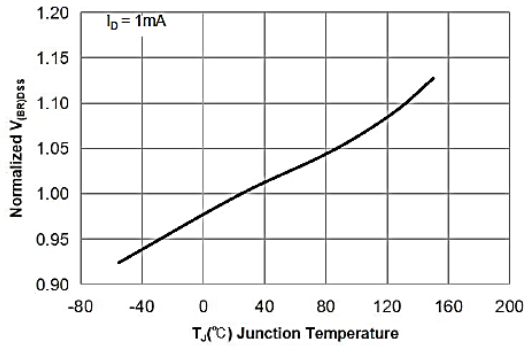


Figure 8: Normalized on Resistance vs. Junction Temperature

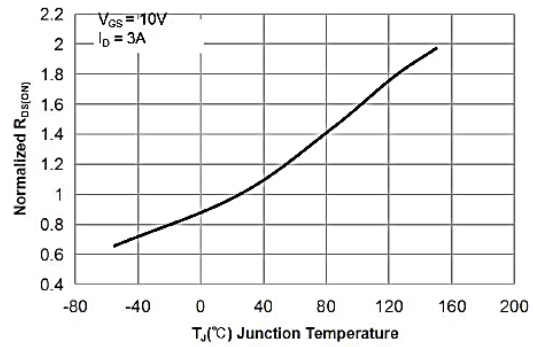


Figure 9: Maximum Safe Operating Area

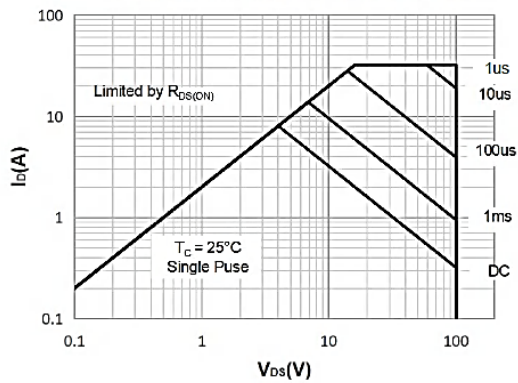


Figure 10: Maximum Continuous Drianc Current vs. Case Temperature

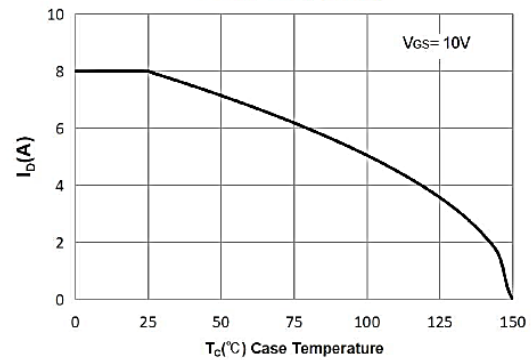


Figure 11: Normalized Maximum Transient Thermal Impedance

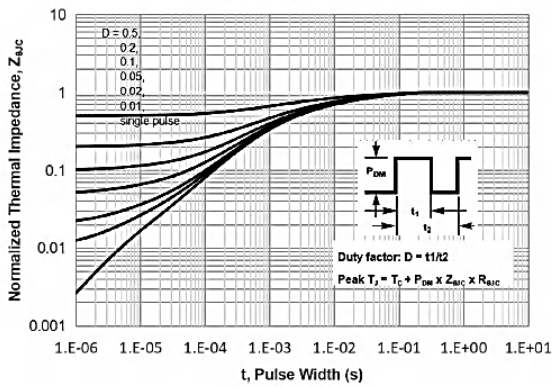
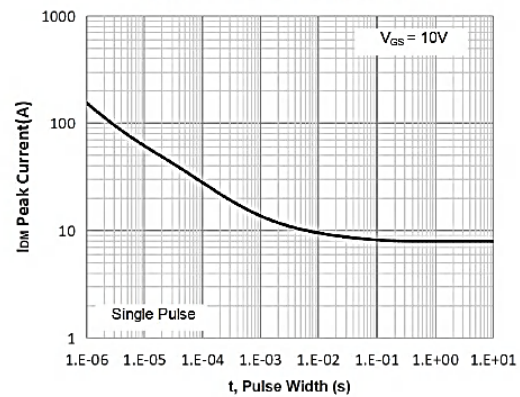


Figure 12: Peak Current Capacity





## Test Circuit

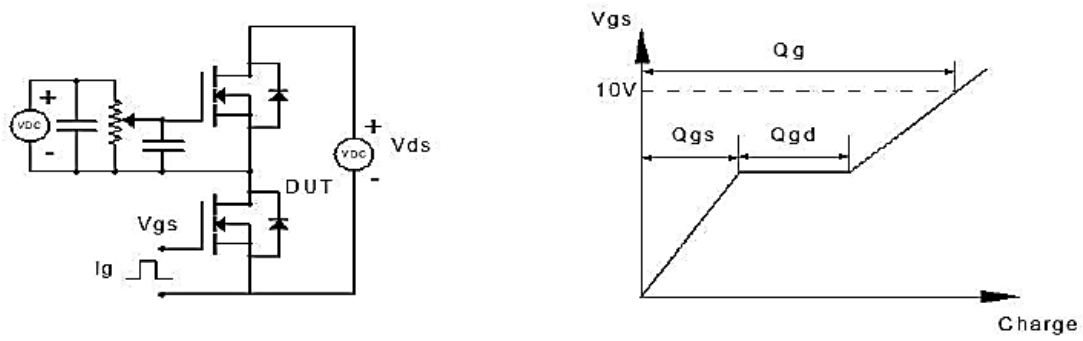


Figure 1: Gate Charge Test Circuit & Waveform

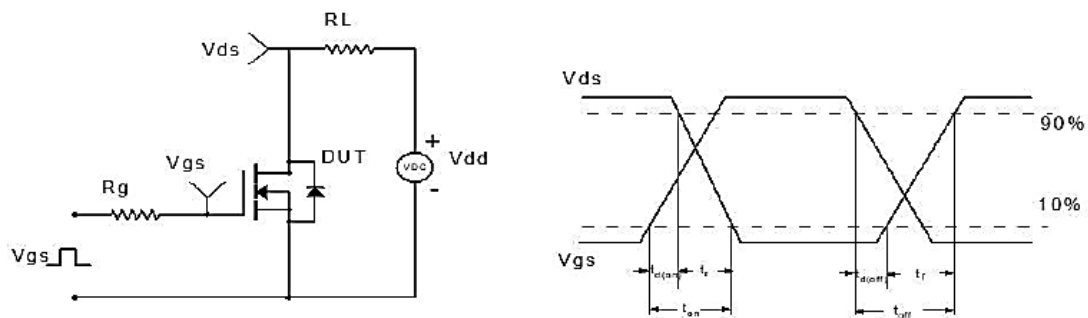


Figure 2: Resistive Switching Test Circuit & Waveform

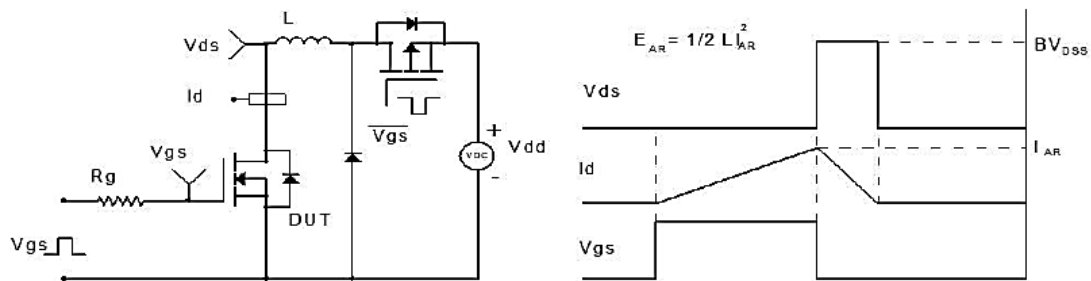


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

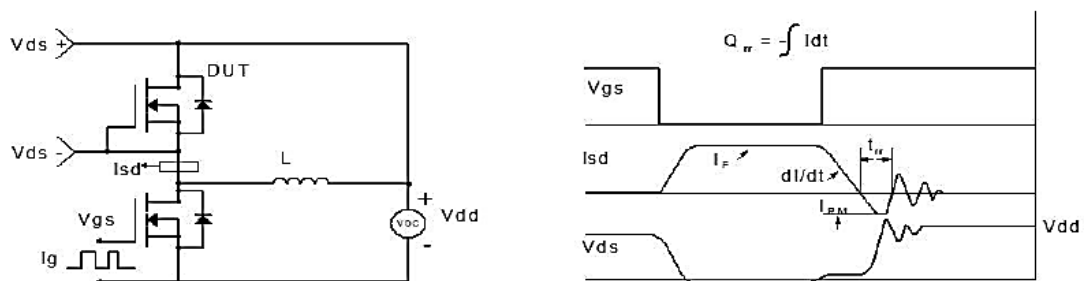
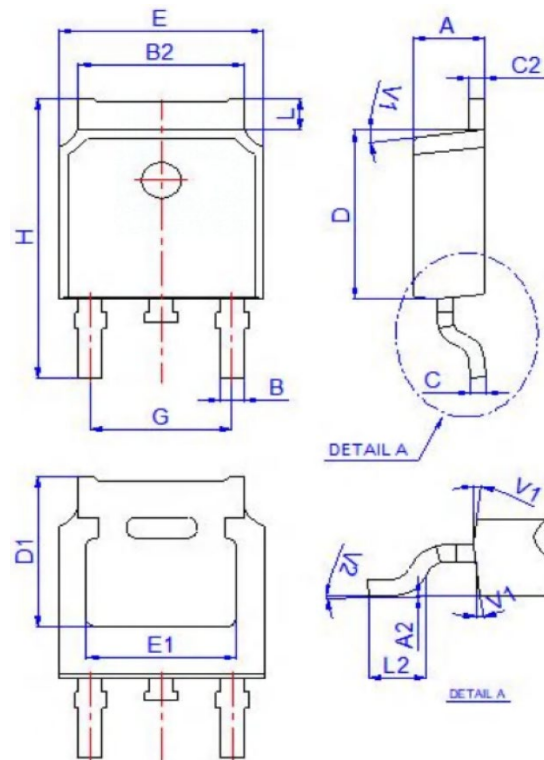


Figure 4: Diode Recovery Test Circuit & Waveform



## Package Mechanical Data(TO-252-3L)



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.10	2.50	0.083	0.098
A2	0	0.10	0	0.004
B	0.66	0.86	0.026	0.034
B2	5.18	5.48	0.202	0.216
C	0.40	0.60	0.016	0.024
C2	0.44	0.58	0.017	0.023
D	5.90	6.30	0.232	0.248
D1	5.30 REF		0.209 REF	
E	6.40	6.80	0.252	0.268
E1	4.63		0.182	
G	4.47	4.67	0.176	0.184
H	9.50	10.70	0.374	0.421
L	1.09	1.21	0.043	0.048
L2	1.35	1.65	0.053	0.065
V1	7°		7°	
V2	0°	6°	0°	6°

## Ordering information

Order Code	Package	V <sub>DS</sub> (V)	I <sub>D</sub> (A)	R <sub>DS(ON)</sub> ( m Ω )	
QND22N10G	TO-252	100	8	V <sub>GS</sub> =10V	<130
				V <sub>GS</sub> =4.5V	<160