1. General Description

The 74LVC244A; 74LVCH244A are 8-bit buffer/line drivers with 3-state outputs. The devices can be used as two 4-bit buffers or one 8-bit buffer. Both devices features two output enables ($1\overline{OE}$ and $2\overline{OE}$), each controlling four of the 3-state outputs. A HIGH on $n\overline{OE}$ and causes the outputs to assume a high-impedance OFF-state. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and Benefits

- Wide supply voltage range from 1.2 V to 5.5 V
- Direct interface with TTL levels
- CMOS low power dissipation
- Overvoltage tolerant inputs to 5.5 V
- Bus hold on all data inputs (74LVCH244A only)
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 6000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V

3.Ordering Information

Table 1. Ordering information

Type number	Package		
	Name	Description	Quantity
74LVC244AD	SOP-20L	plastic small outline package; 20 leads; body width 7.5 mm	2000
74LVCH244AD			
74LVC244APW	TSSOP-20L	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	2500
74LVCH244APW			

4. Function Diagram

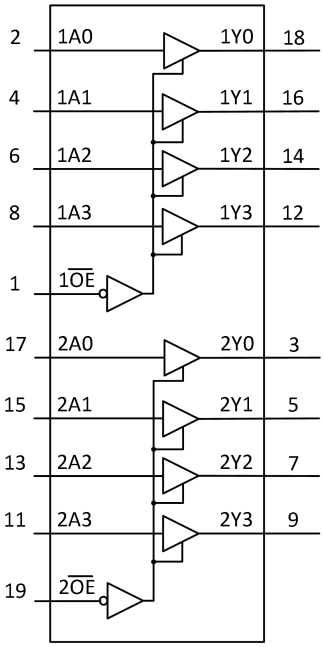


Fig. 1. Functional diagram

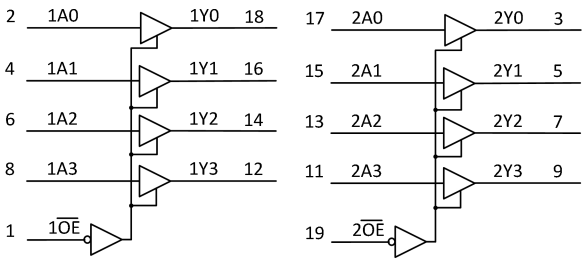


Fig. 2. Logic symbol

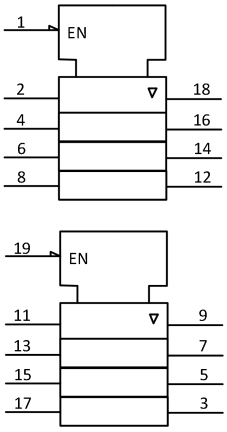


Fig. 3. IEC logic symbol

5. Pinning Information

5.1. Pinning

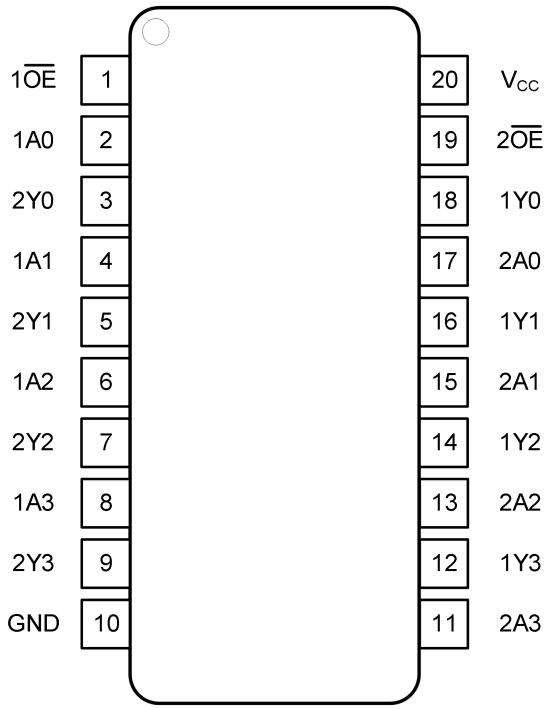


Fig. 4. Top view pin configuration SOP and TSSOP

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{OE}$, 2$\overline{OE}$	1, 19	Output enable input(active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	Data input
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	Bus output
GND	10	Ground (0V)
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	Data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	Bus output
V_{CC}	20	Supply voltage

6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 4. Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50		mA
V_I	Input voltage	[1]	-0.5	6.5	V
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{CC}$		±50	mA
V_O	output voltage	output HIGH or LOW [2]	-0.5	V_{CC}+0.5	V
		output 3-state	-0.5	6.5	V
I_O	output current	V_O = 0 V to V_{CC}		±50	mA
I_{CC}	supply current			100	mA
I_{GND}	ground current		-100		mA
P_{tot}	total power dissipation			500	mW
T_{stg}	storage temperature		-65	150	°C

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.

8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65		5.5	V
		functional	1.2		5.5	V
V_I	input voltage		0		5.5	V
V_O	output voltage	output HIGH or LOW	0		V_{CC}	V
		output 3-state	0		5.5	V
T_{amb}	ambient temperature		-40		125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.2 V to 2.7 V			20	ns/V
		V_{CC} = 2.7 V to 5.5 V			10	ns/V

9.Static Characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). Typical values measured at T_{amb} = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08			1.08		V
		V_{CC} = 1.65 V to 1.95 V	0.65V_{CC}			0.65V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7			1.7		V
		V_{CC} = 2.7 V to 3.6 V	2.0			2.0		V
		V_{CC} = 4.5 V to 5.5 V	0.7V_{CC}			0.7V_{CC}		V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V			0.12		0.12	V
		V_{CC} = 1.65 V to 1.95 V			0.35V_{CC}		0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7		0.7	V
		V_{CC} = 2.7 V to 3.6 V			0.8		0.8	V
		V_{CC} = 4.5 V to 5.5 V			0.3V_{CC}		0.3V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2			1.05		V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9			1.7		V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2			2.1		V
		I_O = -24 mA; V_{CC} = 3.0 V	2.4			2.2		V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8			3.4		V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V			0.1		0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V			0.45		0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V			0.3		0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V			0.4		0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V			0.55		0.8	V
		I_O = 32 mA; V_{CC} = 4.5 V			0.55		0.8	V
I_I	input leakage current	V_I = V_{CC} or GND ; [2] V_{CC} = 5.5 V			±2		±10	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; V_{CC} = 5.5 V ; [2] $V_O = V_{CC}$ or GND			±5		±10	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V ; V_{CC} =0 V			±10		±20	µA
I_{CC}	supply current	$V_I = V_{IH}$ or GND ; I_O = 0 A ; V_{CC} = 5.5 V			10		20	µA
ΔI_{CC}	additional supply current	per input pin ; $V_I = V_{CC}$ – 0.6V ; I_O = 0 A ; V_{CC} = 2.7 V to 5.5 V			500		5000	µA
C_I	input capacitance	Pin $\overline{OE}$		4.0				pF
		Pin nAn		7.7				pF
I_{BHL}	bus hold LOW current	V_I = 0.58 V; V_{CCI} = 1.65 V[3][4]	25			20		µA
		V_I = 0.70 V; V_{CCI} = 2.3 V	45			45		µA
		V_I = 0.80 V; V_{CCI} = 3.0 V	100			80		µA
		V_I = 1.35 V; V_{CCI} = 4.5 V	100			100		µA
I_{BHH}	bus hold HIGH current	V_I = 1.07 V; V_{CCI} = 1.65 V[3][4]	-1			-1		µA
		V_I = 1.70 V; V_{CCI} = 2.3 V	-7			-7		µA
		V_I = 2.00 V; V_{CCI} = 3.0 V	-35			-35		µA
		V_I = 3.15 V; V_{CCI} = 4.5 V	-95			-95		µA
I_{BHLO}	bus hold LOW overdrive current	V_{CCI} = 1.95 V [3][5]	200			200		µA
		V_{CCI} = 2.7 V	300			300		µA
		V_{CCI} = 3.6 V	500			500		µA
		V_{CCI} = 5.5 V	900			900		µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CCI} = 1.95 V [3][5]	-200			-200		µA
		V_{CCI} = 2.7 V	-300			-300		µA
		V_{CCI} = 3.6 V	-500			-500		µA
		V_{CCI} = 5.5 V	-900			-900		µA

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.
[2] The bus hold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input terminal.
[3] Valid for data inputs of bus hold parts only (74LVCH244A). Note that control inputs do not have a bus hold circuit.
[4] The specified sustaining current at the data input holds the input below the specified V_I level.
[5] The specified overdrive current at the data input forces the data input to the opposite input state.

10. Dynamic Characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7. Typical values measured at T_{amb} = 25°C (unless otherwise noted).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nAn to nYn; see Fig. 5 [2]						
		V_{CC} = 1.65 V to 1.95 V			35		40	ns
		V_{CC} = 2.3 V to 2.7 V			20		25	ns
		V_{CC} = 3.0 V to 3.6 V			15		20	ns
		V_{CC} = 4.5 V to 5.5 V			10		15	ns
t_{en}	enable time	$n\overline{OE}$ to nYn; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V			35		40	ns
		V_{CC} = 2.3 V to 2.7 V			20		25	ns
		V_{CC} = 3.0 V to 3.6 V			15		20	ns
		V_{CC} = 4.5 V to 5.5 V			10		15	ns
t_{dis}	disable time	$n\overline{OE}$ to nYn; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V			35		40	ns
		V_{CC} = 2.3 V to 2.7 V			20		25	ns
		V_{CC} = 3.0 V to 3.6 V			15		20	ns
		V_{CC} = 4.5 V to 5.5 V			10		15	ns
$t_{sk(o)}$	output skew time	[3]			1		1.5	ns
C_{PD}	power dissipation capacitance	Per buffer ; V_{CC} = 3.3 V V_I = GND to V_{CC} [4]		18				pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 3.3 V, and 5 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}. t_{en} is the same as t_{PZL} and t_{PZH}. t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

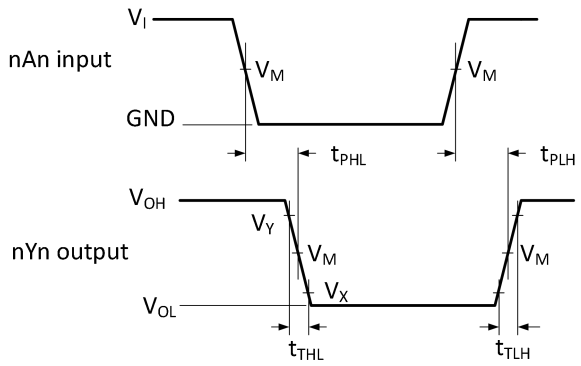
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

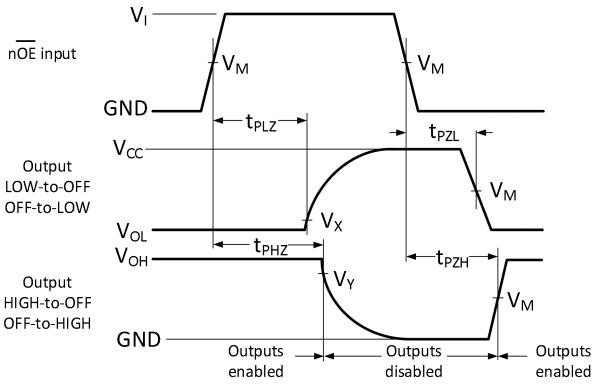
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The input nAn to output nYn propagation delays

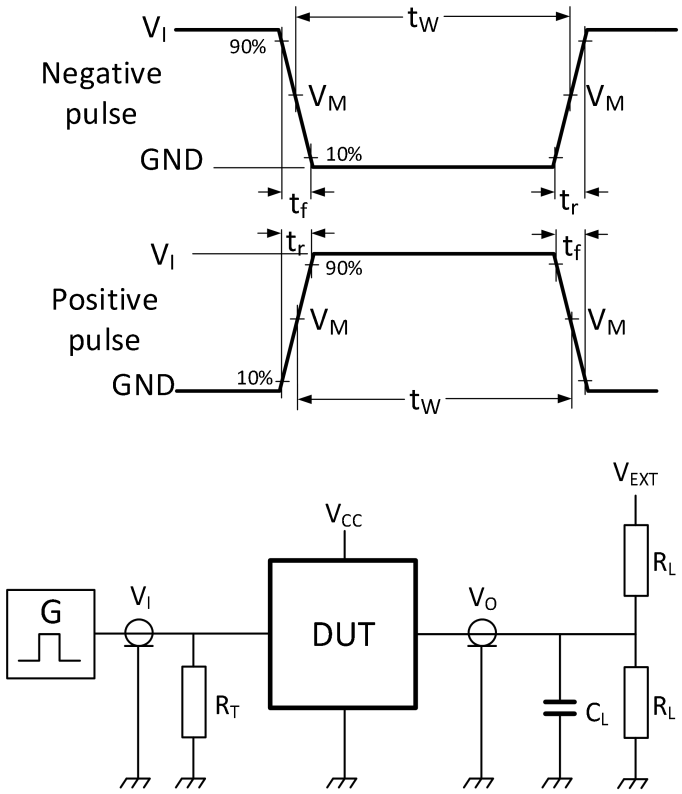


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
4.5 V to 5.5 V	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

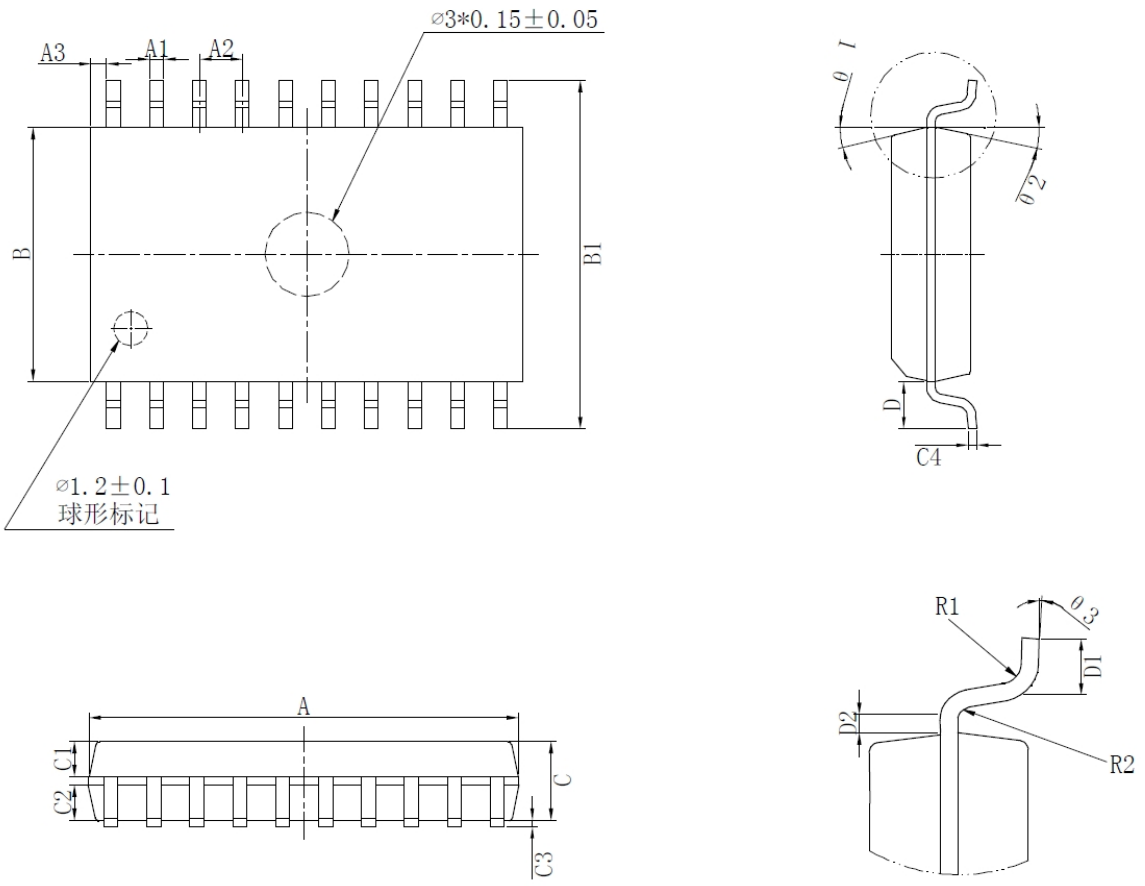
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65V to 1.95V	V_{CC}	≤ 2 ns	15 pF	2kΩ	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	15 pF	2kΩ	open	GND	$2V_{CC}$
3.0 V to 3.6 V	V_{CC}	≤ 2 ns	15 pF	2kΩ	open	GND	$2V_{CC}$
4.5 V to 5.5 V	V_{CC}	≤ 2 ns	15 pF	2kΩ	open	GND	$2V_{CC}$

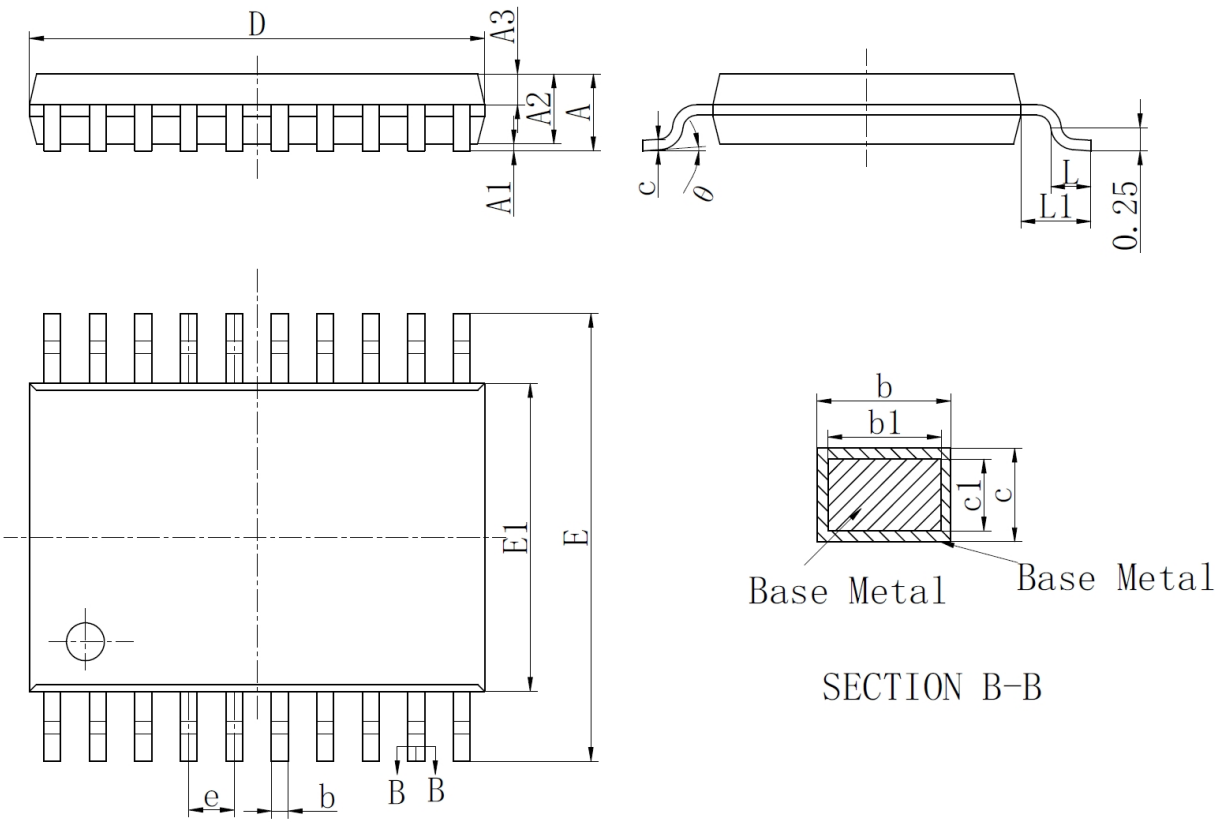
11. Package Outline

SOP-20L



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	12.600	12.900	C4	0.246	0.262
A1	0.381	0.431	D	1.353	1.453
A2	1.240	1.300	D1	0.764	0.964
A3	0.450	0.460	D2	0.18TYP	
B	7.400	7.600	R1	0.30TYP	
B1	10.206	10.406	R2	0.20TYP	
C	2.150	2.300	θ1	12° TYP	
C1	0.938	1.038	θ2	12° TYP	
C2	0.938	1.2038	θ3	0° ~ 8°	
C3	0.145	0.205			

TSSOP-20L



Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min.	Max.		Min.	Max.
A	-	1.20	E	6.20	6.60
A1	0.05	0.15	e	0.65BSC	
A2	0.80	1.05	L	0.45	0.75
A3	0.39	0.49	L1	1.00REF	
b	0.20	0.28	θ	0°	8°
b1	0.19	0.25			
c	0.13	0.17			
c1	0.12	0.14			
D	6.40	6.60			
E1	4.30	4.50			

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model

13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74LVC_LVCH244A Rev. 1.0	Aug 08, 2024	Draft datasheet		