

## 1. General Description

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The 74LVC07A is a hex buffer with open-drain outputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and Benefits

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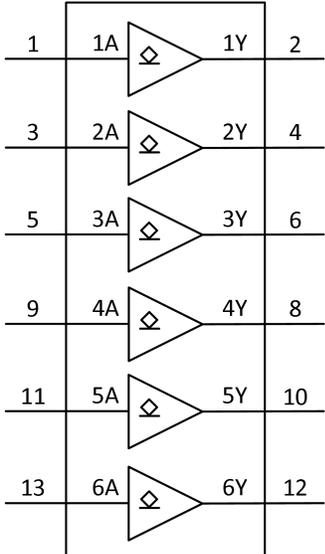
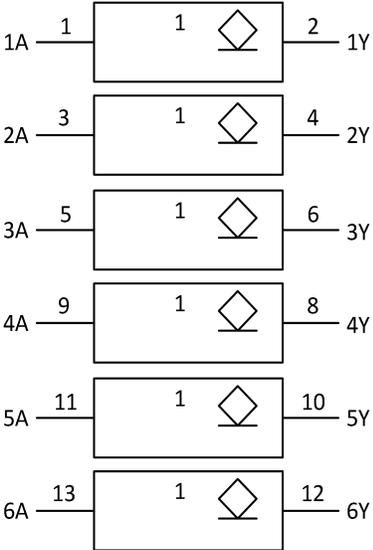
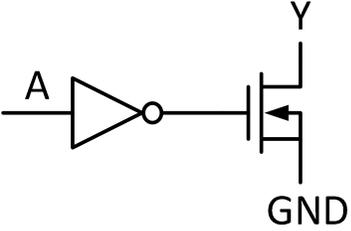
- Wide supply voltage range from 1.2 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low power dissipation
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 6000 V
  - CDM ANSI/ESDA/JEDEC JS-002 Class C3 exceeds 2000 V
- Multiple package options

### 3. Ordering Information

Table 1. Ordering information

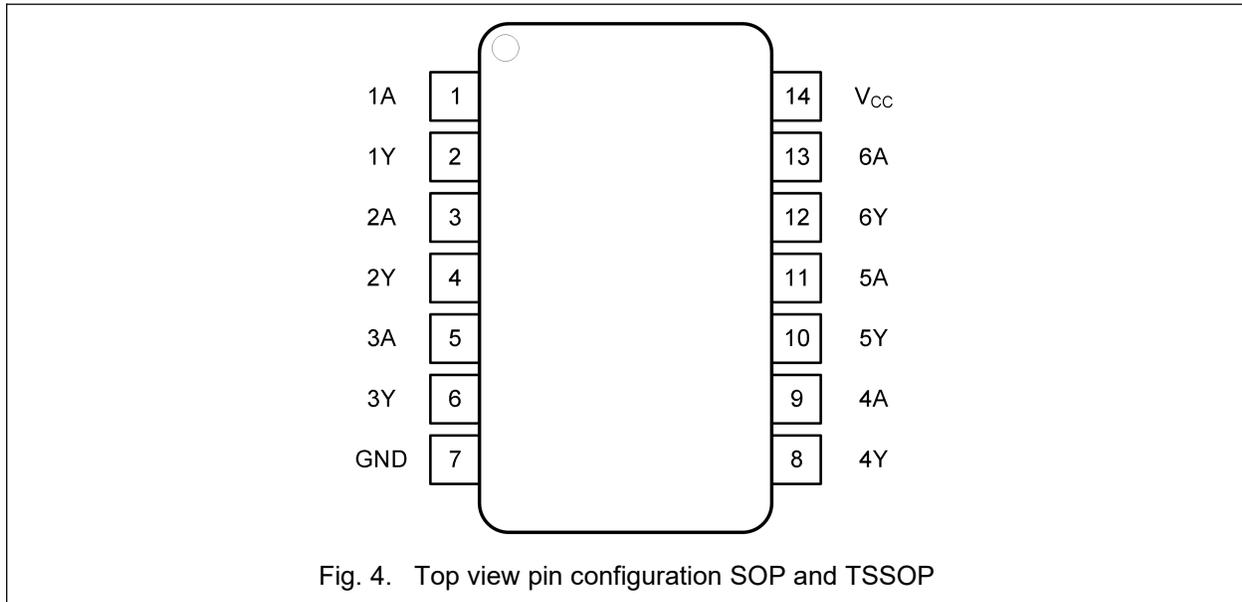
Type number	Package		
	Name	Description	Quantity
74LVC07AD	SOP-14L	plastic small outline package; 14 leads; body width 3.9 mm	2500
74LVC07APW	TSSOP-14L	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	2500

### 4. Function Diagram

 <p>Fig. 1. Logic symbol</p>	 <p>Fig. 2. IEC logic symbol</p>	 <p>Fig. 3. Logic diagram (one gate)</p>
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## 5. Pinning Information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	Data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	Data output
GND	7	Ground (0V)
V <sub>cc</sub>	14	Supply voltage

## 6. Functional Description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input nA	Output nY
L	L
H	Z

## 7. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

**Table 4. Absolute Maximum Ratings**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50		mA
$V_I$	input voltage	[1]	-0.5	6.5	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50		mA
$V_O$	output voltage	Active mode [1]	-0.5	6.5	V
		Power-down mode; $V_{CC} = 0$ V [1]	-0.5	6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$		50	mA
$I_{CC}$	supply current			100	mA
$I_{GND}$	ground current		-100		mA
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C		500	mW
$T_{stg}$	storage temperature		-65	150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 8. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. EnergyMath does not recommend exceeding them or designing to Absolute Maximum Ratings.

**Table 5. Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		1.65	5.5	V
		functional	1.2		V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	Active mode	0	5.5	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
$T_{amb}$	ambient temperature		-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to $2.7$ V	0	20	ns/V
		$V_{CC} = 2.7$ V to $5.5$ V	0	10	ns/V

## 9. Static Characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08			1.08		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>			0.65V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7			1.7		V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0			2.0		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>			0.7V <sub>CC</sub>		V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V			0.12		0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V			0.35V <sub>CC</sub>		0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V			0.7		0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V			0.8		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V			0.3V <sub>CC</sub>		0.3V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V			0.10		0.10	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V			0.45		0.70	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V			0.30		0.45	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V			0.40		0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V			0.55		0.80	V
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V			0.55		0.80	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND ; V <sub>CC</sub> = 0 V to 5.5 V		±0.1	±5		±20	μA
I <sub>oz</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V		±0.1	±10		±20	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V		±0.1	±10		±20	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 1.65 V to 5.5 V ; V <sub>I</sub> = V <sub>CC</sub> or GND ; I <sub>O</sub> = 0 A ;		0.01	10		40	μA

## 74LVC07A

### Hex buffer with open-drain outputs

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$\Delta I_{CC}$	additional supply current	per input pin ; $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}$ ; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$		0.2	500		5000	$\mu\text{A}$
$C_i$	input capacitance	$V_{CC} = 3.3 \text{ V}$ ; $V_I = \text{GND to } V_{CC}$		4				$\text{pF}$

[1]All typical values are measured at  $V_{CC} = 3.3\text{V}$  and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

## 10. Dynamic Characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{PZL}$	OFF-state to LOW propagation delay	nA to nY; see Fig. 5						
		$V_{CC} = 1.2\text{ V}$		28.3				ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	3.5	8.5	16.5	3.5	17	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.0	4.8	8.0	2.0	9.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	3.5	5.5	1.5	6.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.9	4.5	1.0	5.0	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	nA to nY; see Fig. 5						
		$V_{CC} = 1.2\text{ V}$		25.3				ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	3.5	7.7	14.5	3.5	15	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2.0	5.0	7.5	2.0	8.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	3.5	5.5	1.5	6.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	1.0	2.4	3.5	1.0	4.0	ns
$C_{PD}$	power dissipation capacitance	per buffer ; $V_I = \text{GND to } V_{CC}$ [2]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$		3.3				pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		3.4				pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$		3.9				pF
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		4.8				pF

 [1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 3.3\text{ V}$  and  $5.0\text{ V}$  respectively.

 [2]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$$
 where:

 $f_i$  = input frequency in MHz;

 $f_o$  = output frequency in MHz;

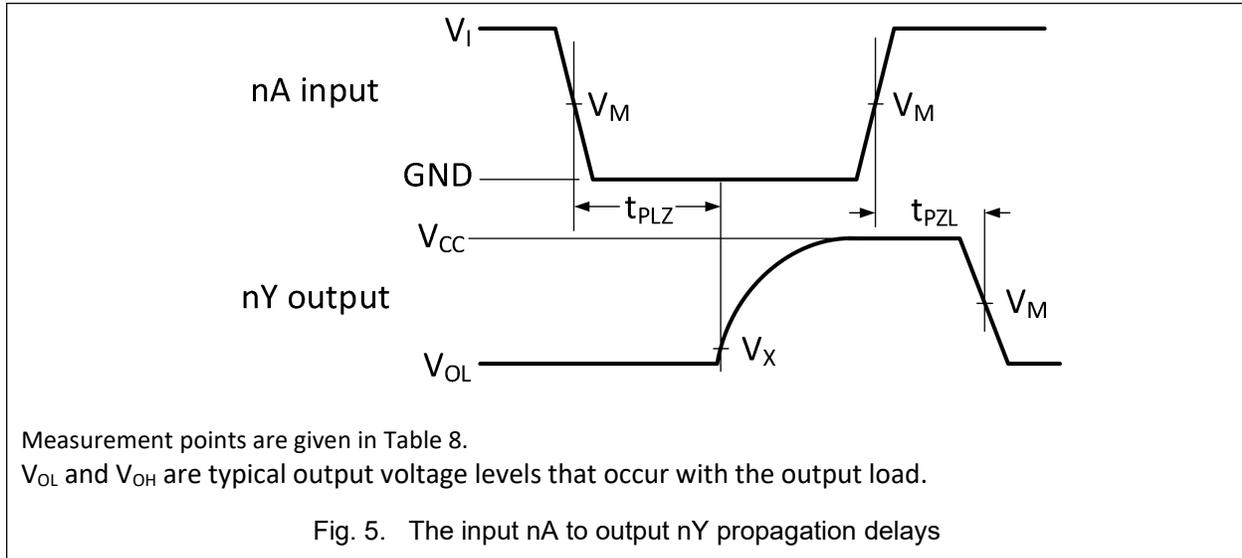
 $C_L$  = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

 $N$  = number of inputs switching;

 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 10.1. Waveforms and test circuit



**Table 8. Measurement points**

Supply voltage	Input	Output	
		$V_X$	$V_M$
$V_{CC}$	$V_M$	$V_X$	$V_M$
1.2 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$0.5V_{CC}$
1.65 V to 1.95 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$0.5V_{CC}$
3.0 V to 3.6 V	1.5 V	$V_{OL} + 0.3 V$	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$0.5V_{CC}$

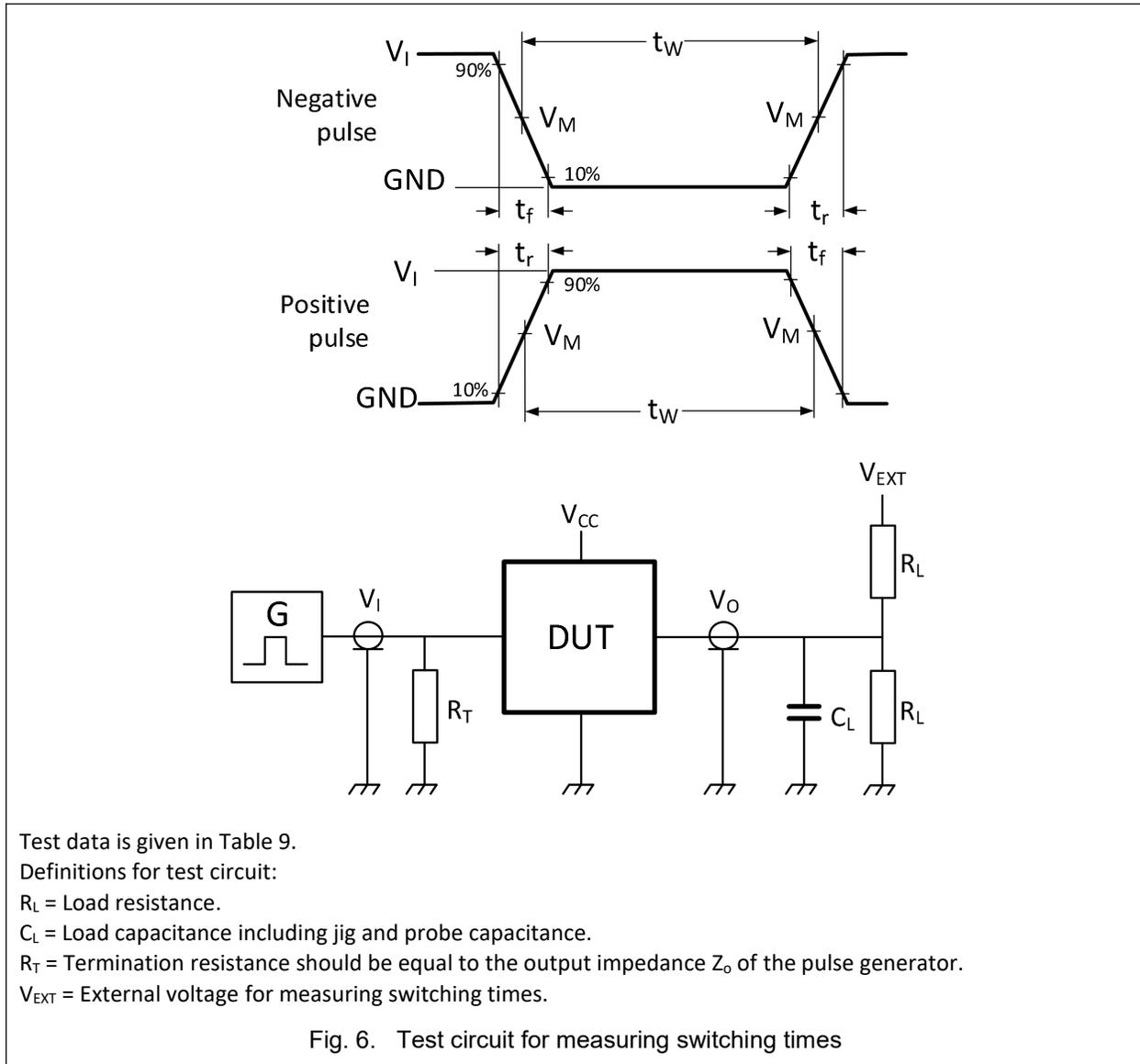
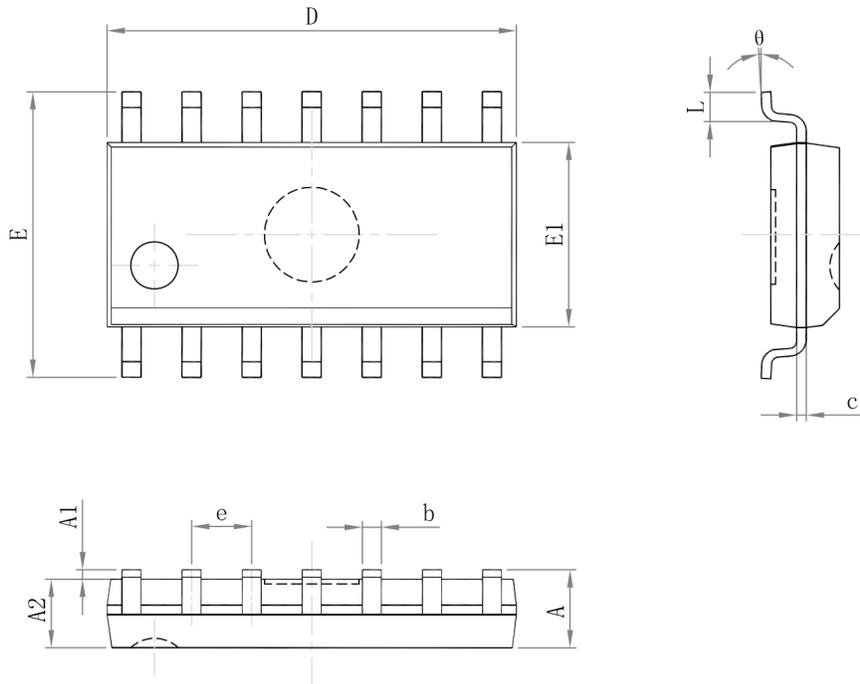


Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$
$V_{CC}$	$V_I$	$t_r = t_f$	$C_L$	$R_L$	$t_{PLZ}, t_{PZL}$
1.2V	$V_{CC}$	$\leq 2.0$ ns	15 pF	500 $\Omega$	$2 \times V_{CC}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	15 pF	500 $\Omega$	$2 \times V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	15 pF	500 $\Omega$	$2 \times V_{CC}$
3.0 V to 3.6 V	3 V	$\leq 2.0$ ns	15 pF	500 $\Omega$	6.0 V
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.0$ ns	15 pF	500 $\Omega$	$2 \times V_{CC}$

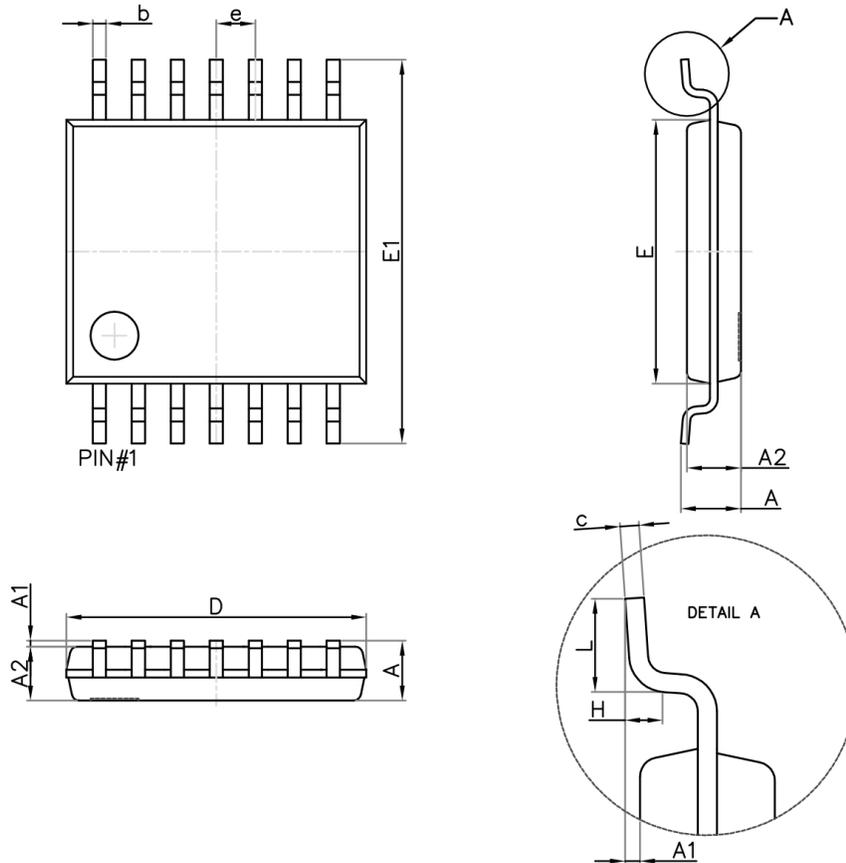
# 11. Package Outline

SOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	--	1.750	--	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	--	0.049	--
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

TSSOP-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A	—	1.200	—	0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
$\theta$	1°	7°	1°	7°

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

## 13. Revision History

Table 11. Revision history

Document ID	Release Date	Data sheet status	Change notice	Supersedes
74LVC07A Rev. 1.0	Aug 08, 2024	Product datasheet		