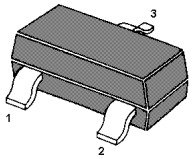
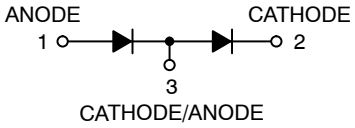
Low Capacitance Diode Array for ESD Protection in a Single Data Line

SOT-23





MARKING : 53*

Features

- Low Capacitance 0.9 pF Typ
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
  Machine Model = Class C
  Human Body Model = Class 3B
- Protection for IEC61000−4−2 (Level 4)
  8.0 kV (Contact)
  15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- Pb−Free Package is Available*

Applications

- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I^2C Bus Protection

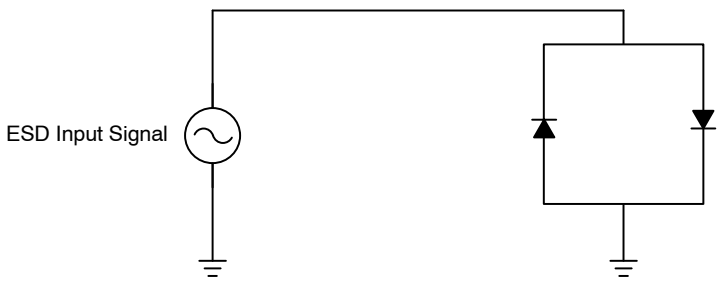


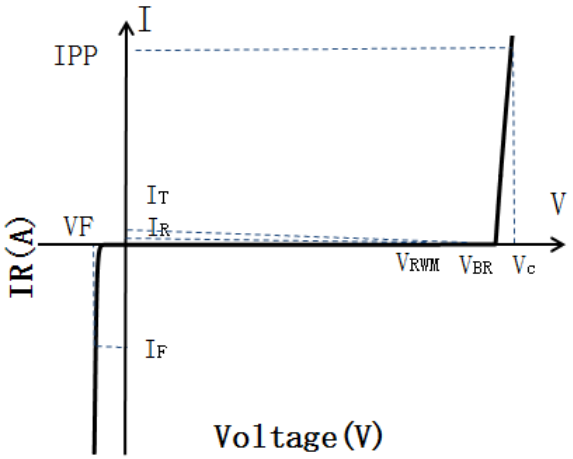
Figure 1. ESD Test Circuit

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppk	150	W
Peak Pulse Current (8/20μs)	IPP	15	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	VESD	±15 ±8	kV
Operating Temperature Range	TJ	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Portion Electronics Parameter

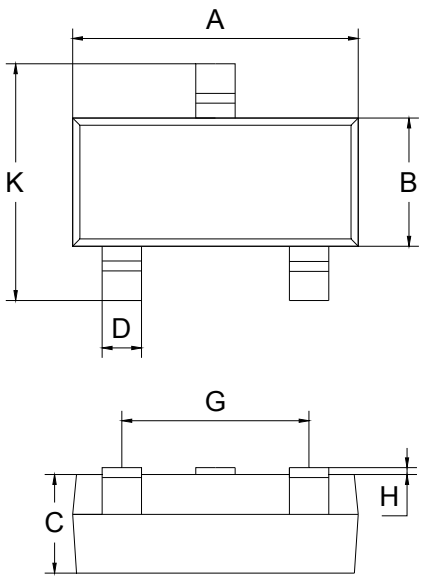
Symbol	Parameter
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
Vc	Clamping Voltage @Ic



Electrical Characteristics (T_A=25°C unless otherwise specified)

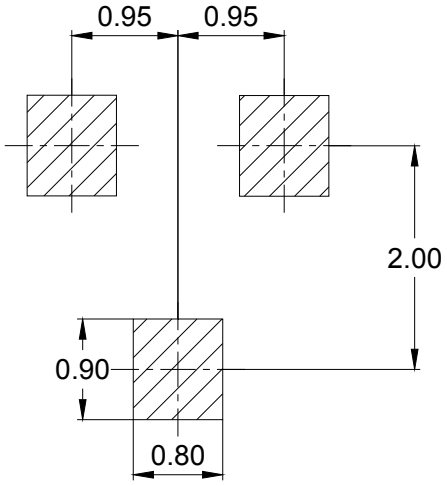
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				100	V
Breakdown Voltage	V_{BR}	I_T = 1mA	110			V
Reverse Leakage Current	I_R	V_{RWM} =100V			0.1	μA
Clamping Voltage	Vc	I_{PP} = 1A (8 x 20μs pulse)			8	V
Clamping Voltage	Vc	I_{PP} = 15A (8 x 20μs pulse)			10	V
Junction Capacitance	C_J	VR = 0V, f = 1MHz		0.9		pF

Plastic surface mounted package SOT-23



SOT-23		
Dim	Min	Max
A	2.70	3.10
B	1.10	1.50
C	1.0 Typical	
D	0.4 Typical	
E	0.35	0.48
G	1.80	2.00
H	0.02	0.1
J	0.1 Typical	
K	2.20	2.60
All Dimensions in mm		

SOLDERING FOOTPRINT



Unit : mm