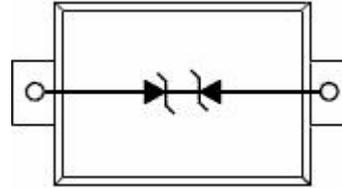
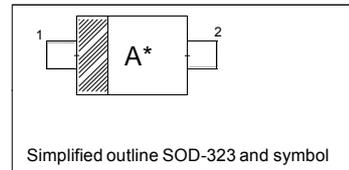


Transient Voltage Suppressor

PINNING

PIN	DESCRIPTION
1	Cathode
2	Anode



The PDYL050B is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Specification Features:

- Ultra Low Capacitance 0.5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions:
- Stand-off Voltage: 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- This is a Pb-Free Device
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

Maximum Ratings (Ta = 25°C)

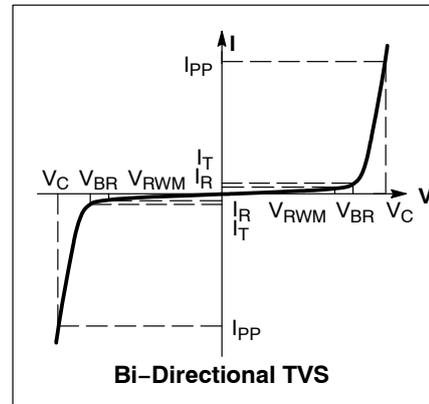
Symbol	Parameter	Value	Unit
TJ	Junction Temperature	-55 to +150	°C
TSTG	Storage Temperature	-55 to +150	°C
Ipp Max	Maximum Peak Pulse Current	3	A
PPK	Peak Pulse Power	45	W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS

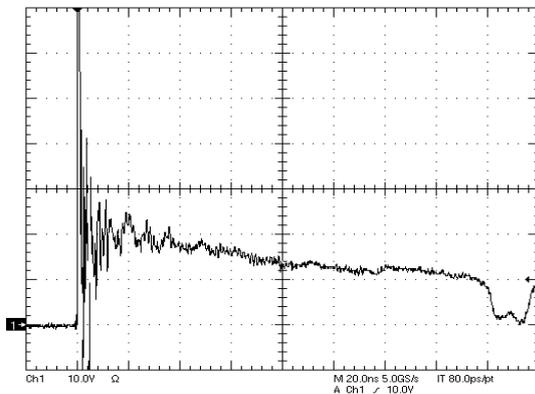
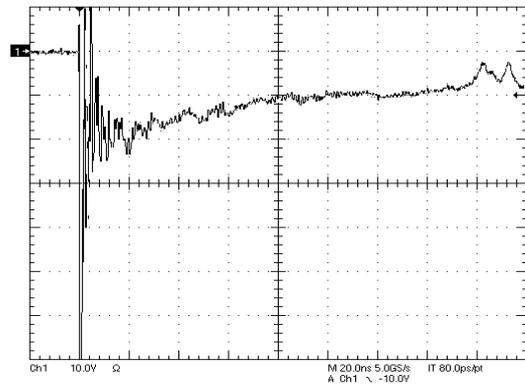
 (T_A = 25°C unless otherwise noted)

Symbol	Parameter
I _{PP}	Maximum Reverse Peak Pulse Current
V _C	Clamping Voltage @ I _{PP}
V _{RWM}	Working Peak Reverse Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
I _F	Forward Current
V _F	Forward Voltage @ I _F
P _{pk}	Peak Power Dissipation
C	Capacitance @ V _R = 0 and f = 1.0 MHz

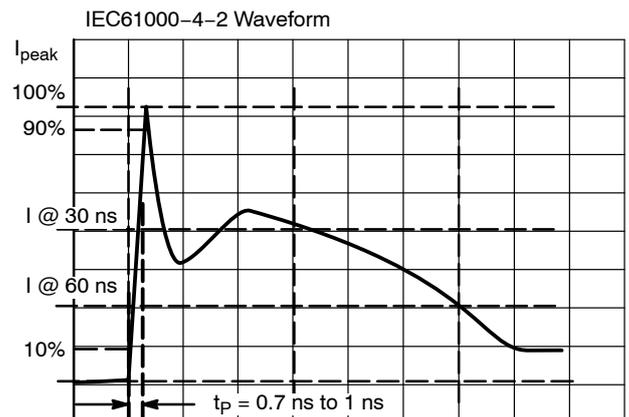

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Device	Device Marking	V _{RWM} (V)	I _R (μA) @ V _{RWM}	V _{BR} (V) @ I _T (Note 2)	I _T (mA)	C (pF) (Max)	V _C (V) @ I _{PP} = 3 A (Note 3)	V _C (Per IEC61000-4-2 (Note 4))
		Max	Max	Min			Max	
PDYL050B	A*	5.0	1.0	5.4	1.0	0.9	15	Figures 1 and 2 See Below

- V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
- Surge current waveform per Figure 4.
- For test procedure see Figures 3.

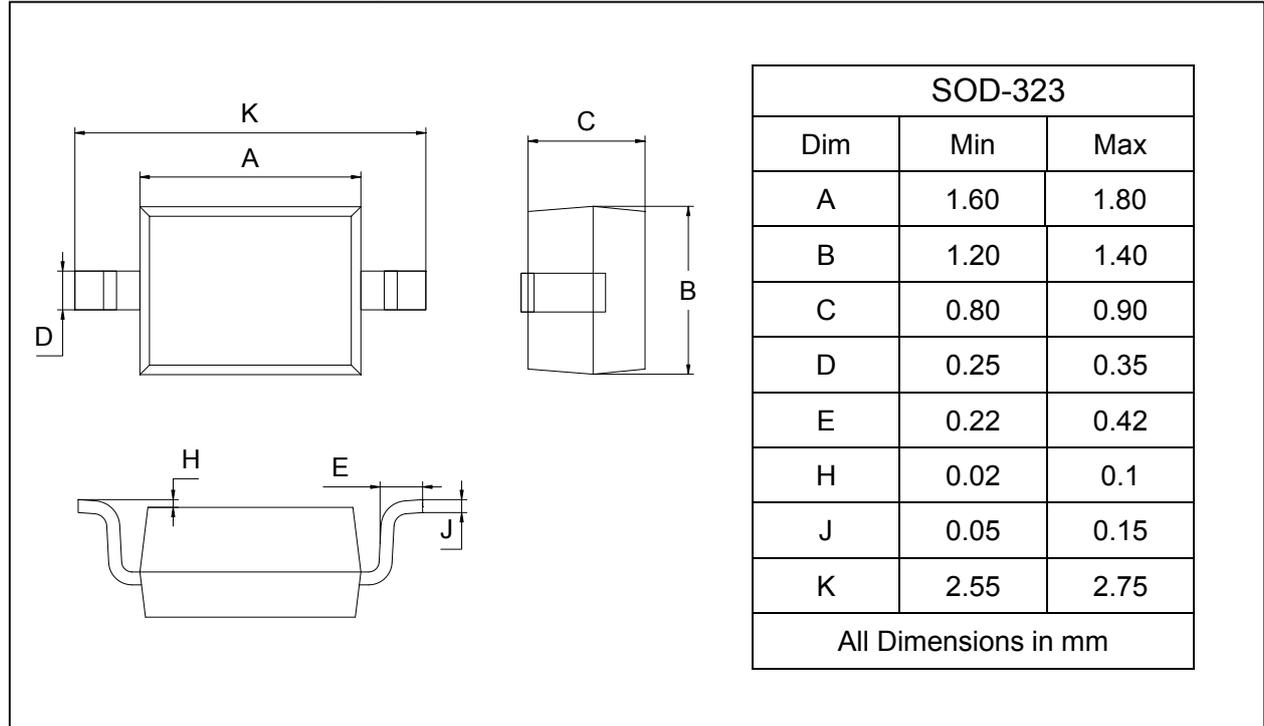

Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2
IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

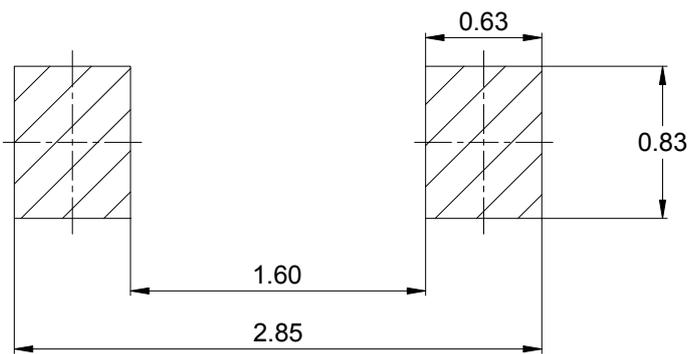

Figure 3. IEC61000-4-2 Spec

Plastic surface mounted package

SOD-323



SOLDERING FOOTPRINT



Unit : mm