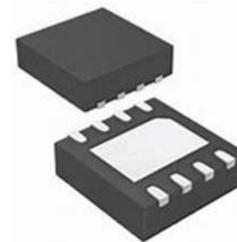


### Description

Innotion's YP161515T is a 15 watt, unmatched LDMOS FETs, designed for Wide-band and Mobile radio and Beidou RDSS System applications. It can be used in Class AB/B and Class C for all typical modulation formats.



DFN 5\*6-8L

### Typical Performance Over 1615MHz (T<sub>c</sub>=25°C)

Table1. (Test in Innotion Fixture): VDD=12V, I<sub>DQ</sub>=100mA, CW.

Frequency (MHz)	Gain (dB)	P <sub>sat</sub> (W)	Eff@ P <sub>sat</sub> (%)
1615	15	15	60

Capable of Handling 10:1 VSWR @ 12Vdc, 1615MHz, 15Watts CW Output Power for Enhanced Ruggedness applications.

### Features

- High Efficiency and Linear Gain Operation
- Integrated ESD Protection, Class2 (HBM)
- Excellent Thermal Stability and Excellent Ruggedness
- Plastic Package for General Use

### Table2. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	+40	Vdc
Gate-Source Voltage	V <sub>GS</sub>	-10 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+12	Vdc
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>C</sub>	+150	°C
Operating Junction Temperature	T <sub>J</sub>	+225	°C

**Table3. Electrical Characteristics**

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>DC Characteristics</b>						
Zero Gate Threshold Drain Leakage Current	$I_{DSS}$			10	uA	$V_{DS}=26V, V_{GS}=0V$
Zero Gate Threshold Drain Leakage Current	$I_{DSS}$			1	uA	$V_{DS}=12V, V_{GS}=0V$
Gate--Source Leakage Current	$I_{GSS}$			1	uA	$V_{DS}=0V, V_{GS}=6V$
Gate Threshold Voltage	$V_{GS(th)}$		1.85		V	$V_{DS}=12V, I_D=250uA$
Gate Quiescent Voltage	$V_{GS(Q)}$		2.68		V	$V_{DD}=12V, I_D=100mA$
<b>RF Characteristics<sup>1</sup> ( Tc=25°C, F<sub>0</sub>=1615MHz unless otherwise noted)</b>						
Saturated Output Power	$P_{sat}$		15		W	
Drain Efficiency@Psat,1615MHz	Eff		60		%	
Power Gain	$G_P$		15		dB	
Input Return Loss	$I_{RL}$		-10		dB	

**Note:**

1. Measured in INNOTION Test Fixture, 50ohm System,  $V_{DD}=12V, I_{DQ}=100mA$ , CW Signal Measurements.

**Table 4. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C= 85^\circ C, T_J=200^\circ C, DC$ test	$R_{\theta JC}$	1.8	$^\circ C/W$

**Table 5. Pin Description**

Pin No.	Symbol	Description
1-4	Gate	RF input,
5-8	Drain	RF Output
EP	Source	The bottom exposed pad is the RF ground. For best thermal dissipation

### Typical Performance

Bias1: VDD=12V, IDQ=100mA, PulseWidth=20us, Dutycycle=10%

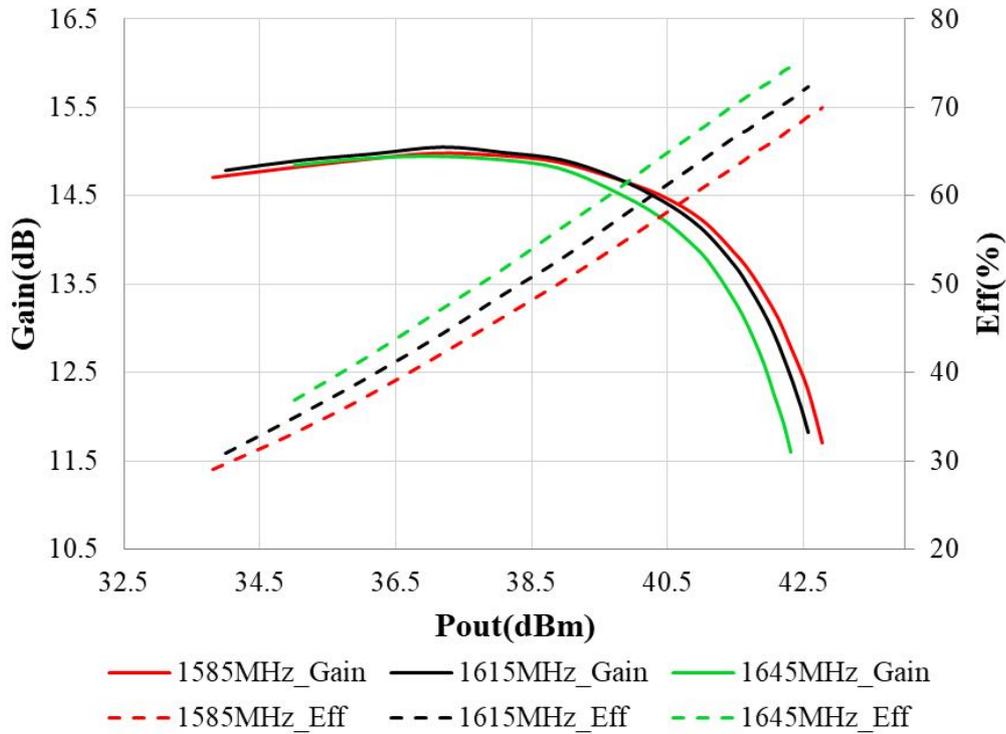


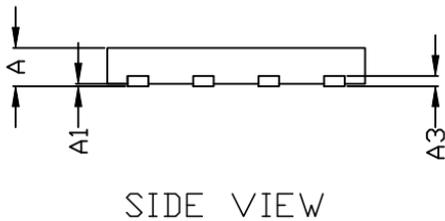
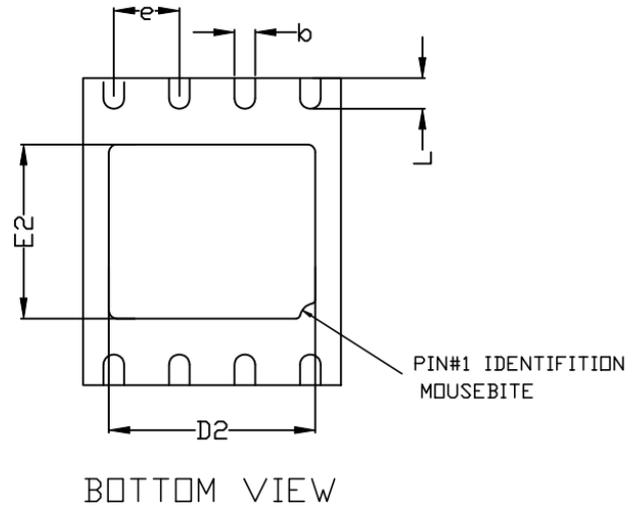
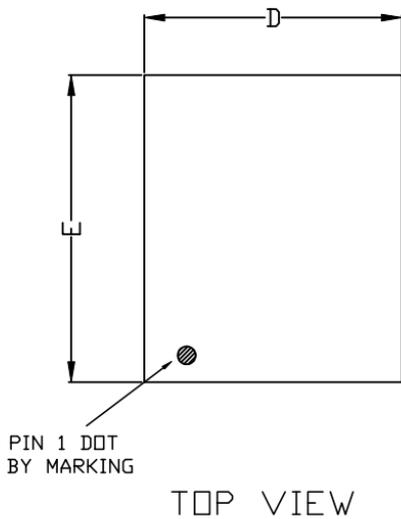
figure1. YP161515T Power sweep

Bias2: YP161515T, VDD=12V, IDQ=100mA; YP2233W, VCC=5V, VR=2.65V



figure2. S21&S11 of YP2233W+YP161515T

### Packaging Diagram



COMMON DIMENSIONS(MM)			
PKG.	W:VERY VERY THIN		
REF.	MIN.	NDM.	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF.		
D	4.95	5.00	5.05
E	5.95	6.00	6.05
D2	3.85	4.00	4.10
E2	3.25	3.40	3.50
b	0.35	0.40	0.45
L	0.50	0.60	0.70
e	1.27 BSC		

PIN 1 - PIN 4 : Gate  
 PIN 5 - PIN 8 : Drain  
 PIN 9(Pkg Base) : GND