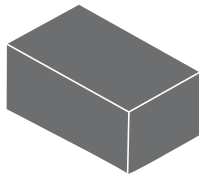
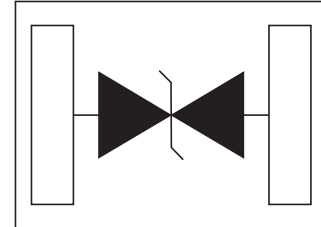


# Electro-Static Discharge for Automobile AUSD05CBL Bidirectional TVS Diode /Low Capacitance

## DFN1006



## Pin Configuration



## Features

- 60 Watts Peak Pulse Power per Line (tp=8/20μs)
- Protects one birectional I/O line
- Low clamping voltage
- Working voltages : 5V
- Low leakage current
- AEC-Q101

## IEC Compatibility

- IEC61000-4-2 (ESD) ±25kV (air), ±25kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ns)

## Applications

- Cell Phone Handsets and Accessories
- Microprocessor based equipment
- Personal Digital Assistants (PDA's)
- Notebooks, Desktops, and Servers
- Portable Instrumentation
- Peripherals
- Pagers

## Mechanical Characteristics

- JEDEC DFN1006 Package
- Terminal: Solder plated or Ni-Pd-Au plated
- Molding Compound Flammability Rating : UL 94V-O
- Weight 0.5 Milligrams (Approximate)
- Quantity Per Reel : 10,000pcs
- Reel Size : 7 inch
- Lead Finish : Lead Free

Maximum Ratings( $T_A=25^{\circ}\text{C}$  unless otherwise specified )

Parameter	Symbol	Value	Units
Peak Pulse Power( $t_p=8/20\mu\text{s}$ )	$P_{PP}$	60	Watts
Lead Soldering Temperature	$T_L$	260(10 sec.)	$^{\circ}\text{C}$
Operating Temperature Range	$T_J$	-55~150	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-55~150	$^{\circ}\text{C}$

Electrical Characteristics( $T_A=25^{\circ}\text{C}$  unless otherwise specified )

AUSD05CBL(Marking:B1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-off Voltage	$V_{RWM}$				5	V
Breakdown Voltage	$V_{BR}$	$I_T=1\text{mA}$	5.6			V
Clamping Voltage	$V_C$	$I_{PP}=1\text{A}, t_p=8/20\mu\text{s}$			12	V
		$I_{PP}=3\text{A}, t_p=8/20\mu\text{s}$			20	V
Reverse Leakage Current	$I_R$	@ $V_{RWM}$			1	$\mu\text{A}$
Junction Capacitance	$C_{I/O}$	0Vdc, f=1MHz Between I/O Pins and GND		0.3	0.4	pF

Ratings and Characteristic Curves

Fig.1 Non-Repetitive Pulse Power vs.Pulse Time

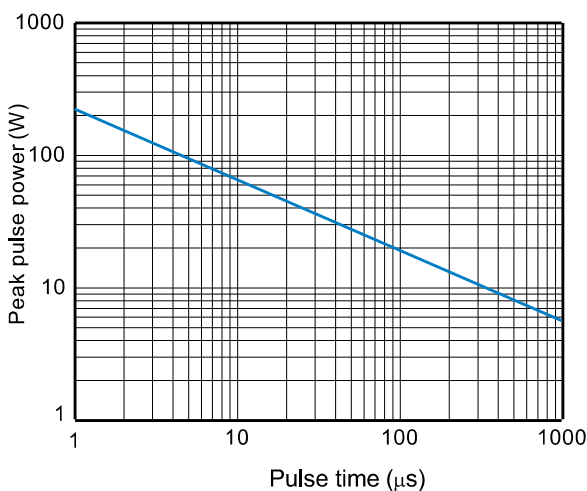
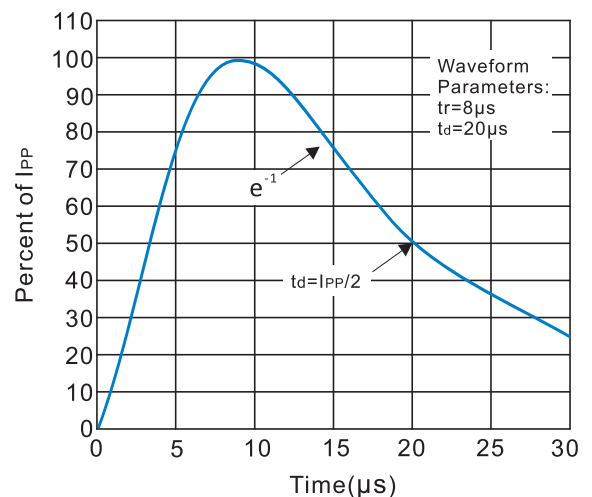
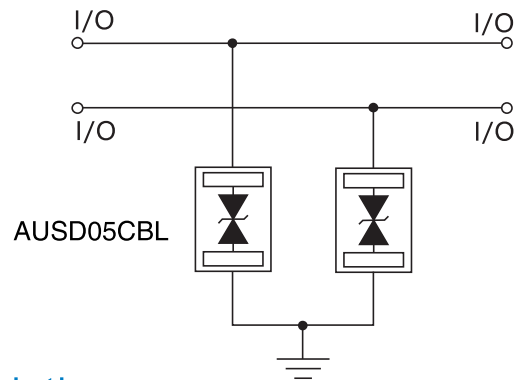


Fig.2 Pulse Waveform



## Application

### I/O Protection

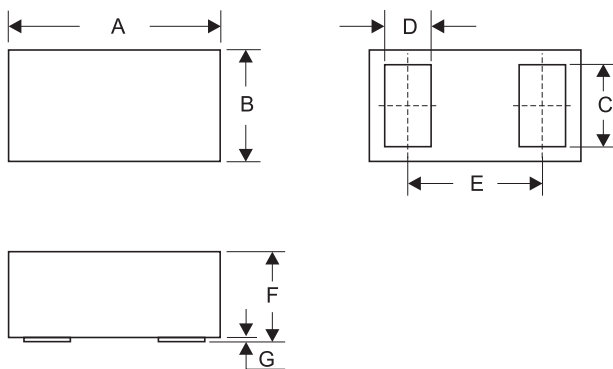


## PCB Layout Recommendations

The location and circuit board layout is critical to maximize the effectiveness of the I/O protection circuit. The following guidelines are recommended:

- Locate the protection devices as close as possible to the I/O connector. This allows the protection devices to absorb the energy of the transient voltage before it can be coupled into the adjacent traces on the PCB.
- Minimize the loop area for the high-speed data lines, power and ground lines to reduce the radiated emissions.
- Avoid running protection conductors in parallel with unprotected conductors
- Use ground planes wherever possible to reduce the parasitic capacitance and inductance of the PCB that degrades the effectiveness of a filter device.
- Using shared transient return paths to a common ground point.

## Dimensions(DFN1006)



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	0.95	1.07	0.037	0.042
B	0.55	0.65	0.022	0.026
C	0.45	0.55	0.017	0.022
D	0.20	0.40	0.008	0.016
E	0.65BSC		0.026BSC	
F	0.40	0.55	0.015	0.022
G	0.00	0.10	0.000	0.004