DFN2020-6L Plastic-Encapsulate MOSFETS

Features

- V_{DS}=-30V
- I_D=-4.5A
- $R_{DS(on)}$@V_{GS}=-10V ＜ 55mΩ
- $R_{DS(on)}$@V_{GS}=-4.5V ＜ 85mΩ
- Advanced trench cell design
- Low Thermal Resistance
- Low Gate Charge

Drain-source Voltage
-30 V
Drain Current
-4.5 Ampere

Applications

- Load Switch for Protable Devices
- Voltage controlled small signal switch

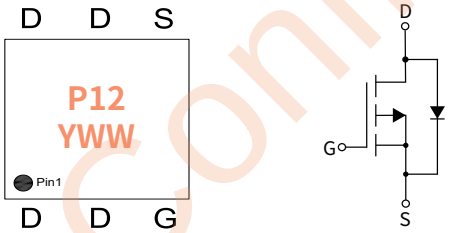
DFN2020-6L

Mechanical Data

- Case: DFN2020-6L
  Molding compound meets UL 94V-0 flammability rating, RoHS-compliant,halogen-free
- Terminals: Solder plated, solderable per MIL-STD-750,Method 2026

Function Diagram

Marking：P12
Date Code：YWW



Ordering Information

PACKAGE	PACKAGE CODE	UNIT WEIGHT(g)	REEL(pcs)	BOX(pcs)	CARTON(pcs)	DELIVERY MODE
DFN2020-6L	R3	0.01	3000	30000	120000	7''

Maximum Ratings (Ta=25°C Unless otherwise specified)

PARAMETER	SYMBOL	UNIT	VALUE
Drain-source Voltage	V_{DS}	V	-30
Gate-source Voltage	V_{GS}	V	±20
Drain Current(1)	I_D	A	-4.5
Pulsed Drain Current (2)	I_{DM}	A	-20
Total Power Dissipation	P_D	W	1.9
Junction temperature	T_J	°C	-55 ~+150
Storage temperature	T_{stg}	°C	-55 ~+150
Thermal Resistance Junction-to-Case(1)	$R_{\theta JC}$	°C / W	30
Thermal Resistance Junction-to-Ambient(1)	$R_{\theta JA}$	°C / W	65

Static Parameter Characteristics (Tj=25°C Unless otherwise specified)

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	V	-30	—	—
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V	μA	—	—	-1.0
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	nA	—	—	±100
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	V	-1.0	-1.5	-2.5
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-4.1A	mΩ	—	42	55
		V_{GS}= -4.5V, I_D=-3.5A		—	62	85

Dynamic Parameters

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHZ	pF	—	470	—
Output Capacitance	C_{oss}			—	126	—
Reverse Transfer Capacitance	C_{rss}			—	61	—

Switching Parameters

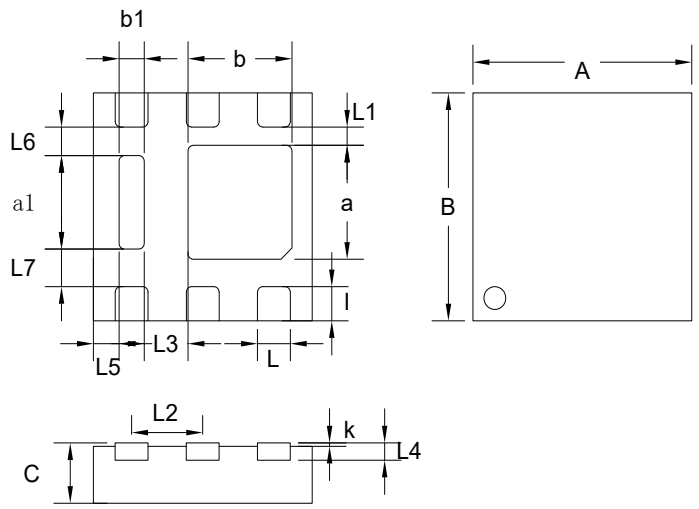
PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DD}=-15V, I_D=-1A ,R_{GEN}=6Ω	nS	—	7	—
Turn-on Rise Time	t_r		nS	—	12	—
Turn-off Delay Time	$t_{D(off)}$		nS	—	16	—
Turn-off fall Time	t_f		nS	—	6	—
Total Gate Charge	Q_g	V_{DS}=-15V, I_D=-4A V_{GS}=-5V	nC	—	6	—
Gate-Source Charge	Q_{gs}		nC	—	2.1	—
Gate-Drain Charge	Q_{gd}		nC	—	2	—

Drian-Source Diode Characteristics

PARAMETER	SYMBOL	Condition	UNIT	Min	Typ	Max
Diode Forward Voltage	V_{SD}	I_S=-4.5A, V_{GS}=0V	V	—	—	-1.2
Maximum Body-Diode Continuous Current	I_S	—	A	—	—	-4.5

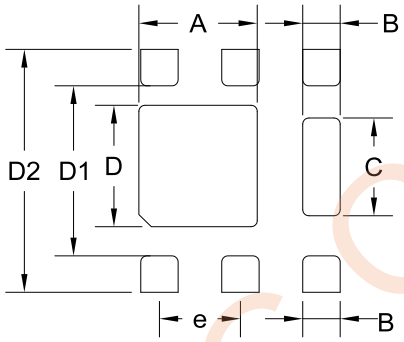
Note :
(1)$R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.$R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. Based on 1 in2 pad of 2 oz copper.
(2)Pulse test: Pulse width ⩽ 300us, duty cycle ⩽ 2%.

Package Outline Dimensions (DFN2020-6L)



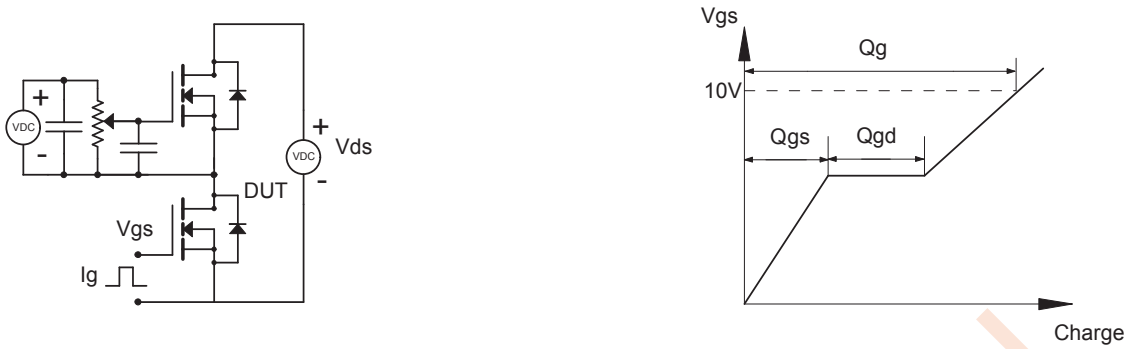
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.90	2.10	0.075	0.083
B	1.90	2.10	0.075	0.083
C	0.50	0.60	0.020	0.024
L	0.25	0.35	0.010	0.014
L1	0.10	0.30	0.004	0.012
L2	0.65 TYP		0.026 TYP	
L3	0.35TYP		0.014 TYP	
L4	0.127 TYP		0.005 TYP	
L5	0.12	0.32	0.005	0.013
L6	0.15	0.35	0.006	0.014
L7	0.25TYP		0.010TYP	
a	0.75	0.85	0.030	0.033
a1	0.75	0.85	0.030	0.033
b	0.90	1.0	0.035	0.039
b1	0.25	0.35	0.010	0.014
l	0.30	0.40	0.012	0.016
K	0	0.05	0	0.002

Suggested Pad Layout

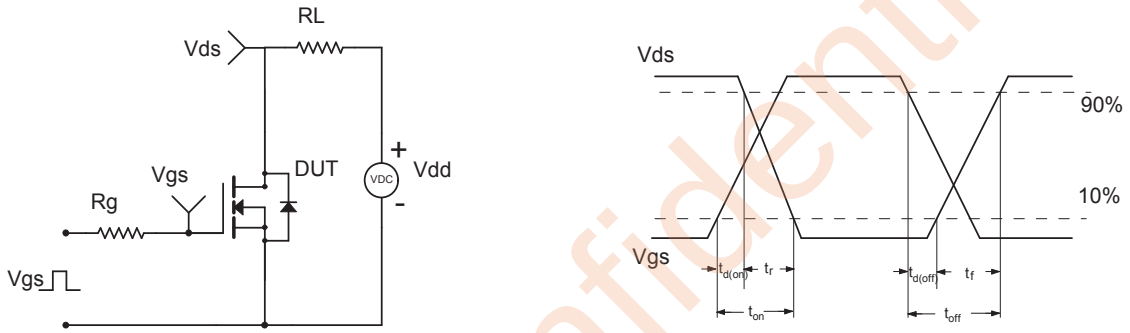


Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043
B	0.30	0.50	0.012	0.020
C	0.56	0.76	0.022	0.030
D	0.95	1.15	0.037	0.045
D1	1.30	1.50	0.051	0.059
D2	2.20	2.40	0.087	0.094
e	0.55	0.75	0.022	0.030

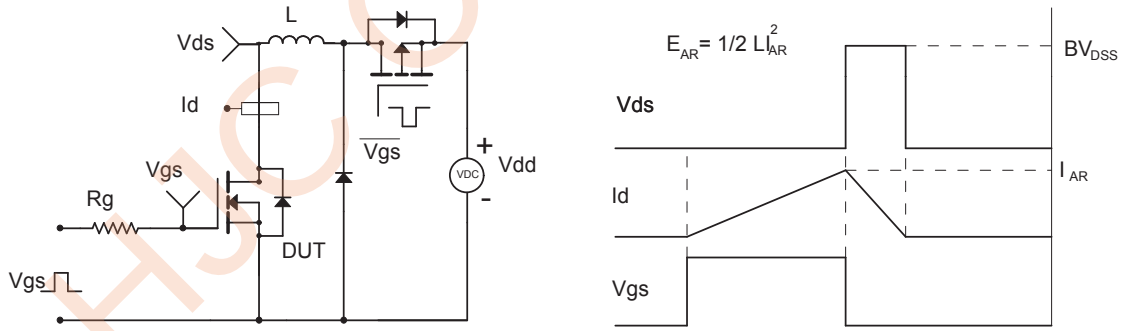
1.Gate Charge Test Circuit & Waveforms



2. Resistive Switching Test Circuit & Waveforms



3.Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



4.Diode Recovery Test Circuit & Waveforms