

## HMC545AETR-HX GaAs MMIC SPDT SWITCH, DC -3 GHz

## Description

The HMC545AETR-HX are low-cost, single-pole double-throw (SPDT) switches housed in compact 6-lead SOT-23-6 plastic packages, designed for general-purpose switching applications demanding exceptionally low insertion loss and minimal footprint. Featuring a typical insertion loss of just 0.25 dB, these devices support signal control from DC to 3.0 GHz and are particularly well suited for IF and RF applications—including cellular/3G, ISM band, automotive, and portable systems. Their optimized design delivers outstanding insertion loss performance, making them ideal for filter and receiver switching. When in the “Off” state, RF1 and RF2 present reflective short circuits. The two control inputs require only minimal DC current and are compatible with CMOS and select TTL logic families.

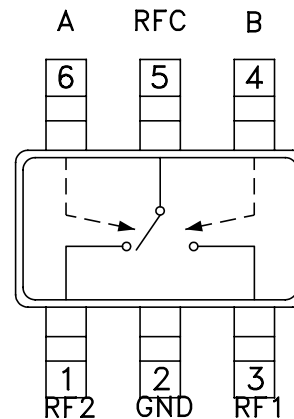
## Features

- ★ Low Insertion Loss: 0.27 dB
- ★ High Input IP3: +54 dBm
- ★ Low DC Power Consumption
- ★ Positive Control: 0/+3V to 0/+8V
- ★ Ultra Small Package: SOT-23-6

## Applications

- ★ Cellular/3G Infrastructure
- ★ Private Mobile Radio Handsets
- ★ WLAN, WiMAX & WiBro
- ★ Automotive Telematics
- ★ Test Equipment

## Functional Diagram

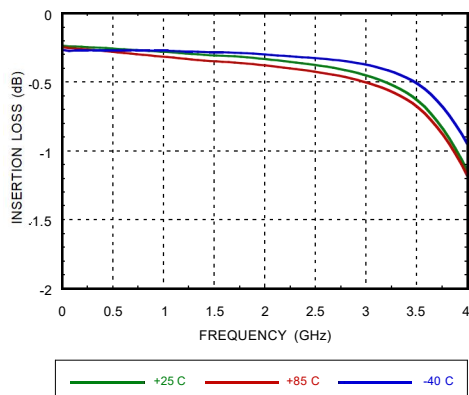


## Electrical Specifications

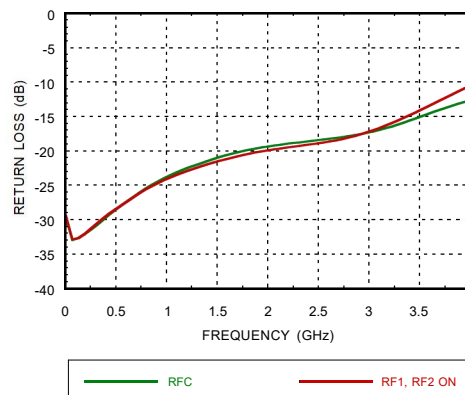
$T_A = +25^\circ\text{C}$ ,  $V_{ctl} = 0/+5\text{ Vdc}$  (Unless Otherwise Stated), 50 Ohm System

Parameter		Frequency	Min	Typ	Max	Units
Insertion Loss		DC - 1.0 GHz		0.27	0.4	dB
		DC - 2.5 GHz		0.3	0.5	dB
		DC - 3.0 GHz		0.4	0.7	dB
Isolation		DC - 2.0 GHz	26	31		dB
		DC - 2.5 GHz	22	26		dB
		DC - 3.0 GHz	19	22		dB
Return Loss		DC - 1.0 GHz		24		dB
		DC - 2.0 GHz		20		dB
		DC - 2.5 GHz		19		dB
		DC - 3.0 GHz		17		dB
Input Power for 1 dB Compression	Vctl = 0/+3V	0.5 - 3.0 GHz	20	23		dBm
	Vctl = 0/+5V		27	30		dBm
	Vctl = 0/+8V		30	33		dBm
Input Third Order Intercept (Two-tone Input Power = +17 dBm Each Tone)	Vctl = 0/+3V	0.5 - 3.0 GHz		31		dBm
	Vctl = 0/+5V			51		dBm
	Vctl = 0/+8V			54		dBm
Switching Characteristics		DC - 3.0 GHz		70		ns
tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)				90		ns

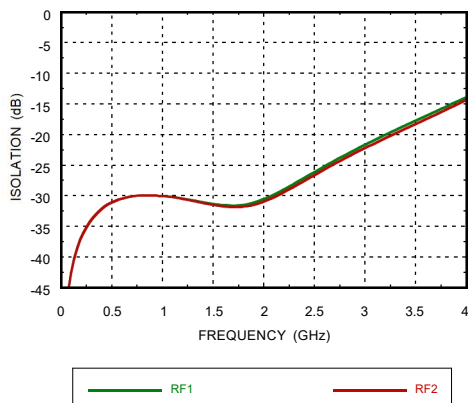
**Insertion Loss**



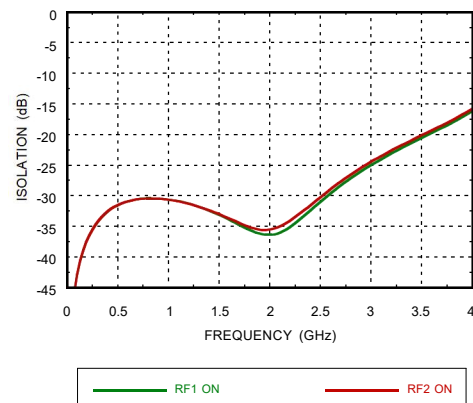
**Return Loss**



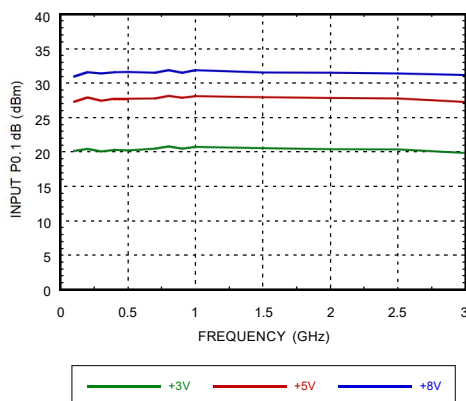
**Isolation Between Ports RFC and RF1/RF2**



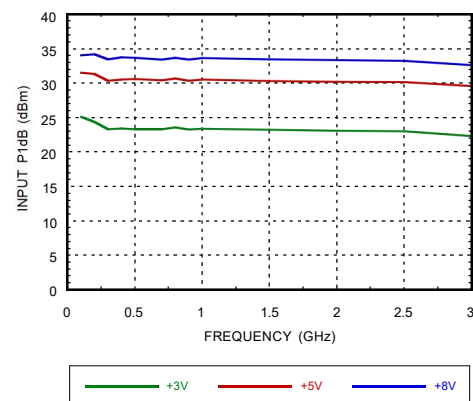
**Isolation Between Ports RF1 and RF2**



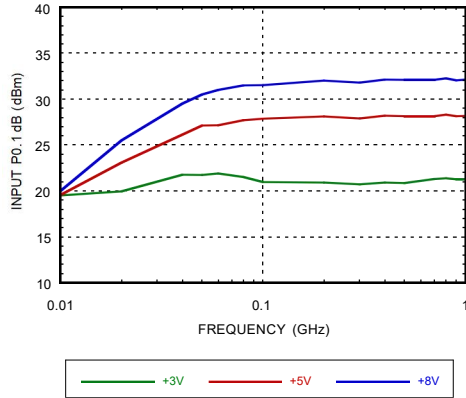
**Input P0.1dB vs. Vctl**



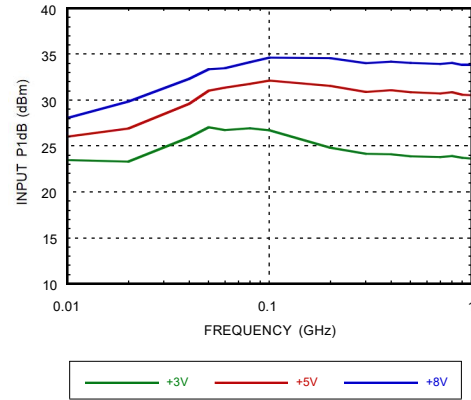
**Input P1dB vs. Vctl**



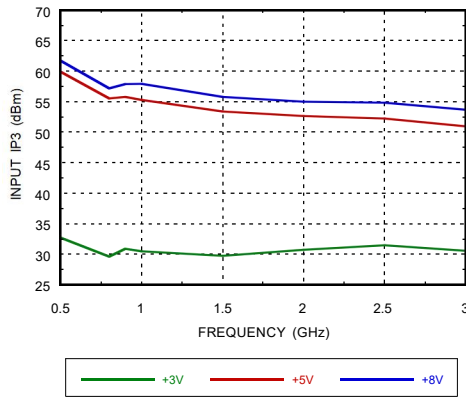
Low Frequency Input P0.1dB vs. Vctl



Low Frequency Input P1dB vs. Vctl



Input Third Order Intercept Point vs. Control Voltage

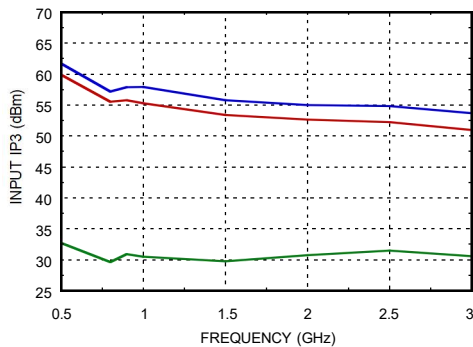


Absolute Maximum Ratings

RF Input Power (Vctl = 0/+8V)	+34 dBm
Control Voltage Range (A & B)	-0.2 to +12 Vdc
Hot Switch Power Level (Vctl = 0/+8V)	+32 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 5.6 mW/ °C above 85°C)	0.1 W
Thermal Resistance	169°C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

DC blocks are required at ports RFC, RF1 and RF2.

Insertion Loss, T = +25 °C



ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS

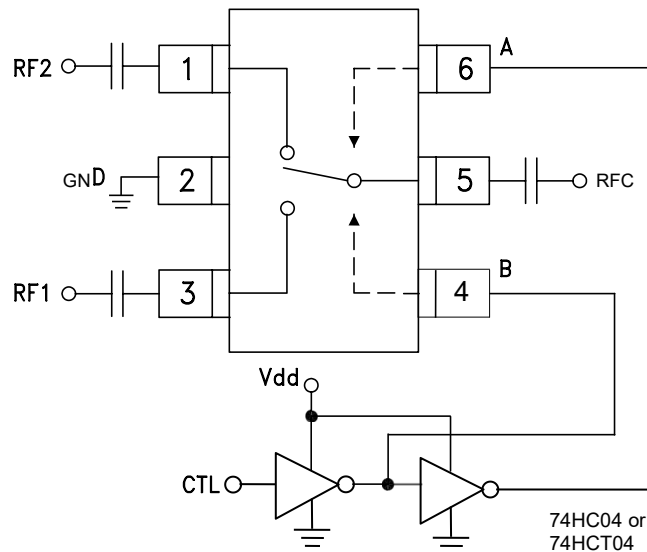
Truth Table

Control Input		Control Current	
A	B	RFC to RF1	RFC to RF2
Low	High	Off	On
High	Low	On	Off

Control Voltages

State	Bias Condition
Low	0 to 0.2 Vdc @ 1 $\mu$ A Typical
High	+3 Vdc @ 0.5 $\mu$ A Typical to +8 Vdc @ 14 $\mu$ A Typical ( $\pm$ 0.2 Vdc)

## Typical Application Circuit



### Notes:

1. Set logic gate Vdd = +3V to +5V and use HCT series logic to provide a TTL driver interface.
2. Control inputs A/B can be driven directly with CMOS logic (HC) with Vdd of +3V to +8V applied to the CMOS logic gates.
3. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation.
4. Highest RF signal power capability is achieved with Vdd = +8V and A/B set to 0/+8V.

## Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5	RF2, RF1, RFC	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
2	GND	This pin must be connected to RF/DC ground.	
4	B	See truth and control voltage tables.	
6	A	See truth and control voltage tables.	

## List of Materials for Evaluation PCB HMC545AETR-HX <sup>[1]</sup>

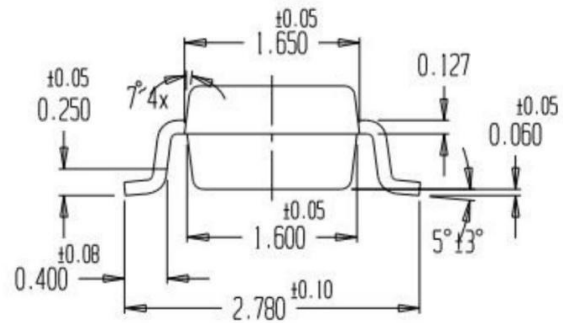
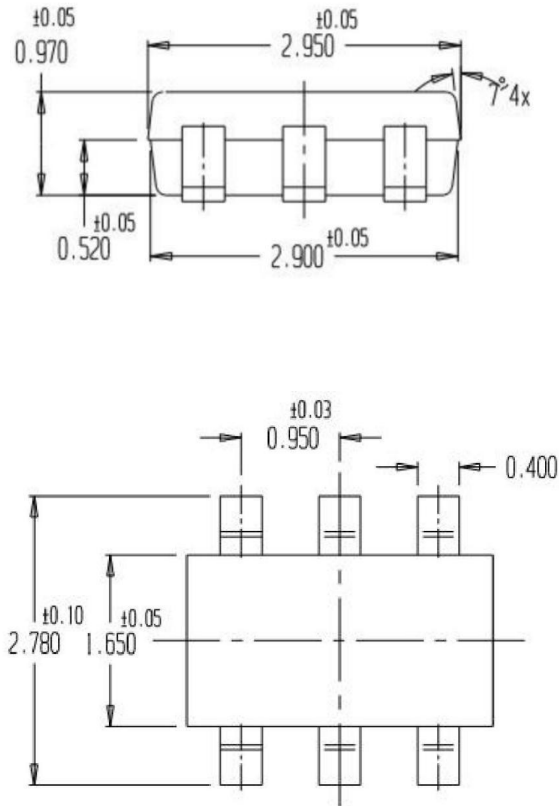
Item	Description
J1 - J3	PCB Mount SMA RF Connector
J4 - J6	DC Pin
R1 - R2	1K Ohm resistor, 0402 Pkg.
C1 - C3	330 pF capacitor, 0402 Pkg.
U1	HMC545AETR-HX SPDT Switch
PCB [2]	101659 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 Ohm impedance and the package ground leads should be connected directly to the ground plane similar to that shown above.

## Outline Drawing SOT-23-6



### NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
4. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
5. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

## Package Information

Part Number	Package Body Material	Packaging	MSL Rating
HMC545AETR-HX	RoHS-compliant Low Stress Injection Molded Plastic	SOT-23-6	MSL1 <sup>[2]</sup>

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C