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TPNLSX4373DR2G

2-Bit 20 Mb/s Dual-Supply Level Translator

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Features

- VL can be Less than, Greater than or Equal to VCC
- Wide VCC Operating Range: 1.5 V to 5.5 V
  Wide VL Operating Range: 1.5 V to 5.5 V
- Low Bit−to−Bit Skew
- High−Speed with 20 Mb/s Guaranteed Date Rate
- Integrated 10 kΩ Pullup Resistors
- Nonpreferential Powerup Sequencing
- Enable Input and I/O Lines have Overvoltage Tolerant (OVT) to 5.5 V
- This is a Pb−Free Device
- package: SOP-8

Applications

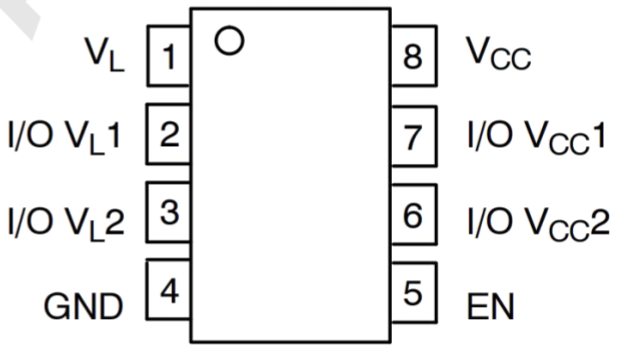
- I^2C, SMBus, PMBus
- Low Voltage ASIC Level Translation
- Mobile Phones, PDAs, Cameras

General Description

The is a 2−bit configurable dual−supply bidirectional auto sensing translator that does not require a directional control pin. The VCC I/O and VL I/O ports are designed to track two different power supply rails, VCC and VL respectively. The VCC supply rail is configurable from 1.5 V to 5.5 V while VL supply rail is configurable to 1.5 V to 5.5 V. This allows voltage logic signals on the VL side to be translated into lower, higher or equal value voltage logic signals on the VCC side, and vice−versa.

The translator has open−drain outputs with integrated

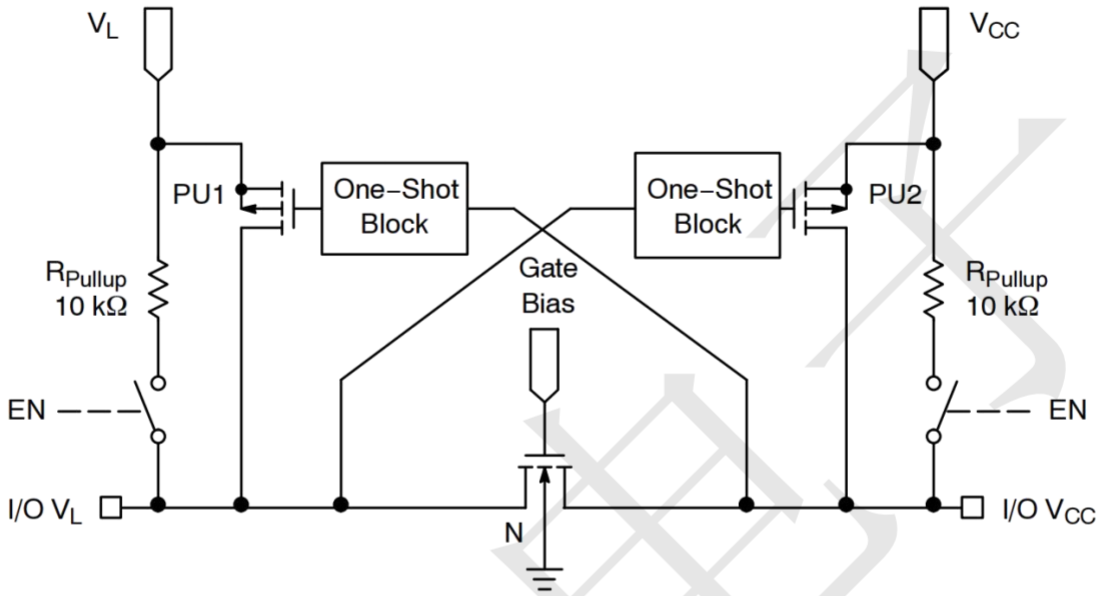
Pinout (top view)



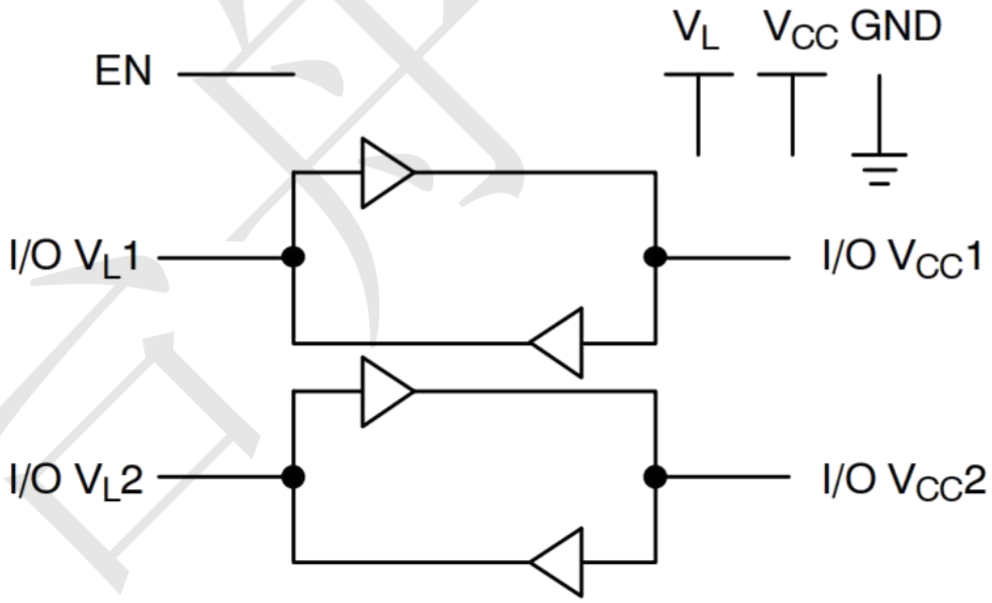
Pin Configurations

Pin Number	Pin Name	Pin Function
1	VL	VL Input Voltage
2	I/O VL1	VL I/O Port, Referenced to VL
3	I/O VL2	VL I/O Port, Referenced to VL
4	GND	Ground
5	EN	Output Enable
6	I/O VCC2	VCC I/O Port, Referenced to VCC
7	I/O VCC1	VCC I/O Port, Referenced to VCC
8	VCC	Supply Voltage

Block Diagram



LOGIC DIAGRAM



FUNCTION TABLE

EN	Operating Mode
L	Hi−Z
H	I/O Buses Connected

Absolute Maximum Ratings

Symbol	Parameter	Value	Condition	Unit
V_{CC}	High−side DC Supply Voltage	−0.3 to +7.0		V
V_L	High−side DC Supply Voltage	−0.3 to +7.0		V
I/O V_{CC}	V_{CC}−Referenced DC Input/Output Voltage	−0.3 to (V_{CC} + 0.3)		V
I/O V_L	V_L−Referenced DC Input/Output Voltage	−0.3 to (V_L + 0.3)		V
V_{EN}	Enable Control Pin DC Input Voltage	−0.3 to +7.0		V
I_{I/O_SC}	Short−Circuit Duration (I/O V_L and I/O V_{CC} to GND)	40	Continuous	mA
T_{STG}	Storage Temperature	−65 to +150		℃

Note: Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended operating conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	High−side Positive DC Supply Voltage	1.5	5.5	V
V_L	High−side Positive DC Supply Voltage	1.5	5.5	V
V_{EN}	Enable Control Pin Voltage	GND	5.5	V
V_{IO}	Enable Control Pin Voltage	GND	5.5	V
T_A	Operating Temperature Range	−40	+85	℃

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.5 V to 5.5 V and V_L = 1.5 V to 5.5 V, unless otherwise specified)

Symbol	Parameter	Test Conditions	–40°C to +85°C			Unit
			Min	Typ(1, 2)	Max	
V_{IHC}	I/O V_{CC} Input HIGH Voltage		V_{CC} – 0.4	--	--	V
V_{ILC}	I/O V_{CC} Input LOW Voltage		--	--	0.15	V
V_{IHL}	I/O V_L Input HIGH Voltage		V_L – 0.2	--	--	V
V_{ILL}	I/O V_L Input LOW Voltage		--	--	0.15	V
V_{IH}	Control Pin Input HIGH Voltage		V_L – 0.2	--	--	V
V_{IL}	Control Pin Input LOW Voltage		--	--	0.15	V
V_{OHC}	I/O V_{CC} Output HIGH Voltage	I/O VCC Source Current = 20 μA	2/3 * V_{CC}	--	--	V
V_{OLC}	I/O V_{CC} Output LOW Voltage	I/O VCC Sink Current = 20 μA	--	--	1/3 * V_{CC}	V
V_{OHL}	I/O V_L Output HIGH Voltage	I/O VL Source Current = 20 μA	2/3 * V_L	--	--	V
V_{OLL}	I/O V_L Output LOW Voltage	I/O V_L Sink Current = 20 μA	--	--	1/3 * V_L	V
I_{QVCC}	V_{CC} Supply Current	I/O VCC and I/O VL Unconnected, VEN = VL	--	0.5	2.0	μA
I_{QVL}	V_L Supply Current	I/O VCC and I/O VL Unconnected, VEN = VL	--	0.3	1.5	μA
I_{TS-VCC}	V_{CC} Tristate Output Mode Supply Current	I/O VCC and I/O VL Unconnected, VEN = GND	--	0.1	1.0	μA
I_{TS-VL}	V_L Tristate Output Mode Supply Current	I/O VCC and I/O VL Unconnected, VEN = GND	--	0.1	1.0	μA
I_{OZ}	I/O Tristate Output Mode Leakage Current	TA = +25℃	--	0.1	1.0	μA
R_{PU}	Pullup Resistor I/O V_L and V_{CC}	TA = +25℃	--	10	--	kΩ

Note:

1. Typical values are for V_{CC} = +2.8 V, V_L = +1.8 V and T_A = +25℃.
2. All units are production tested at T_A = +25℃. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS −RAIL−TO−RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (3 and 4)			Unit
			Min	Typ	Max	
V_L = 1.5 V, V_{CC} = 5.5 V						
t_{RVCC}	I/O V_{CC} Risetime		--	--	15	ns
t_{FVCC}	I/O V_{CC} Falltime		--	--	20	ns
t_{RVL}	I/O V_L Risetime		--	--	30	ns
t_{FVL}	I/O V_L Falltime		--	--	10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)		--	--	20	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})		--	--	20	ns
t_{PPSKEW}	Part−to−Part Skew		--	--	5	nS
	Maximum Data Rate		20	--	--	Mb/s
V_L = 1.8 V, V_{CC} = 2.8 V						
t_{RVCC}	I/O V_{CC} Risetime		--	--	15	ns
t_{FVCC}	I/O V_{CC} Falltime		--	--	15	ns
t_{RVL}	I/O V_L Risetime		--	--	25	ns
t_{FVL}	I/O V_L Falltime		--	--	10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)		--	--	15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})		--	--	15	ns
t_{PPSKEW}	Part−to−Part Skew		--	--	5	nS
	Maximum Data Rate		20	--	--	Mb/s
V_L = 2.5 V, V_{CC} = 3.6 V						
t_{RVCC}	I/O V_{CC} Risetime		--	--	15	ns
t_{FVCC}	I/O V_{CC} Falltime		--	--	10	ns
t_{RVL}	I/O V_L Risetime		--	--	15	ns
t_{FVL}	I/O V_L Falltime		--	--	10	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)		--	--	15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})		--	--	15	ns
t_{PPSKEW}	Part−to−Part Skew		--	--	5	nS
	Maximum Data Rate		20	--	--	Mb/s

Note: 3.Typical values are for V_{CC} = +3.3 V, V_L = +1.8 V and T_A = +25℃.
4.All units are production tested at T_A = +25℃. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS − RAIL−TO−RAIL DRIVING CONFIGURATIONS

(I/O test circuit of Figures 2 and 3, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (3 and 4)			Unit
			Min	Typ	Max	
V_L = 3.6 V, V_{CC} = 2.5 V						
t_{RVCC}	I/O V_{CC} Risetime		--	--	15	ns
t_{FVCC}	I/O V_{CC} Falltime		--	--	10	ns
t_{RVL}	I/O V_L Risetime		--	--	15	ns
t_{FVL}	I/O V_L Falltime		--	--	15	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)		--	--	15	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})		--	--	15	ns
t_{PPSKEW}	Part−to−Part Skew		--	--	5	nS
	Maximum Data Rate		20	--	--	Mb/s
V_L = 5.5 V, V_{CC} = 1.5 V						
t_{RVCC}	I/O V_{CC} Risetime		--	--	30	ns
t_{FVCC}	I/O V_{CC} Falltime		--	--	10	ns
t_{RVL}	I/O V_L Risetime		--	--	15	ns
t_{FVL}	I/O V_L Falltime		--	--	20	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)		--	--	20	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})		--	--	20	ns
t_{PPSKEW}	Part−to−Part Skew		--	--	5	nS
	Maximum Data Rate		20	--	--	Mb/s

Note: 3.Typical values are for V_{CC} = +3.3 V, V_L = +1.8 V and T_A = +25℃.
4.All units are production tested at T_A = +25℃. Limits over the operating temperature range are guaranteed by design.

TIMING CHARACTERISTICS –OPEN DRAIN DRIVING CONFIGURATIONS

(I/O test circuit of Figures 4 and 5, C_{LOAD} = 15 pF, driver output impedance ≤ 50 Ω, R_{LOAD} = 1 MΩ)

Symbol	Parameter	Test Conditions	−40°C to +85°C (5 and 6)			Unit
			Min	Typ	Max	
+1.5 ≤ V_L ≤ V_{CC} ≤ +5.5 V						
t_{RVCC}	I/O V_{CC} Risetime		--	--	400	ns
t_{FVCC}	I/O V_{CC} Falltime		--	--	50	ns
t_{RVL}	I/O V_L Risetime		--	--	400	ns
t_{FVL}	I/O V_L Falltime		--	--	60	ns
$t_{PDVL-VCC}$	Propagation Delay (Driving I/O V_L)		--	--	1000	ns
$t_{PDVCC-VL}$	Propagation Delay (Driving I/O V_{CC})		--	--	1000	ns
t_{PPSKEW}	Part−to−Part Skew		--	--	50	nS
MDR	Maximum Data Rate		2	--	--	Mb/s

Note:5.Typical values are for V_{CC} = +3.3 V, V_L = +1.8 V and T_A = +25℃.
6.All units are production tested at T_A = +25℃. Limits over the operating temperature range are guaranteed by design.

TEST SETUPS

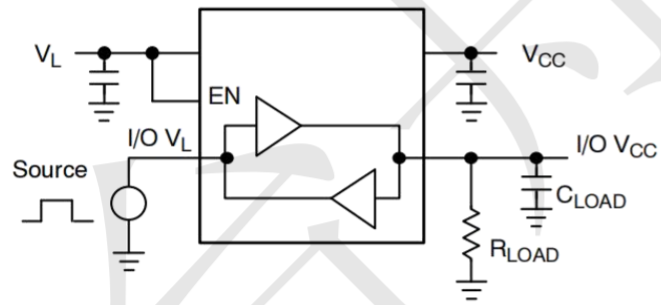


Figure 1. Rail−to−Rail Driving I/O V_L

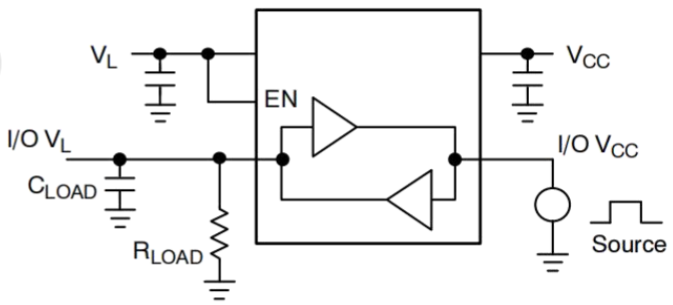


Figure 2. Rail−to−Rail Driving I/O V_{CC}

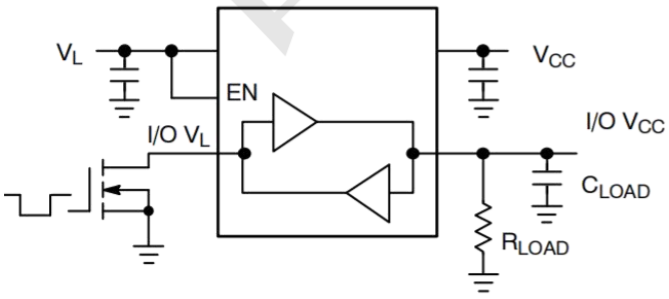


Figure 3. Open−Drain Driving I/O V_L

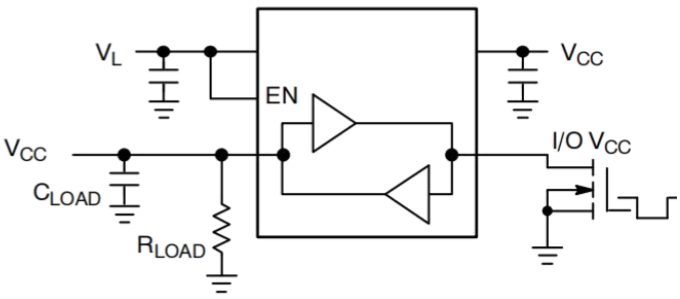


Figure 4. Open−Drain Driving I/O V_{CC}

TEST SETUPS

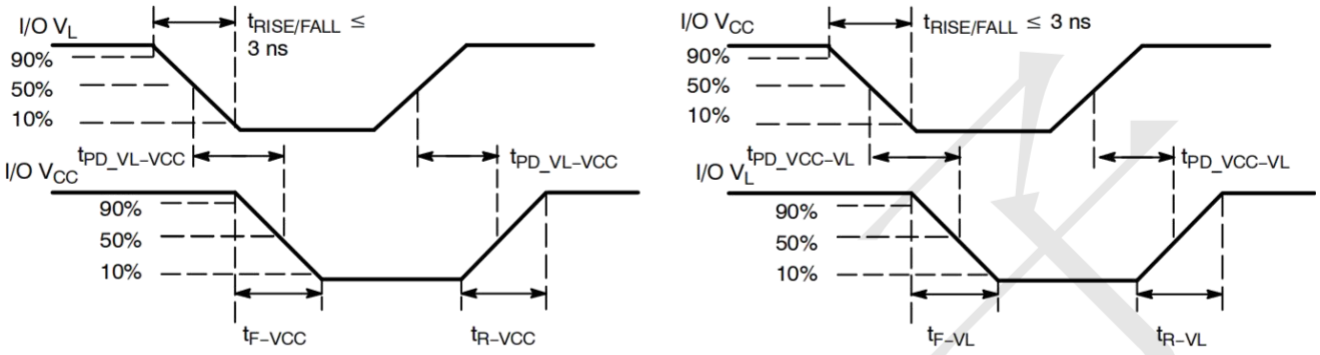
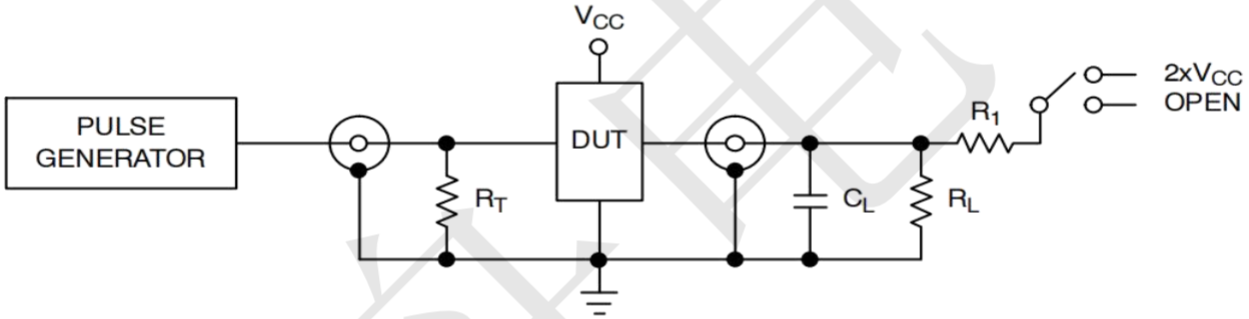


Figure 5. Definition of Timing Specification Parameters



Test	Switch
t_{PZH}, t_{PHZ}	Open
t_{PZL}, t_{PLZ}	2 x V_{CC}

C_L = 15 pF or equivalent (Includes jig and probe capacitance)
R_L = R_1 = 50 kΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 6. Test Circuit for Enable/Disable Time Measurement

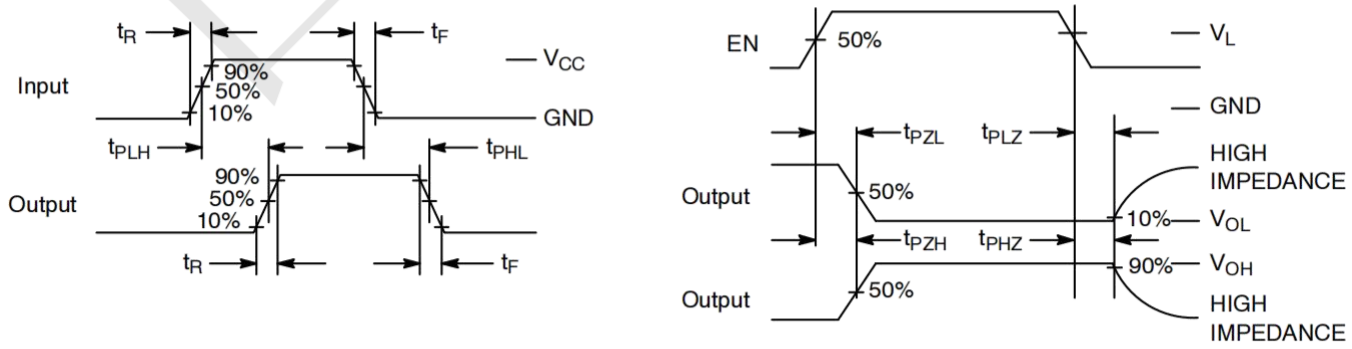
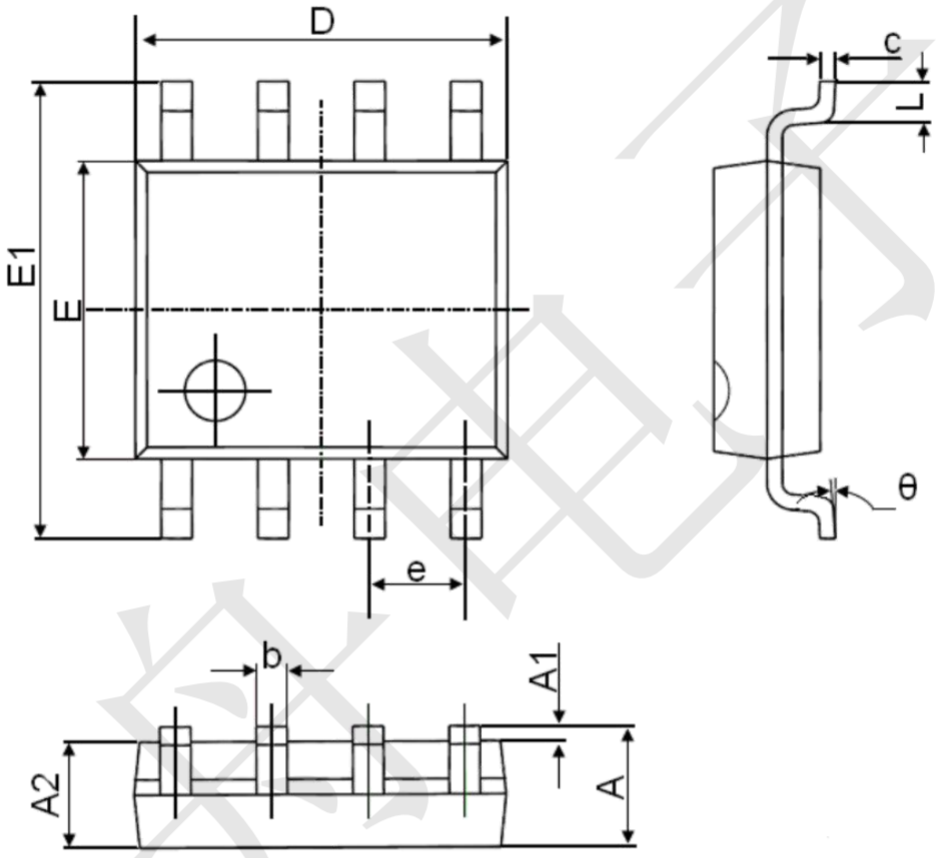


Figure 7. Timing Definitions for Propagation Delays and Enable/Disable Measurement

Package Information

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°