

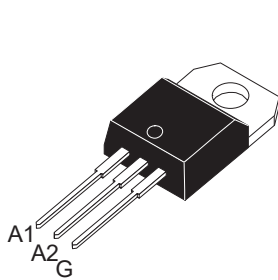
1.Description

NPNN five-layer structure of silicon bidirectional devices; with independent intellectual property rights of single-sided digging technology, table glass passivation process; multi-layer metallized electrodes on the back; with high blocking voltage and high temperature stability.

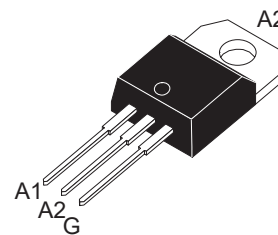
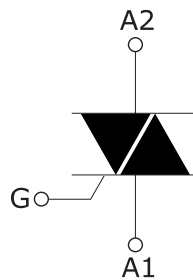
2.Features

vacuum cleaners, power tools and other motor speed controllers; solid state relays; heating controllers (temperature regulation); other phase control circuits.

3.Pinning Information



**TO-220AB
insulated
BTA24**



**TO-220AB
BTB24**



4. Absolute maximum ratings ($T_J=25^{\circ}\text{C}$ unless otherwise stated)

Parameter			Symbol	Values	Units
RMS on-state current (full sine wave)	BTA	T _C =80°C	I _{T(RMS)}	24	A
	BTB	T _C =90°C			
Non repetitive surge peak on-state current (full cycle, T _J initial=25°C)	F=50HZ, tp=20ms		I _{TSM}	240	A
I ² t value for fusing	tp=10ms		I ² t	288	A ² S
Critical rate of rise of on-state current I _G =2 x I _{GT} , tr≤100ns	T _J =125		di/dt	50	A/us
Off state repetitive peak voltage Reverse repetitive peak voltage	T _J =25°C		V _{DRM} /V _{RRM}	600/800	V
Peak gate current	tp=20us	T _J =150°C	I _{GM}	4	A
Average gate power dissipation		T _J =150°C	P _{G(AV)}	1	W
Storage junction temperature range			T _{STG}	-40 to 150	°C
Operating junction temperature range			T _J	-40 to 125	°C



5.1 Electrical characteristics (3 quadrants)

Parameter	Quadrant	Range	Symbol	CW	BW	Units
$V_D=12V$ $R_L=33\Omega$	I - II - III	MAX	$I_{GT}^{(1)}$	35	50	mA
	I - II - III	MAX	V_{GT}	1.3		V
$V_D=V_{DRM}$, $R_L=3.3k\Omega$, $T_J=125^\circ C$	I - II - III	MIN	V_{GD}	0.2		V
$I_T=500mA$		MAX	I_H	50	75	mA
$I_G=1.2 \times I_{GT}$	I - III	MAX	I_L	70	80	mA
	II	MAX		80	100	mA
$V_D = 67\% V_{DRM}$ gate open	$T_J=125^\circ C$	MIN	dv/dt	500	1000	V/ μs
Without snubber	$T_J=125^\circ C$	MIN	$(dv/dt)_c$	13	22	A/ms

(1) minimum I_{GT} is guaranteed at 5% of I_{GT} max.

5.2 Electrical characteristics (4 quadrants)

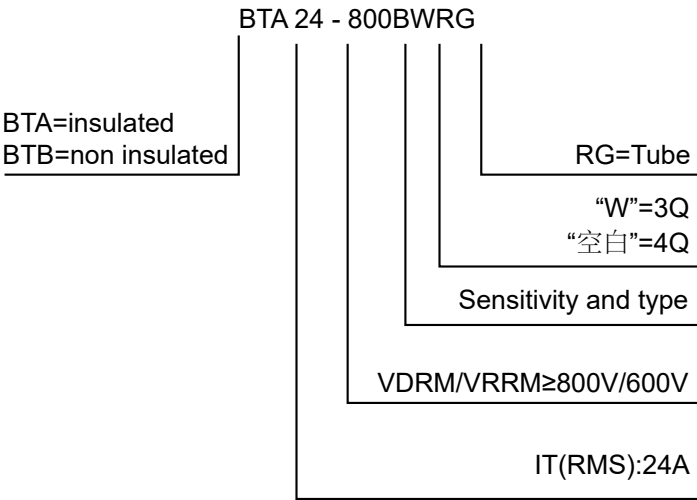
Parameter	Quadrant	Range	Symbol	value		Units
$V_D=12V$ $R_L=100\Omega$	I - II - III	MAX	I_{GT}	I II III	IV	mA
		MAX		≤ 50	≤ 120	mA
	IV	MAX	V_{GT}	1.5		V
$V_D=V_{DRM}$, $R_L=3.3k\Omega$, $T_J=125^\circ C$		MIN	V_{GD}	0.2		V
$I_T=500mA$		MAX	I_H	80		mA
$I_G=1.2 \times I_{GT}$		MAX	I_L	80		mA
		MAX		100		mA
$V_D = 67\% V_{DRM}$, gate open, mA, $T_J=125^\circ C$		MIN	dv/dt	500		V/us
Critical rise rate of commutation voltage $T_J=150^\circ C$		MIN	$(dv/dt)_c$	10		V/us



6.Static Parameters

Parameter			Symbol	Values	Units
$I_{TM}=50A$	$T_J=25^{\circ}C$	MAX	V_{TM}	1.55	V
threshold on-state voltage	$T_J=150^{\circ}C$	MAX	V_{T0}	0.87	V
Dynamic resistance	$T_J=150^{\circ}C$	MAX	R_d	14.6	mΩ
$V_{DRM}=V_{RRM}$	$T_J=25^{\circ}C$	MAX	I_{DRM}, I_{RRM}	5	uA
	$T_J=150^{\circ}C$	MAX		1	mA
Junction to ambient	BTA	MAX	$R_{th(j-c)}$	2.05	°C/W
	BTB	MAX		1.25	°C/W

7.Static Parameters





8.1 Typical Characteristic

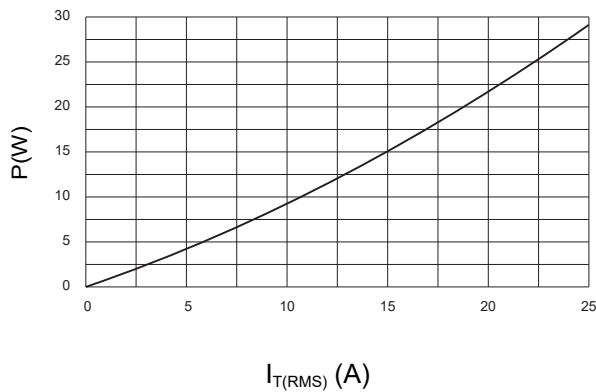


Figure 1: Maximum power dissipation versus RMS on-state current (full cycle)

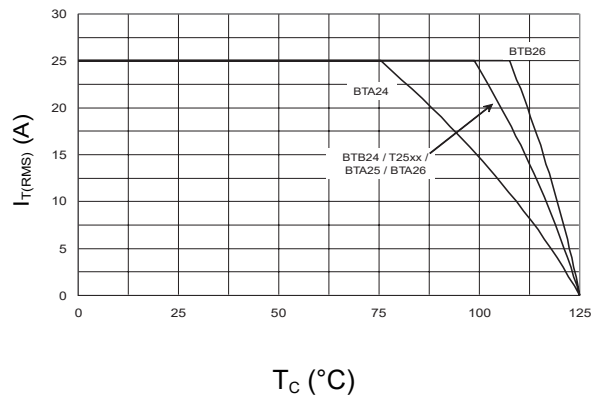


Figure 2: RMS on-state current versus case temperature (full cycle)

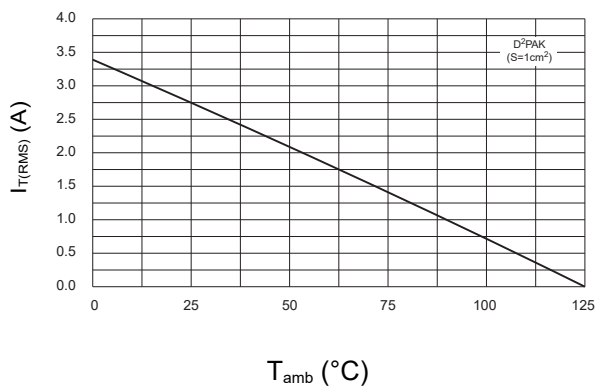


Figure 3: D²PAK RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35μm) (full cycle)

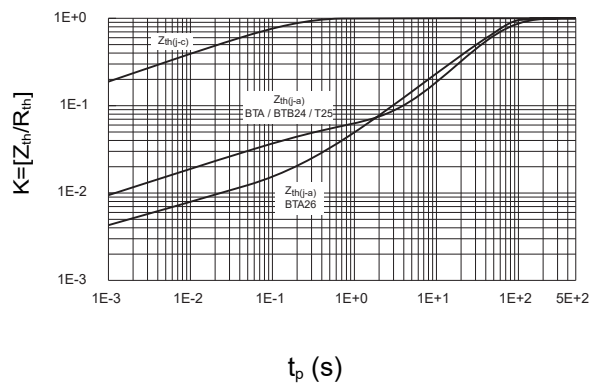


Figure 4: Relative variation of thermal impedance versus pulse duration

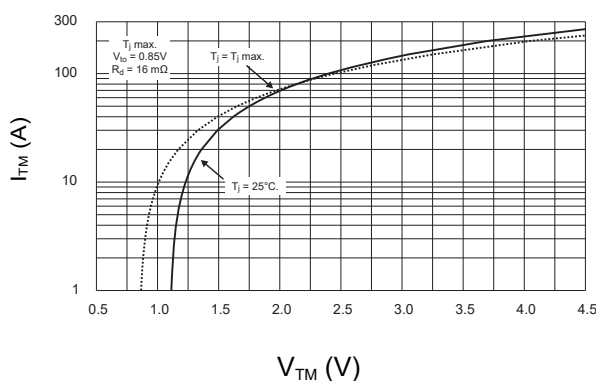


Figure 5: On-state characteristics (maximum values)

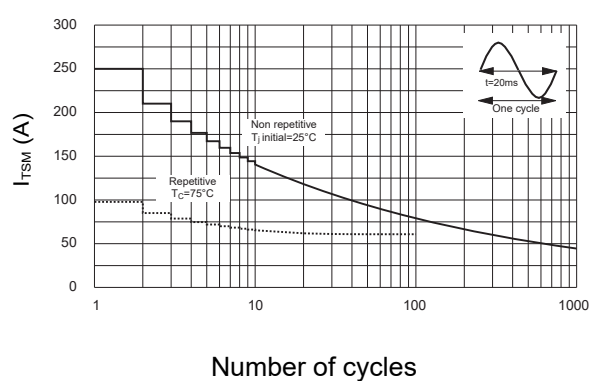


Figure 6: Surge peak on-state current versus number of cycles



8.2 Typical Characteristic

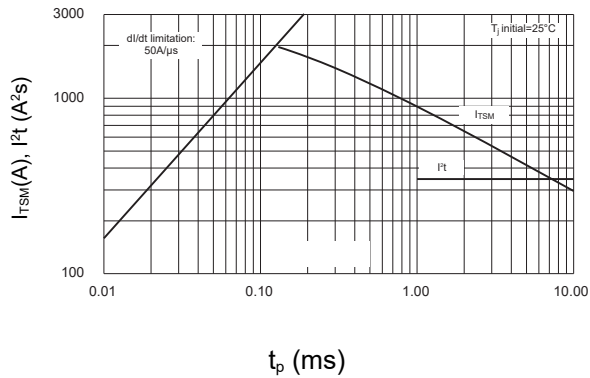


Figure 7: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms and corresponding value of I^2t

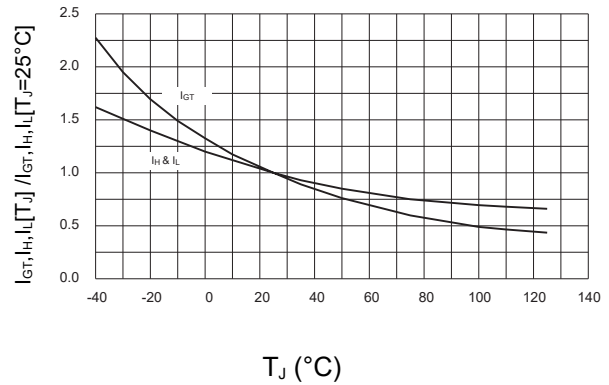


Figure 8: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

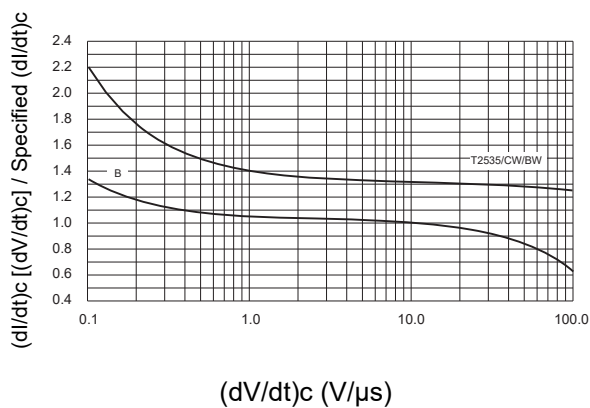


Figure 9: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values)

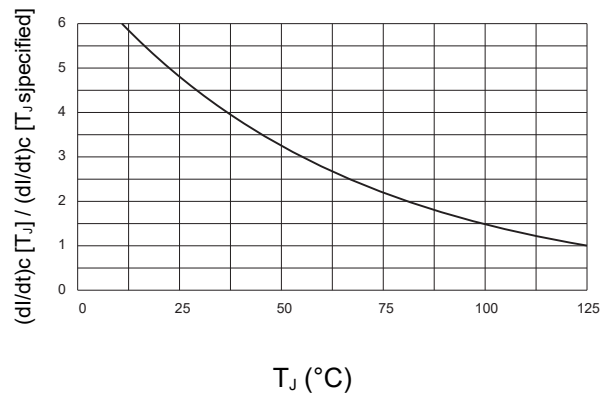


Figure 10: Relative variation of critical rate of decrease of main current versus T_J

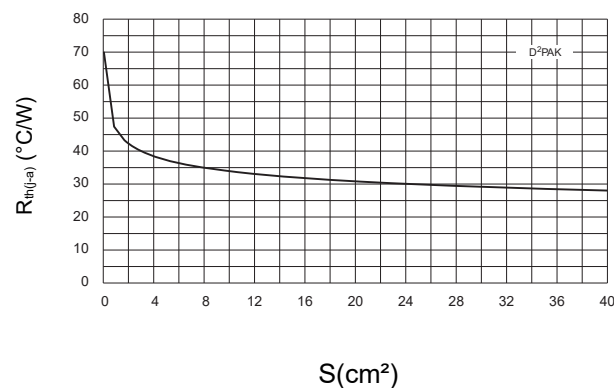
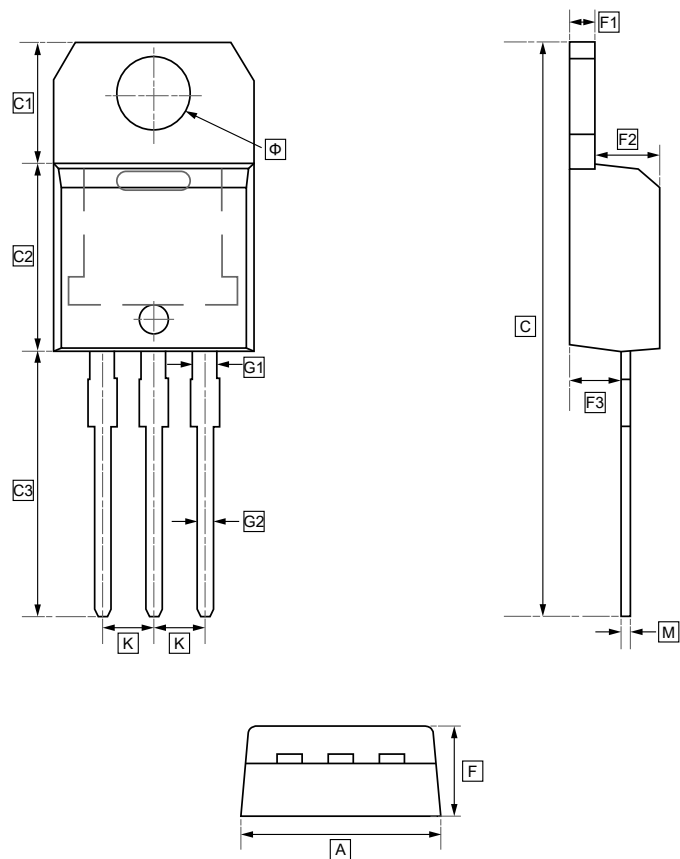


Figure 11: D²PAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 μm)



9.TO-220A/B Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	C	C1	C2	C3	Φ	F	F1	F2	F3	G1	G2
Min	9.900	28.600	6.100	9.240	13.160	3.700	4.320	1.200	3.120	2.300	1.200	0.750
Max	10.100	29.000	6.200	9.440	13.460	3.800	4.620	1.300	3.320	2.700	1.300	0.850

Symbol	M	K
Min	0.400	2.540
Max	0.500	



10.Ordering information

BTA24-600C
UMW yyww

yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW BTA24-600BWRG	BTA24-600BW	TO-220A	1000	Tube and box
UMW BTA24-600CRG	BTA24-600C	TO-220A	1000	Tube and box
UMW BTA24-600CWRG	BTA24-600CW	TO-220A	1000	Tube and box
UMW BTB24-600BRG	BTB24-600B	TO-220B	1000	Tube and box
UMW BTB24-600BWRG	BTB24-600BW	TO-220B	1000	Tube and box
UMW BTB24-600CWRG	BTB24-600CW	TO-220B	1000	Tube and box
UMW BTA24-800BRG	BTA24-800B	TO-220A	1000	Tube and box
UMW BTA24-800BWRG	BTA24-800BW	TO-220A	1000	Tube and box
UMW BTA24-800CRG	BTA24-800C	TO-220A	1000	Tube and box
UMW BTA24-800CWRG	BTA24-800CW	TO-220B	1000	Tube and box
UMW BTB24-800BRG	BTB24-800B	TO-220B	1000	Tube and box
UMW BTB24-800BWRG	BTB24-800BW	TO-220B	1000	Tube and box
UMW BTB24-800CWRG	BTB24-800CW	TO-220B	1000	Tube and box



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